Buck Converter Experiment Module

PEK-120

USER MANUAL

ISO-9001 CERTIFIED MANUFACTURER

GW INSTEK

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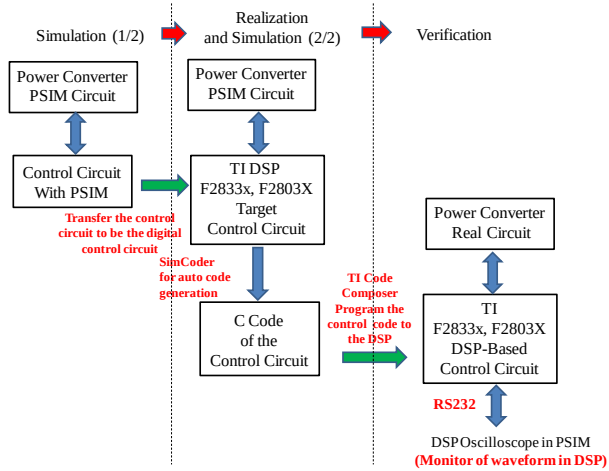
Introduction

The power converter utilizing digital control, which largely improves both functions and performances, further elevating the added values itself, is the mainstream tendency for the comtemporary industrial products. It has seen more and more digital control technologies deployed in power converters nowadays. The purpose of this manual as shown in the figure 1.1 is to provide a learning platform for power converter of specifically digital control, having users, via PSIM software, to understand the principle, analysis as well as design of power converter through simulating process. More than that, it helps convert, via SimCoder tool of PSIM, control circuit into digital control and proceed to simulation with the circuit of DSP, eventually burning the control program, through simulating verification, in the DSP chip. Also, it precisely verifies the accuracy of designed circuit and controller via control and communication of DSP.

Figure 1.1
The process in details



The main features of this teaching aid are eloaborated below.

1. To provide both electric and electronic analysis, design, simulation and practical verification.

2. To complete programming and burning via hardware circuit established within PSIM, facilitating new learner in DSP firmware to quickly grasp tips for programming, thus realizing the area of digital control with ease.

3. This teaching aid offers resourceful instructional materials containing SimCoder usage to set up method of hardware programming, in-depth instructions on teaching aid to each part of circuit, detailed principle and design of experimental circuit, PSIM circuit simulating file, DSP hardware layout and setting, the method of program burning, etc.

4. This teaching aid provides completely educational slides for both teachers and users' reference.

5. This teaching aid offers purchasers for free on any additional experimental items later.

Instruction on Teaching Aid of Buck DC-DC Converter Module

As the figure 1.2 shown, the buck DC-DC converter experimental module currently provides the following 5 experiments.

1. Pulse Width Modulation, PWM
2. Voltage mode control
3. Current mode control
4. (1) PV MPPT Control - Pertube and Observe method
   (2) PV MPPT control – Incremental Conductance method
5. PV Battery charger

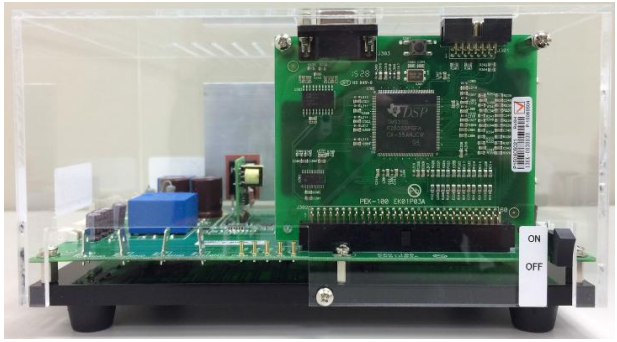


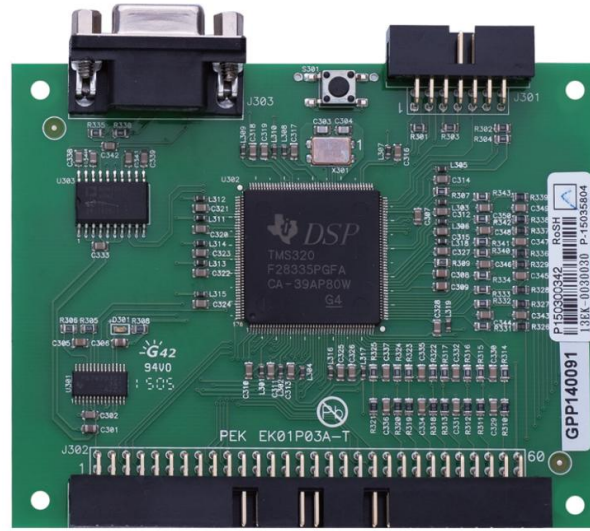
Figure 1.2 Buck DC-DC Converter experimental module

In addition to the Buck DC-DC Converter main power circuit, the experiment module comprises the following components.

DSP Control Module

- 2 modules, TI F28335 and F28035, are available.
- Each module is equipped with the isolated RS-232 interface, which allows DSP internal signal to be sent back to PSIM for observation during the process of experiment.

Figure 1.3 DSP Control Module



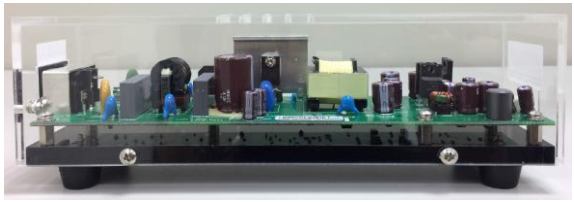
Auxiliary Power Module

Input voltage ranges from 100 to 250Vac with multiple isolated power outputs (+15V, -15V, 12V, 5V) and the output maximizes up to 23W. Check the table 1.1 for the specification.

Description	Symbol	Min	Typ	Max	Units
Input					
Voltage	V_{IN}	100		250	VAC
Frequency	f_{LINE}	47	50/60	63	Hz
Output					
Output Voltage 1	V_{OUT1}	11.4	12	12.6	V
Output Current 1	I_{OUT1}	0.1	0.5	0.6	A
Output Voltage 2	V_{OUT2}	11.4	12	12.6	V
Output Current 2	I_{OUT2}	0.1	0.5	0.6	A
Output Voltage 3	V_{OUT3}	14.25	15	15.75	V
Output Current 3	I_{OUT3}	0.1	0.2	0.24	A
Output Voltage 4	V_{OUT4}	-14.25	-15	-15.75	V
Output Current 4	I_{OUT4}	-0.1	-0.2	-0.24	A
Output Voltage 5	V_{OUT5}	4.75	5	5.25	V
Output Current 5	I_{OUT5}	0.5	1	1.2	A
Total Output Power	P_{OUT}	7.505	23	28.98	W

Table 1.1

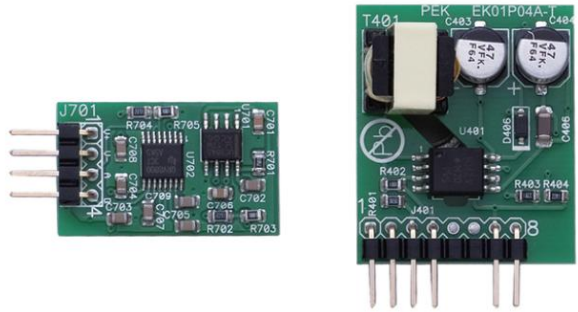
Figure 1.4 Flyback Auxiliary Power Module



Motor Power and Switch Driver Modules

- With one set of 12V isolated power, this module can provides multiple groups of isolated power, addressing the issue of complicated multiple groups of isolated motor powers validly.
- Driver module offers driving power of high frequency and current (2A) with the protection circuit equipped with Miller effect to prevent from false actions by accident.

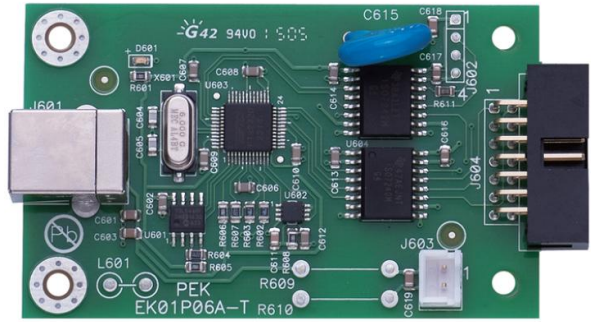
Figure 1.5 Motor Power and Switch Driver Modules



JTAG Burning Module

It offers isolated protection burning to be free from computer burnout during the experimental process due to lack of proper insulation.

Figure 1.6
JTAG Burning
Module



The Goal of Experiment

The teaching aid proceeds to query-oriented learning on the basis of circuit analysis, design, simulation, experiment, etc., and designs electric circuit and controller quantitatively based on the coverter specification. Furthermore, it facilitates readers to have profound understanding of relevant technology of Buck DC-DC Converter, via PSIM simulation verification, SimCoder programming process, therefore developing the following capabilities for readers.

1. The capability of analysis and design on power converter.
2. PSIM circuit simulating capability.
3. The design capability for controller of power converter.
4. DSP digital control technology (complete programming via SimCoder)
5. The layout and integration of hardware and firmware
6. The capability for circuit production and verification step by step

The Description on Chapters

See the chaper arrangements as follows

Brief	Briefly describes the circuit setup, experimental method and experimental purpose of the teaching aid. It also explains the contents of each chapter.
PSIM Brief	Briefly introduces the setup and functions of PSIM to help user realize the working contents of PISM that is able to assist converter to analyze and design circuit.
Introduction on hardware and equipment of teaching aid	Thoroughly introduces the working principle of each circuit and way to operate the equipment of the teaching aid.
Experiment 1 Pulse Width Modulation	Learns the theory of PWM, the conduction mode of Buck DC-DC module, the measurement of open-loop voltage and current, the pin setup of TI F28335 DSP IC, the PWM of DSP and A/D modules setting, the method of monitoring DSP internal signal via RS232, etc.
Experiment 2 Voltage Mode Control	Realizes the derivation method for small-signal module of Buck converter, the method of bode plot scanning by AC sweep, the design of voltage loop controller, the hardware layout and SimCoder programming, etc.
Experiment 3 Current Mode Control	Understands the method of average current mode control for Buck converter including model derivation of current and voltage loop, controller design, hardware layout and SimCoder programming, etc.

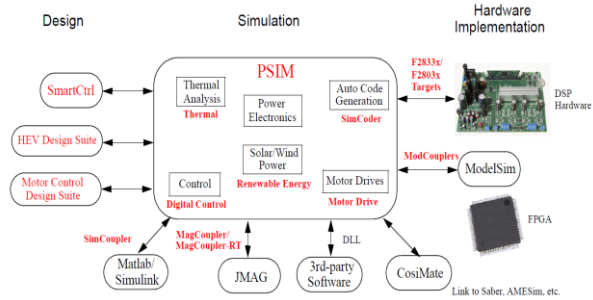
Experiment 4 Photovoltaics (PV) Module Max. Power Point Tracking (MPPT) Control	Learns the PV MPPT Control covering the pertube and observe method, incremental conductance MPPT control, hardware layout and the programming of control software.
Experiment 5 PV Charger	Realizes the control method of PV charger including the control of battery 3-level charging, the combination of MPPT control and charge control, hardware layout and the programming of control software.

PSIM Introduction

PSIM, the simulating software specifically designed for diversified systems of electric and electronic, motor-driven as well power converter, has the following features: full functions, intact components, fast and precise simulation, user-friendly interface, etc. It is the most popular teaching and researching software in the international academic community and related industry. Therefore, this teaching aid, by adopting the software as platform, makes efforts in helping reader better sync with the international research and education.

PSIM, with abundantly all-directional features including simulation, design as well as hardware circuit realization, provides the functions as the figure 2.1 shown. In addition to the main frame that supplies simulation of electricity, electron and circuit, the following modules are included.

Figure 2.1 Simulation provided by PSIM



Motor Driver Module	It includes DC motor, brushless DC motor, squirrel-cage rotor, wound-rotor motor, permanent-magnet synchronous motor, synchronous motor, switched reluctance motor, various feedback circuit devices for speed, location and torque, different mechanical loads and drive source devices that can be utilized as various motors and generators for simultation in application systems.
Digital Control Module	It includes several discrete components like zero-order hold, z-domain transfer function, digital filter, quantization blocks, etc, all of which are components that can execute digital control and analysis.
SimCoupler Module	It can be used to be the interface of PSIM and Simulink that empowers Co-sumulation for PSIM and Simulink, while allowing the user of Simulink to use the original technology. In addition, due to the advancements in simulating speed and convergence by adopting PSIM, it empowers the user of PSIM to make use of abundant Toolbox functions of Matlab via Simulink.
Thermal Module	It provides the module with actual power semiconductor component characteristics that is able to calculate the loss of power of semiconductor component for measuring temperature rise and reference on radiator mechanism design. User is able to construct power semiconductor component with Thermal in accordance with the data manual of actual component.
Renewable Energy Module	It contains Photovoltaics module, wind turbine and battery module.

SimCoder Module	It automatically converts control circuit into C program, and executes burning, via TI Composer, for DSP chip. Also, it offers a platform for interaction between hardware and firmware engineers through PSIM to build a specific field of closely tight cooperation.
F2833X Target	It contains the element database of TI DSP F2833X, which automatically generates program for burning F2833X.
F2803X Target	It contains the element database of TI DSP F2803X, which automatically generates program for burning F2803X.
MagCoupler Module	It offers the interface for PSIM and magnetic circuit analysis software JMAG and further links the above 2 for Co-simulation.
MagCoupler-RT Module	It provides link of data files for PSIM and magnetic circuit analysis software JMAG.
MagCoupler Module	It offers the interface of PSIM and ModelSim and further links the 2 for Co-simulation. 2 versions are available: ModCoupler-VHDL supporting VHDL program and ModCoupler-Verilog supporting Verilog program.
HEV Design Suite	It has some templates providing assistant design for powertrain system of HEV.
Motor Control Design Suite	It has some templates providing assistant design for induction motor, linear and non-linear permanent-magnet synchronous motor actuator.

In addition, PSIM offers user link with CosiMate, through which co-simulation can be realized with various software including Matlab/Simulink, ModelSim, Saber (from Synopsys), Easy5 and Adams (from MSCSoftware), Inventor (from Autodesk), AMESim (from LMS), GT-Power (from Gamma Technologies), etc. For more details, refer to the website link www.chiastek.com.

Teaching Aid Hardware

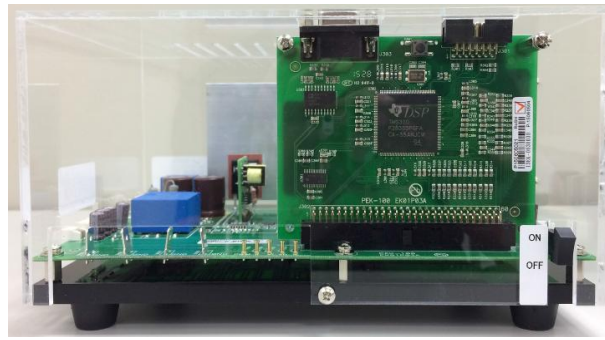
The teaching aid is a buck converter and the input device is GW PSW 160-7.2 360W with the input voltage ranging from 30V to 70V. The output devices are GW PEL-2004 and PEL-2040. Also, the GW GDS-2304A is the main oscilloscope. The following chapter will dive into the details of the mentioned devices profoundly.

Power Circuit

The physical appearance of teaching aid is shown as the figure 3.1, and the circuit is shown as the figure 3.2. For safety concern, the input voltage is limited at 50V and output voltage is within 24V, respectively. There is a 10A fuse in the forefront of input terminal followed by two 100uF/250V input electrolytic capacitors in parallel, and a buck converter consisting of MOS, diode and inductor (365uH) follows behind, for which the later part will further elaborate. Also, three output electrolytic capacitors (100uF/250V) in parallel are in the rear side and the circuit finally connects to the output terminal.

Figure 3.1

Buck DC-DC Converter Experiment Module



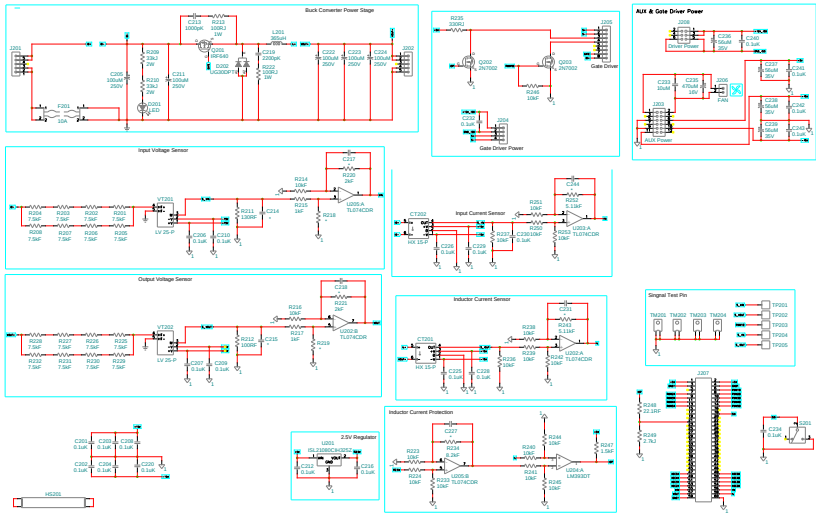


Figure 3.2 Buck DC-DC Converter Circuit Diagram

In the control and feedback circuit, the four parameters (input voltage (V_{IN}), output voltage (V_0), input current (I_{IN}) and output current (I_0) will be sampled before sent to DSP. The sample process before sent to DSP will be further illustrated in-depth in the following section.

1. The sample process of input voltage is excerpted as the figure 3.2 shown. Refer to the figure 3.3, the input voltage, after routing 8 resistors and attenuating by 1/15k times, is sent to the sampled IC with model name LEM LV 25-P. The IC magnifies the voltage by 2.5 times followed by timing 100Ω to produce the V_{IN} signal. It will be then sent to DSP after passing through the OP magnifier with the amplification of 1.44 times. The sampled attenuated ratio is shown as the figure

3.1. $$Gain = \frac{1}{15k} \times 2.5 \times 100 \times 1.44 = 0.024 \quad (3.1)$$

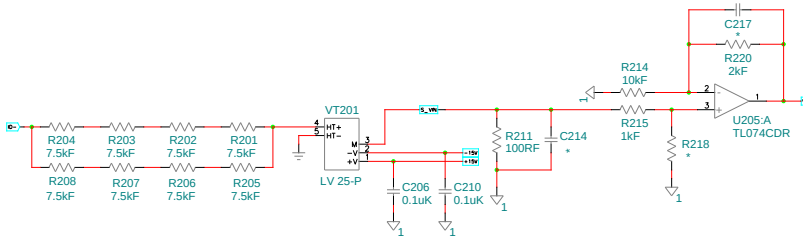


Figure 3.3 Input voltage sampled circuit

2. The sample process of output voltage is excerpted as the figure 3.2 shown. Refer to the figure 3.4, the output voltage, after routing 8 resistors and attenuating by 1/15k times, is sent to the sampled IC with model name LEM LV 25-P. The IC magnifies the voltage by 2.5 times followed by timing 100Ω to obtain the V_0 signal. It will be then sent to DSP after passing through the OP magnifier with the amplification of 1.44 times. The sampled attenuated ratio is shown as the figure 3.2.

$$Gain = \frac{1}{15k} \times 2.5 \times 100 \times 1.44 = 0.024 \qquad (3.2)$$

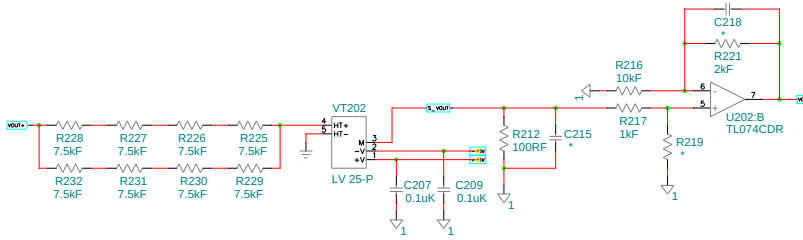


Figure 3.4 output voltage sampled circuit

3. The sample process of input current is excerpted as the figure 3.2 shown. Refer to the figure 3.5, the input current passes through the current sensor IC LEM HX 15-P with the conversion ratio 2.67×10^{-5} times. It will be then multiplied by 10kΩ followed by routing through the OP magnifier with the amplification of 1.125 to be sent to DSP. The sampled attenuated ratio is shown as the figure 3.3. $Gain = (2.67\times10^{-5})\times10k\times1.125 = 0.3$ (3.3)

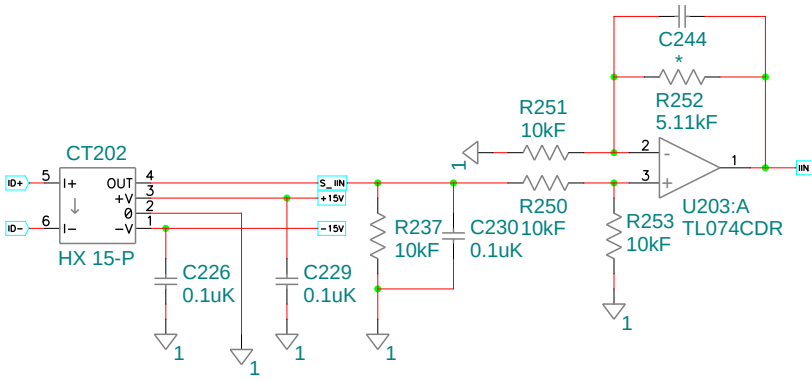


Figure 3.5 input current sampled circuit

4. The sample process of inductance current is excerpted as the figure 3.2 shown. Refer to the figure 3.6, the inductance capacitance passes through the current sensor IC LEM HX 15-P with the conversion ratio 2.67×10^{-5} times. It will be then multiplied by 10kΩ followed by routing through the OP magnifier with the amplification of 1.125 to be sent to DSP. The sampled attenuated ratio is shown as the figure 3.4.

$Gain = (2.67\times10^{-5})\times10k\times1.125 = 0.3$ (3.4)

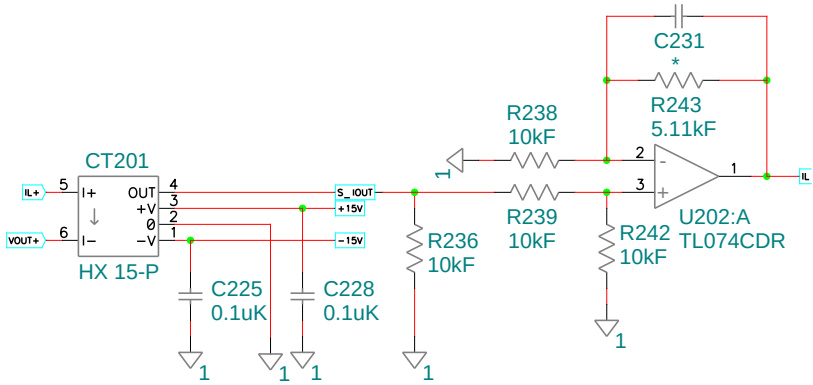


Figure 3.6 inductance current sampled circuit

In general, hardware circuit has the built-in OC (Over Current) Protection design with the normality of high level. Once current is beyond the limit, output will switch to low level to trigger the protection mechanism which forces converter to stop operation at once in case of damage. Refer to the figure 3.7 for the circuit.

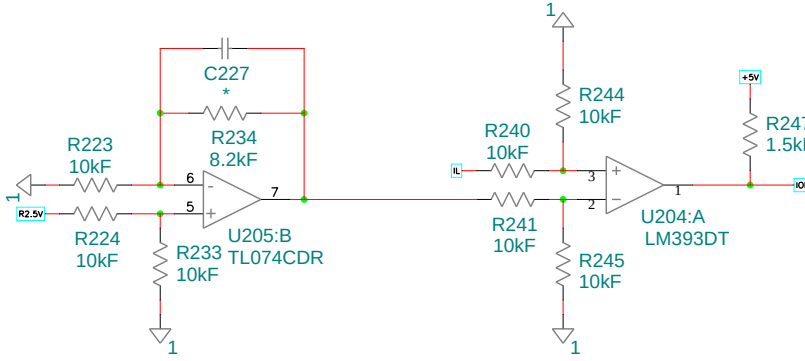


Figure 3.7 Over Current Protection (OCP) circuit

Buck DC-DC Converter teaching aid provides the following test points for users to measure:

1. DSP sends out PWM followed by drive circuit to drive MOS. The PWM signal can be measured from the measuring point.

2. Input voltage (V_{IN}), after routing 8 resistors and attenuating by 1/15k times, is sent to the sampled IC. The IC magnifies the voltage by 2.5 times followed by timing 100Ω to generate the exactly measuring value of measuring point. The attenuated ratio is shown as the figure 3.5.

$$Gain = \frac{1}{15k} \times 2.5 \times 100 = 1.67 \times 10^{-2} \quad (3.5)$$

3. Inductance current (V_0), after routing 8 resistors and attenuating by 1/15k times, is sent to the sampled IC. The IC magnifies the voltage by 2.5 times followed by timing 100Ω to generate the exactly measuring value of measuring point. The attenuated ratio is shown as the figure 3.6.

$$Gain = \frac{1}{15k} \times 2.5 \times 100 = 1.67 \times 10^{-2} \quad (3.6)$$

4. Output current (I_{IN}) passes through the current sensor with the conversion ratio 2.67×10^{-5} times. It will be then multiplied by 10kΩ to generate the exactly measuring value of measuring point. The attenuated ratio is shown as the figure 3.7.

$$Gain = (2.67 \times 10^{-5}) \times 10k = 0.267 \quad (3.7)$$

5. Output voltage (I_0) passes through the current sensor with the conversion ratio 2.67×10^{-5} times. It will be then multiplied by 10kΩ to generate the exactly measuring value of measuring point. The attenuated ratio is shown as the figure 3.8.

$$Gain = (2.67 \times 10^{-5}) \times 10k = 0.267 \quad (3.8)$$

DSP Control Circuit

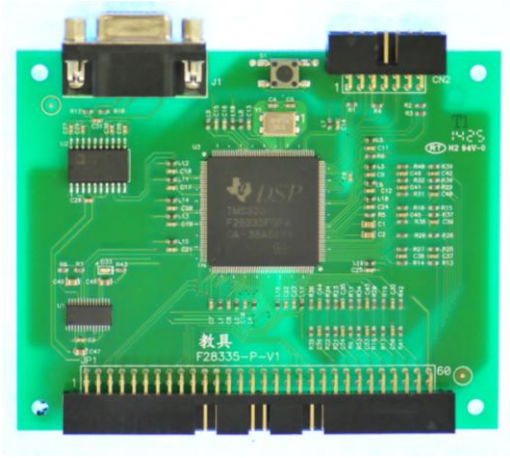
DSP control circuit is the hardware based on the TI TMS320F28335 (check figure 3.8 and 3.9 for the circuit diagram) to supply, via dual output regulator IC, 3.3V, the 28335 IC working power, and 1.8V. Before sent into DSP, the signal passes through the diode clamp circuit to ensure the voltage sent to IC is within 0 ~ 3V in case of damage to DSP. Through the isolated RS232 interface, it is available to sent DSP internal signal back to the oscilloscope of PSIM for observation. The output definitions of each pin on control panel are well explained in the table below.

	Pin		
+5V in	1	2	+5V in
GND	3	4	GND
GPIO-00 / EPWM-1A	5	6	GPIO-01 / EPWM-1B / MFSR-B
GPIO-02 / EPWM-2A	7	8	GPIO-03 / EPWM-2B / MCLKR-B
GPIO-04 / EPWM-3A	9	10	GPIO-05 / EPWM-3B / MFSR-A / ECAP-1
GPIO-06 / EPWM-4A / SYNCI / SYNCO	11	12	GPIO-07 / EPWM-4B / MCLKR-A / ECAP-2
GPIO-08 / EPWM-5A / CANTX-B / ADCSOC-A	13	14	GPIO-09 / EPWM-5B / SCITX-B / ECAP-3
GPIO-10 / EPWM-6A / CANRX-B / ADCSOC-B	15	16	GPIO-11 / EPWM-6B / SCIRX-B / ECAP-4
GPIO-48 / ECAP5 / XD31 (EMIF)	17	18	GPIO-49 / ECAP6 / XD30 (EMIF)
GPIO-50	19	20	GPIO-51
GPIO-12 / TZ1n / CANTX-B / MDX-B	21	22	GPIO-13 / TZ2n / CANRX-B / MDR-B
GPIO-15 / TZ4n / SCIRX-B / MFSX-B	23	24	GPIO-14 / TZ3n / SCITX-B / MCLKX-B
GPIO-24 / ECAP1 / EQEPA-2 / MDX-B	25	26	GPIO-25 / ECAP2 / EQEPB-2 / MDR-B
GPIO-26 / ECAP3 / EQEPI-2 / MCLKX-B	27	28	GPIO-27 / ECAP4 / EQEPS-2 / MFSX-B
GPIO-16 / SPISIMO-A /	29	30	GPIO-17 / SPISOMI-A / CANRX-

CANTX-B / TZ-5			B / TZ-6
GPIO-18 / SPICLK-A / SCITX-B	31	32	GPIO-19 / SPISTE-A / SCIRX-B
GPIO-20 / EQEP1A / MDX-A / CANTX-B	33	34	GPIO-21/ EQEP1B/ MDR-A/ CANRX-B
GPIO-22 / EQEP1S / MCLKX-A / SCITX-B	35	36	GPIO-23/ EQEP1I/ MFSX-A / SCIRX-B
GPIO-28 / SCIRX-A / -- / TZ5	37	38	GPIO-29 / SCITX-A / -- / TZ6
GPIO-30 / CANRX-A	39	40	GPIO-31 / CANTX-A
GPIO-32 / I2CSDA / SYNCI / ADCSOCA	41	42	GPIO-33 / I2CSCL / SYNCO / ADCSOCB
ADCIN-B7	43	44	ADCIN-A7
ADCIN-B6	45	46	ADCIN-A6
ADCIN-B5	47	48	ADCIN-A5
ADCIN-B4	49	50	ADCIN-A4
ADCIN-B3	51	52	ADCIN-A3
ADCIN-B2	53	54	ADCIN-A2
ADCIN-B1	55	56	ADCIN-A1
ADCIN-B0	57	58	ADCIN-A0
GND	59	60	GND

Figure 3.8

DSP control circuit



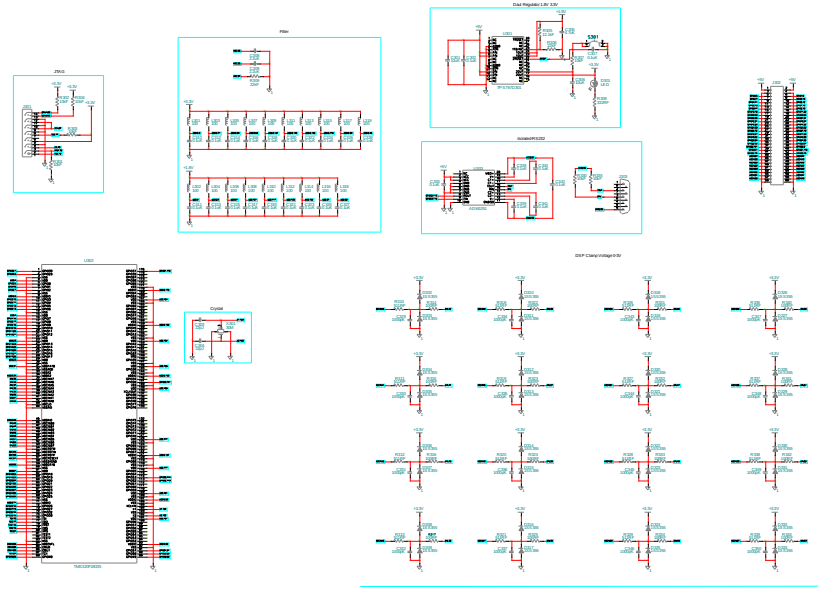


Figure 3.9 F28335 circuit diagram

Auxiliary Power

Bsed on the layout design of Flyback, this module has input voltage from 100 ~ 250V, and 3 groups of isolated output power, which is (1)12V, (2)12V, 5V (3)15V, -15V repectively. Refer to the figure 3.10 for physical appearance and figure 3.11 for circuit diagram.

Figure 3.10
Auxiliary power

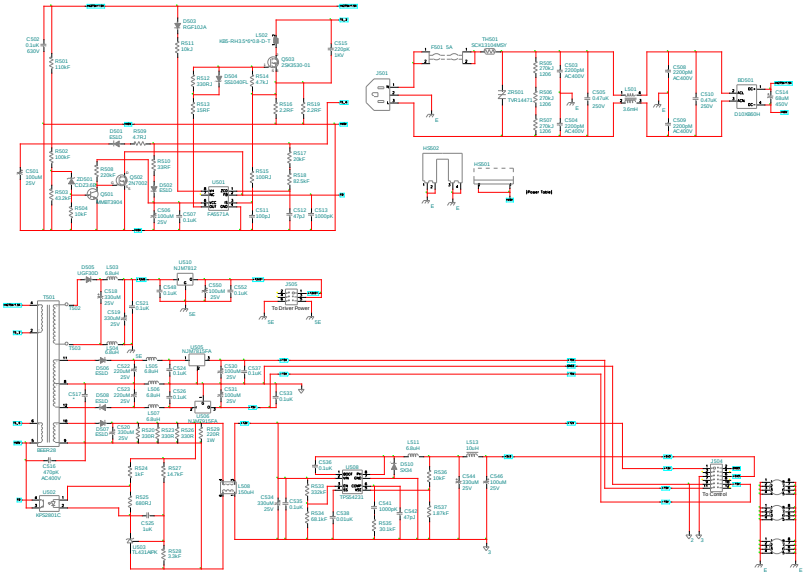
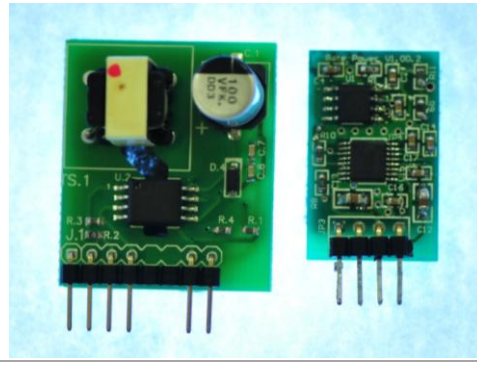


Figure 3.11 Auxiliary power circuit

Drive Circuit

Drive power module, which consists of Gate Driver board and Gate Driver Power board, provides multiple isolated powers. Refer to the figure 3.12 for Gate Driver (left) and Gate Driver Power (right). Also refer to the figures 3.13 and 3.14 for circuit diagrams. Inputting the 12V voltage to Gate Driver Power generates the output of ±12V square wave. The ±12V square wave along with the PWM signal generated by DSP, via the input of Gate Driver, will output the signal of drive MOS. Gate Driver meets the objective of isolation through inverter and optocoupler driver IC.

Figure 3.12 Circuit drive circuit module



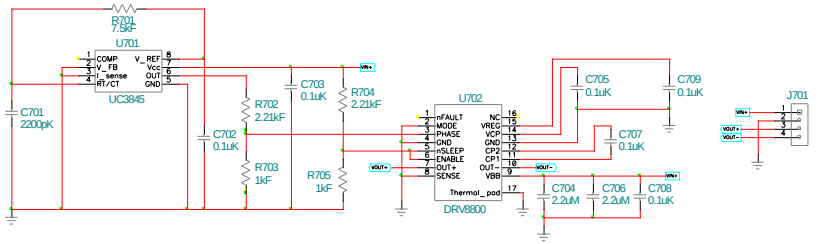


Figure 3.13 Gate Driver Power circuit diagram

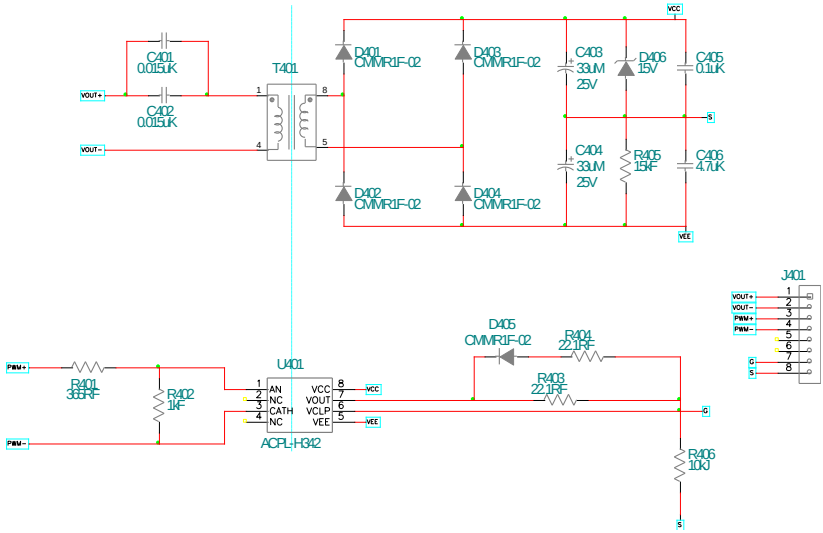


Figure 3.14 Gate Driver circuit diagram

JTAG Burning Circuit

The module helps burning program from PC to DSP chip. Refer to the figure 3.15 for hardware circuit and 3.16 for the circuit diagram. Connect USB to PC, and JTAG to DSP port individually.

Figure 3.15 USB_JTAG burning circuit

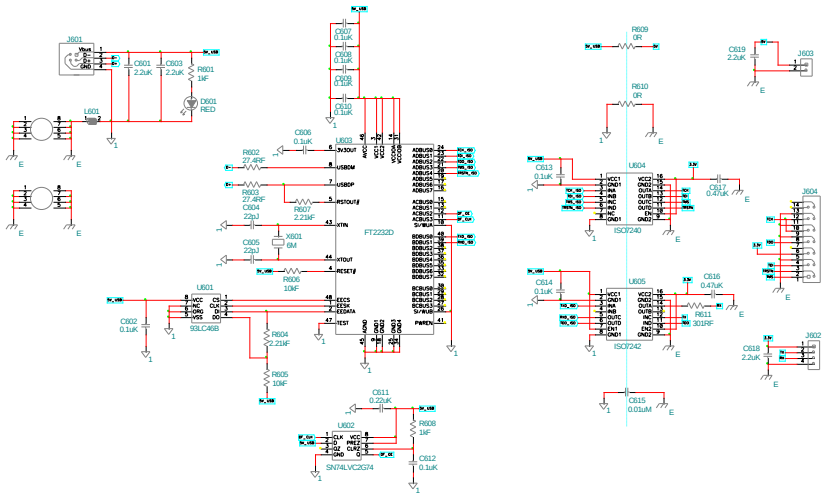


Figure 3.16 USB_JTAG circuit

Experiment 1 – Pulse Width Modulation (PWM)

The purpose of experiment

- Learn the principle of switch for PWM
- Work mode of Buck
- Measurement for open-loop voltage and current
- TI F28335 DSP IC pin setup
- Module setting for PWM and A/D module of DSP
- Method of monitoring DSP internal signal via RS232
- Familiarize the hardware circuit operation of this experiment

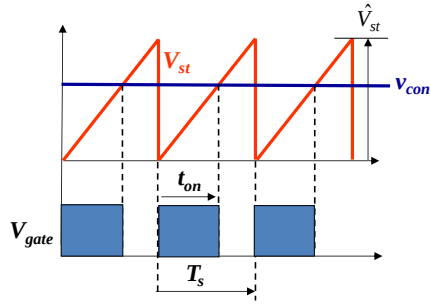
The principle of experiment

The principle of PWM (Pulse Width Modulation)

PWM is the most typical way for switchable converter to convert control signal to switch ON/OFF trigger signal. As the figure 4.1 shown, sawtooth wave frequency (f_s) is the change frequency of switch, whilst the reciprocal of change frequency is named change cycle (T_s=1/f_s). The ratio between switch conduction time (T_{on}) and change cycle (T_s) is called D, duty ratio or duty cycle. The relation between D and PWM control voltage V_{con} and sawtooth wave V_{st} is as the following:

$$D = \frac{t_{on}}{T_S} = \frac{v_{con}}{\hat{V}_{st}} \quad (4.1)$$

Figure 4.1 PWM waveform



From the aforementioned, sawtooth wave, of which $\hat{V}_{st}$ is the amplitude (peak to peak), is generally a constant frequency. In order to, however, raise efficiency for light load, and also reduce wastage for no-load, several converters lower down the change frequency per varied loads so as to greatly cut down the major lose from consuming and switching under light load. In addition, to mitigate the issue of EMI, the control IC, by and large, makes "Jitter" in constant frequency; that is, the f_d of change frequency, f_s $\pm f_d$, will be the range of jitter. By doing so, the switch energy will be, instead of concentration in one frequency, divided into one

frequency band. The jitter, f_d, is generally far lower than switch frequency. For example, jitter of the converter of 65kHz is within the range of few kHz, e.g., 5kHz, and the cycle of sweep is within the range of several ms.

The influence of switching frequency

Swithcing frequency is the basis of characteristics of converter in that it determines the specifics of converter like dimension, weight, response speed and efficiency. The influence to dimension by switching frequency is illustrated in the figure 4.2.

When switch is conducted and inductance current i_L is continuous conduction mode, i.e., i_L>0, the voltage V_{oi} is the input voltage V_d and inductance current starts circulation. When switch is off, inductance current will be conducted through diode and the voltage V_{oi} will be zero. Therefore, the voltage V_{oi} within the figure 4.2 (b) is a square wave identical to the duty cycle.

The cyclic waveform V_{oi} can be resolved, via Fourier Series, to both DC basic wave, i.e., switch frequency, and harmonic of multiples to switch frequency. See the figure 4.2 (b) for the spectrum. LC plays the role of low-pass filter here and the transfer function of output voltage, V_o and V_{oi}, is as the following:

$$H(s)=\frac{V_o(s)}{V_{oi}(s)}=\frac{R//\frac{1}{sC}}{sL+(R//\frac{1}{SC})}=\frac{1}{s^2+R/Ls+1/LC} \qquad (4.2)$$

Refer to the figure 4.2 (b) for the bode plot of LC low-pass filter, of which the cutoff frequency, f_c =($1/(2\pi\sqrt{LC})$), is far lower than switch frequency. After V_{oi} passes through LC low-pass filter, in addition to DC part that is attenuated by low-pass filter with the speed of -40dB/decade, the basic wave and harmonics of V_o are neglected by vast majority and the waveform will be close to pure DC with bare ripples.

In the figure 4.2 (b), when switch frequency rises, the high frequency switch attenuates, whilst the cutoff frequency, fc, of LC rises. Hence, the values of L and C will be relatively reduced.

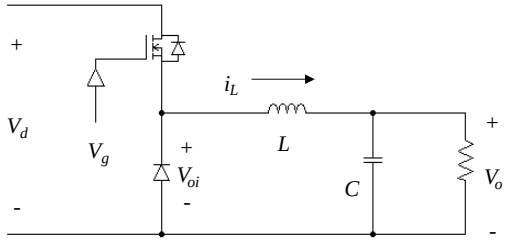
Due to the fact that LC passive components and power semiconductor units occupy the major parts of dimension of converter, LC value decreasing leads to scale down to dimension of L and C. Thus, to raise switch frequency is the most effective way to shrink the dimension of converter.

However, the ensuing issues of thermal and EMI are critical when raising switch frequency. The switch loss to power semiconductor units will elevate after switch frequency raise; in order to manage the thermal issue, it requires to enhace cooling area, e.g., heat sink enlargement, addintioal fan in place, for reducing thermal resistance.

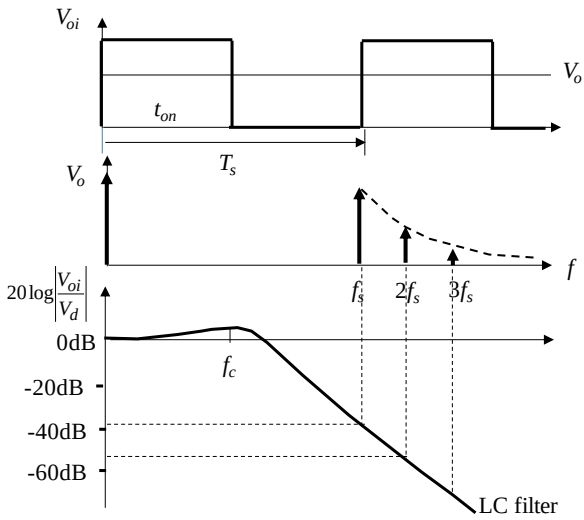
Consequently, there is a contradiction between raising switch frequency for shrinking size of passive components and effective dimension for heat dissipation. Secondly, switch frequency raise will pull up the level of *dv/dt* and *di/dt* in circuit, thus causing serious problems in dealing with deteriorated EMI issue within smaller dimension.

Figure 4.2

Explanation on relation between switch frequency and low-pass filter: (a) buck converter



(b) Waveform of V_{oi} and its spectrum



As the aforementioned, switch frequency raise comes with switch loss to power semiconductor units, and aggravates the wear and tear of magnetic components. Nevertheless, due to the less wastage of cord length by shrinked dimension along with adoption of components with less stray wastage, switch frequency raise has varied impacts to light load and heavy load, which depends on conditions per actual circuit.

In respect to the response speed of voltage and current, switch frequency raise, which reduces passive component value, is able to boost bandwidth controlled by open-loop system, also increasing the response speed of closed-loop system indirectly.

Working Principle of Buck Converter

Refer to the figure 4.3 for the relative parameters of buck converter circuit. The classification of output inductance current conduction can be divided into CCM (Continuous Conduction Mode), BCM (Boundary Conduction Mode) and DCM (Discontinuous Conduction Mode).

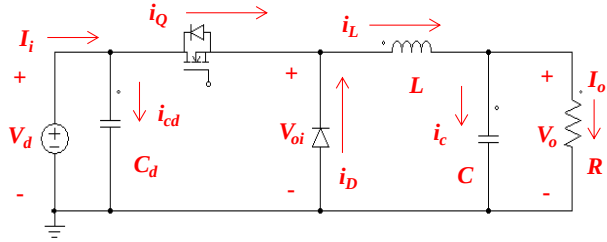


Figure 4.3 The relative parameters indications of buck converter circuit

(1) CCM (Continuous Conduction Mode)

CCM indicates that the waveforms of inductance current within a cycle are above 0 and the buck converter in CCM is divided into switch ON and switch OFF as the figure 4.4 shown. The corresponding working waveforms are illustrated as the figure 4.5. When switch (Q) is ON (state ①) and diode (D) is back bias voltage, energy will be transferred from input to output directly and the inductance current is as follows:

$$V_L = V_d - V_o \tag{4.3}$$

Because V_L value is greater than zero, the inductance current i_L will be rising (rising slope: $di_L/dt=V_L/L$) and i_L will rise from I_1 to I_2 during the cycle of switch conduction under steady state.

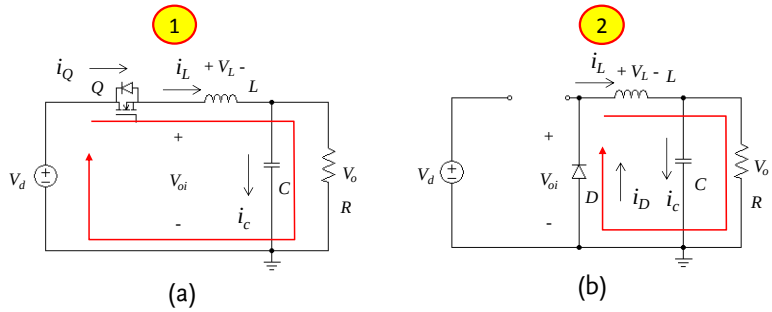


Figure 4.4 The working state of buck converter under CCM: (a) switch ON (b) switch OFF

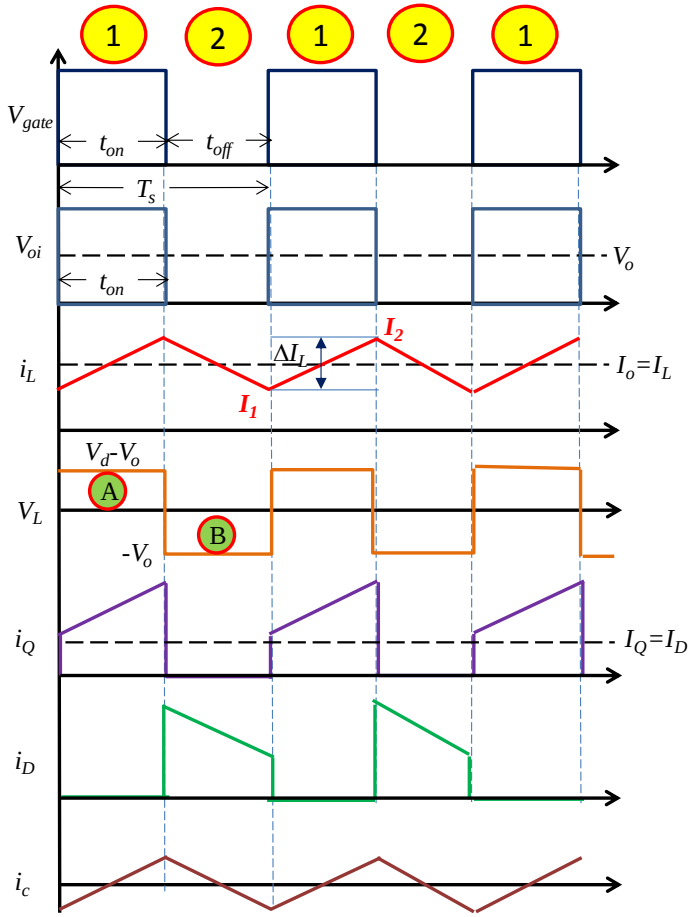


Figure 4.5 The working waveforms of buck converter under CCM

When switch is OFF (state ②) and diode is conducted, the energy of inductance will linger between diode and output, and the inductance voltage will be as follows:

$$V_L = -V_o \tag{4.4}$$

Because V_L value is smaller than zero, the inductance current i_L will be falling (falling slope: $di_L/dt = Vo/L$) and i_L will fall from I_2 to I_1 during the cycle of diode conduction under steady state. The B-H

(magnetic flux density – magnetic field strength) curve, which is equal to the expression of both Faraday's law and Ampère's law, of inductance is illustrated as the figure 2.6; for inductance, that N-turn circular coil passes through current I will result in magnetomotive force (mmf).

$$F = NI = Hl \tag{4.5}$$

From the above, l(m) is the magnetic path of inductance and the magnetic field strength (H) is directly proportional to, from the figure (4.5), the flowing current I(A). The unit of H, therefore, is present as (A/m). When switch of buck converter is ON (state ①), the inductance current will rise from I_1 to I_2 followed by routing along the bottom edge of B-H curve, of which work flow is as the figure 4.6 shown, to change from B_1 to B_2. When switch of buck converter is OFF (state ②), the inductance current will fall from I_2 to I_1 and its work in B-H curve will change from B_2 to B_1, through the top edge of B-H curve. The area between B-H curve and B axis is the current energy stored by inductance; therefore, a course of ON and OFF results in the loss of area, i.e., energy, by the work loop of B-H curve. This energy either multiplied by switch frequency (f_s) or divided by switch cycle (T_s) leads to a power loss, aka the "core loss", which deteriorates worse while switch frequency gets higher. We obtain the following via Faraday's law:

$$N\Delta BA = N\Delta\phi = \Delta\int Edt \tag{4.6}$$

Where A (m²) is the sectional area of core, and ϕ is the magnetic flux (Wb). In addition, B is magnetic flux density (Wb/m²=Tesla, 1 Tesla=10000Gauss), and E is the voltage (V) of inductance.

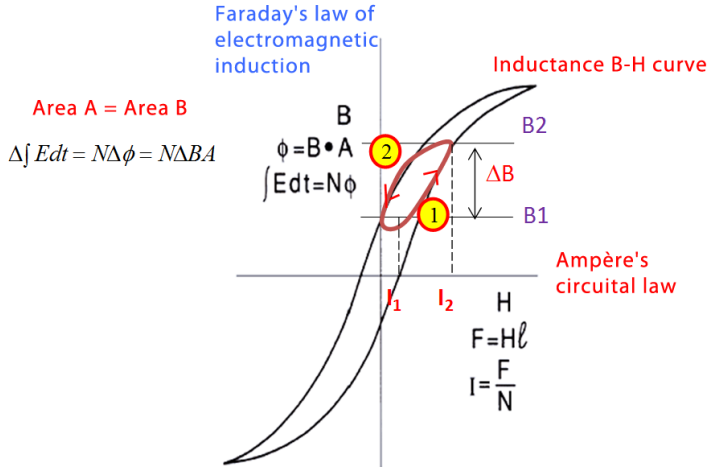


Figure 4.6 B-H curve and work loop of inductance

The ΔB (magnetic flux density change) of switch ON and OFF under steady state are identical. From (4.6), we may obtain as follows:

$$\Delta \int_{ON} Edt = \Delta \int_{OFF} Edt \tag{4.7}$$

The inductance voltage is equal to the integral of time during the course of switch ON and OFF; that is, the average of a cycle of inductance voltage is zero). Hence, from the waveforms of inductance voltage in the figure 4.6, area A = area B, which is called "voltage-second balance". We may further obtain as follows from the area A = area B in the figure 4.6:

$$(V_d - V_o)t_{on} = V_o t_{off} \tag{4.8}$$

The voltage conversion ratio of buck converter operated under CCM can be obtained as follows from the (4.8):

$$\frac{V_o}{V_d} = D \tag{4.9}$$

If the efficiency of buck converter is 100%, P_o=P_d; therefore:

$$V_o I_o = V_d I_i \tag{4.10}$$

And

$$I_o = I_L = \frac{V_o}{R} \tag{4.11}$$

Therefore

$$I_i = I_Q = DI_o \tag{4.12}$$

$$I_D = (1-D)I_o \tag{4.13}$$

We may obtain as follows from the waveform of the figure 4.6:

$$\Delta I_L = I_2 - I_1 = \frac{V_d - V_o}{L} t_{on} = \frac{V_d}{L}(1-D)DT_s = \frac{V_o}{L}(1-D)T_s \tag{4.14}$$

Definition: $\tau_L = \frac{L}{RT_s}$, we may infer the following from the figure 2.6:

$$I_1 = I_o(1 - \frac{1-D}{2\tau_L}) \tag{4.15}$$

$$I_2 = I_o(1 + \frac{1-D}{2\tau_L}) \tag{4.16}$$

$$i_{L(rms)} = I_o[1 + \frac{1}{12}(\frac{1-D}{\tau_L})^2]^{1/2} \tag{4.17}$$

$$i_{Q(rms)} = I_o\{D[1 + \frac{1}{12}(\frac{1-D}{\tau_L})^2]\}^{1/2} \tag{4.18}$$

$$i_{D(rms)} = I_o\{(1-D)[1 + \frac{1}{12}(\frac{1-D}{\tau_L})^2]\}^{1/2} \tag{4.19}$$

$$i_{c(rms)} = I_o \frac{(1-D)}{\sqrt{12}\tau_L} \tag{4.20}$$

$$i_{C_d(rms)} = I_o\{D[(1-D) + \frac{1}{12}(\frac{1-D}{\tau_L})^2]\}^{1/2} \tag{4.21}$$

The above equations can be used to calculate current of component, which can be the basis for component selection.

(2) BCM (Boundary Conduction Mode)

The average (I_L) of inductance current from buck converter is equal to load current ($Io=Vo/R$); when load current getting smaller which forces inductance current to be falling to zero within a course of cycle is called BCM, the inductance current will then be said boundary inductance current (I_{LB}), and the corresponding load current wil be called boundary current current (I_{OB}). The working waveform of BCM is shown as the figure 4.8. ILB meets the following under BCM:

$$I_{LB} = \frac{1}{2} i_{L,pk} = \frac{1}{2} \frac{(V_d - V_o)}{L} t_{on} = \frac{DT_s}{2L} (V_d - V_o) = I_{oB} \qquad (4.22)$$

The following content is divided in to 2 parts: the applications of V_d constant value and V_o constant value, respectively:

When V_d is constant value:

$$V_o = DV_d \qquad (4.23)$$

We may obtain the following by substituting (4.23) into (4.22):

$$I_{LB} = \frac{T_s V_d}{2L} D(1-D) \qquad (4.24)$$

Where the maximum value occurs when D = 0.5:

$$I_{LB,\max} = \frac{T_s V_d}{8L} \qquad (4.25)$$

Therefore, (4.24) can be rephrased as:

$$I_{LB} = 4 I_{LB,\max} D(1-D) \qquad (4.26)$$

When V_o is constant value:

$$V_d = V_o / D \qquad (4.27)$$

We may obtain the following by substituting (4.27) into (4.22):

$$I_{LB} = \frac{T_S V_o}{2L}(1-D) \tag{4.28}$$

Where the maximum value occurs when D = 0:

$$I_{LB,\max} = \frac{T_S V_o}{2L} \tag{4.29}$$

Therefore, (4.28) can be rephrased as:

$$I_{LB} = (1-D) I_{LB,\max} \tag{4.30}$$

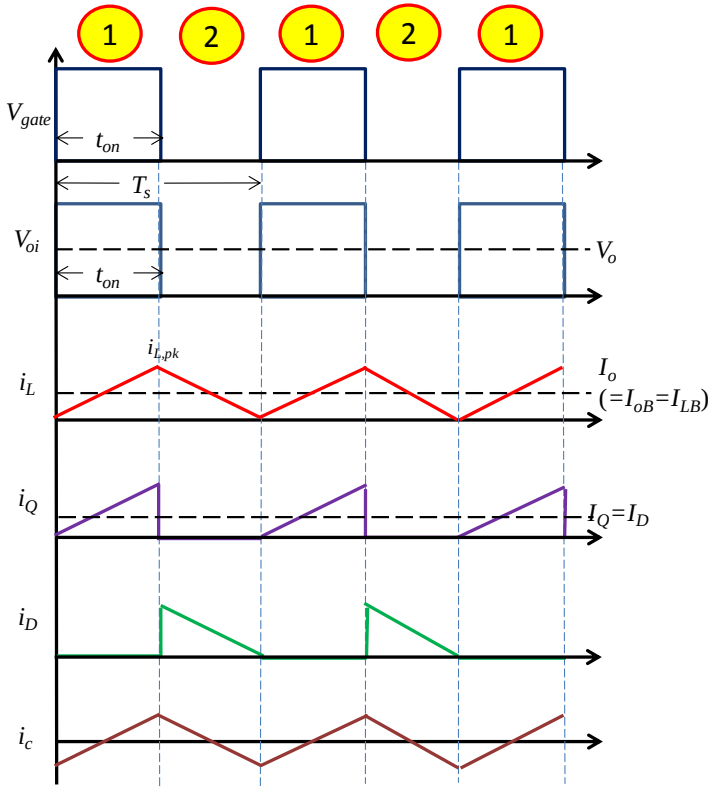


Figure 4.7 The working waveform of buck converter under BCM

(3) DCM (Discontinuous Conduction Mode)

When load current is lower than I_{LB}, the inductance current will enter DCM before falling to zero within a course of cycle when switch is off. The working waveform of DCM is shown as the figure 4.9. The inductance voltage vL needs to meet volt-seconds balance (area A=B):

$$(V_d - V_o)DT_s + (-V_o)\Delta T_s = 0 \tag{4.31}$$

We may obtain as follows after refresh:

$$\frac{V_o}{V_d} = \frac{D}{D+\Delta} \tag{4.32}$$

The peak value of inductance current is:

$$i_{L,pk} = \frac{V_o}{L}\Delta T_s \tag{4.33}$$

$$I_o = i_{L,pk}\frac{D+\Delta}{2} = \frac{V_o T_s}{2L}(D+\Delta)\Delta = \frac{V_d T_s}{2L}D\Delta = 4I_{LB,\max}D\Delta \tag{4.34}$$

When V_d is constant value:

We may obtain the following by utilizing (4.25) and (4.34):

$$\Delta = \frac{I_o}{4I_{LB,\max}D} \tag{4.35}$$

We may obtain the following by refresh after substituting (4.35) into (4.32):

$$\frac{V_o}{V_d} = \frac{D^2}{D^2 + \frac{1}{4}(I_o / I_{LB,\max})} \tag{4.36}$$

We utilize the diagram of characteristics of buck converter based on (4.9), (4.36) and (4.36). Refer to the figure 4.10(a) for demonstration.

When V_o is constant value:

We may obtain by utilizing (4.29) and (4.34):

$$\Delta = (\frac{I_o}{I_{LB,\max}} \frac{V_d - V_o}{V_d})^{1/2} \quad (4.37)$$

We may obtain the following by refresh after substituting (4.37) into (4.32):

$$D = \frac{V_o}{V_d} (\frac{I_o / I_{LB,\max}}{1 - V_o / V_d})^{1/2} \quad (4.38)$$

We utilize the diagram of characteristics of buck converter based on (4.9), (4.30) and (4.38). Refer to the figure 4.10(b) for demonstration.

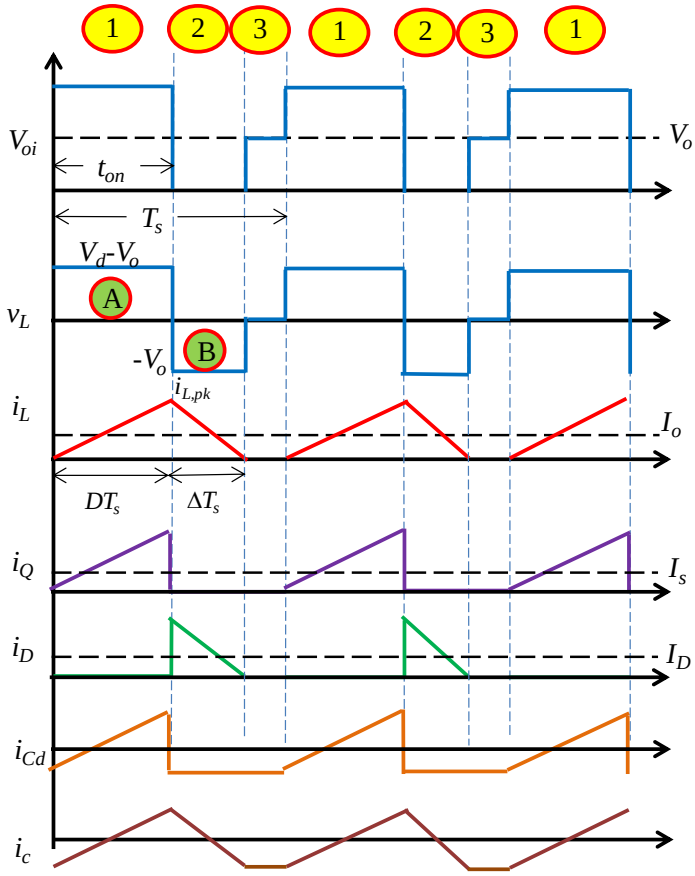
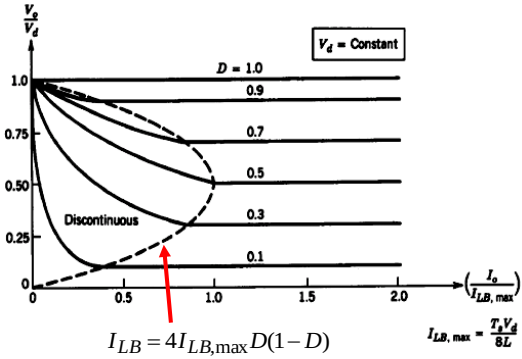
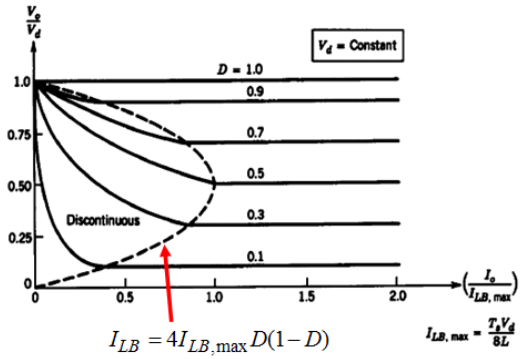


Figure 4.8 The working waveform of buck converter under DCM

Figure 4.9 The diagram of characteristics of buck converter:
(a) *Vd* is constant value



(b) *Vo* is constant value



The design of L and C

1. The inductance design

Method 1: conduction mode consideration

Design inductance by regarding the minimum current (I_o=I_{oB}) as the boundary condition so that load current will be higher than IoB and operate under CCM. It meets the following as the figure 4.10 shown:

$$2I_{oB} = i_{L,peak} = \frac{V_d - V_o}{L} T_{on} \tag{4.39}$$

When V_d is constant value,

We may obtain as follows from (4.39) when taking the change of duty cycle of output voltage change into account:

$$L_{\min} = \frac{T_s V_d}{2I_{oB}} [D(1-D)]_{\max} \tag{4.40}$$

When V_o is constant value,

We may obtain as follows from (4.39) when taking the change of duty cycle of input voltage change into account:

$$L_{\min} = \frac{T_s V_o}{2I_{oB}} (1 - D_{\min}) \tag{4.41}$$

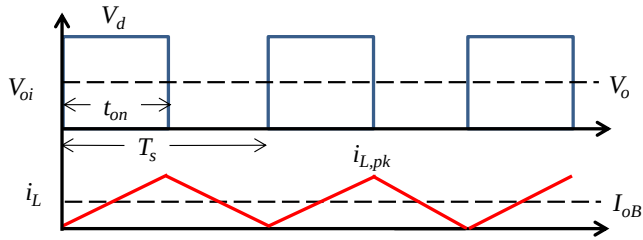


Figure 4.10 The inductance current waveform of buck converter under BCM

Method 2: inductance current ripple consideration

Define a specification, $\Delta I_L/I_{o,rated}$, of inductance current ripple, and obtain the inductance quantity meeting this specification. Refer to the figure 4.11 below, the inductance current ripple under CCM will be:

$$\Delta I_L = \frac{V_d - V_o}{L} t_{on} \tag{4.42}$$

When V_d is constant value,

We may obtain as follows from (4.42) when taking the change of duty cycle of output voltage change into account:

$$L_{\min} = \frac{T_s V_d}{2\Delta I_L} [D(1-D)]_{\max} \tag{4.43}$$

When V_o is constant value,

We may obtain as follows from (4.43) when taking the change of duty cycle of input voltage change into account:

$$L_{\min} = \frac{T_s V_o}{2\Delta I_L} (1 - D_{\min}) \tag{4.44}$$

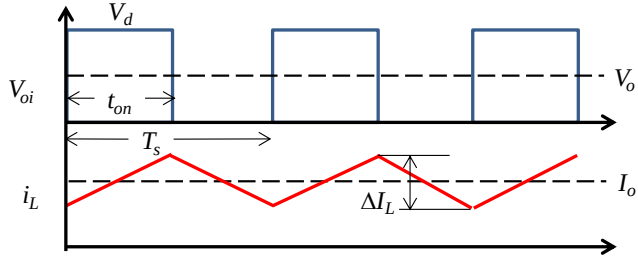


Figure 4.11 The inductance current ripple of buck converter under CCM

The two methods of inductance design above are equivalent. For instance, the specification of 20% inductance current ripple is equivalent to I_{oB}=10%$I_{o,rated}$.

2. Capacitance design

The factor one: output voltage ripple

The output capacitance ripple is resulted from inductance current ripple charging/discharging capacitance as the figure 4.12 shown. The ripple contains the ripple caused by capacitance charging/discharging itself and the ripple formed by capacitance current flowing through ESR (Equivalent Series Resistance).

$$\begin{aligned}\Delta V_o &= \Delta I_L R_e + \frac{\Delta Q}{C} \\ &= \Delta V_{o1} + \Delta V_{o2}\end{aligned} \tag{4.45}$$

If the ripple formed by ESR (Re) is the primary (ΔV_o=ΔV_{o1}) to this voltage ripple, it is required to first design capacitance by ESR followed by determining capacitance value by ESR.

$$R_e = \frac{\Delta V_o}{\Delta I_L} \quad \text{or} \quad R_e = \frac{\Delta V_o}{2I_{oB}} \tag{4.46}$$

$$C = \frac{(RC \text{ product of Capacitor})}{R_e} \tag{4.47}$$

In general, if electrolyptic capacitance is utilized, the ripple caused by ESR will be the primary to the voltage ripple. The typical electrolyptic capacitance (RC product) = 30×10^{-6} ~ 80×10^{-6}.

If, however, the utilized capacitance is low ESR material, the ripple resulted from capacitance charging/discharging itself will be the primary (ΔV_o=ΔV_{o2}) to the voltage ripple:

$$\begin{aligned}\Delta V_o &= \frac{\Delta Q}{C} = \frac{\frac{(\Delta I_L/2)(T_S/2)}{2}}{C} \\ &= \frac{\Delta I_L T_S}{8C} = \frac{V_o(1-D)T_S^2}{8LC}\end{aligned} \tag{4.48}$$

We may obtain the following by (4.48):

$$C == \frac{V_o(1-D_{\min})T_s^2}{8L\Delta V_o} \tag{4.49}$$

It requires to first define inductance value before design by (4.49).

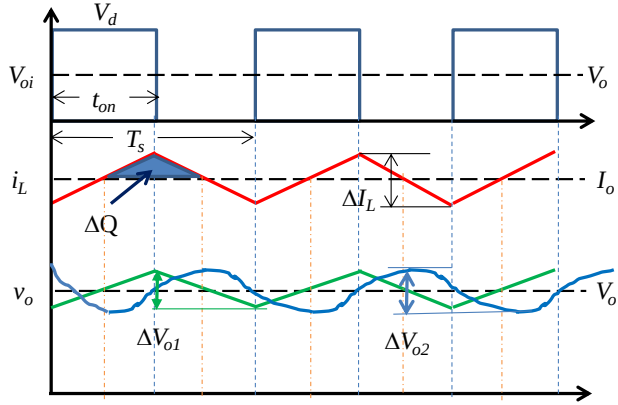


Figure 4.12 The voltage ripple of buck converter under CCM

The factor two: capacity of capacitor

When load changes accidentally and inductance current is Not able to catch up for replenish yet, load current will be provided by capacitor that results in transient fall of output voltage, or rise when load-reducing. Refer to the figure 4.13 shown. If voltage falls from V_{o1} to V_{o2} within the time period of Δt, it will meet as follows:

$$\Delta P_o = \frac{C(V_{o1}^2 - V_{o2}^2)}{2\Delta t} \tag{4.50}$$

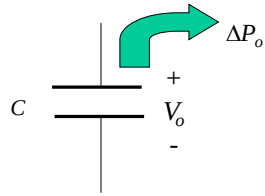
We may get the required capacitance quantity as follows via (4.50):

$$C = \frac{2\Delta P_o \Delta t}{V_{o1}^2 - V_{o2}^2} \tag{4.51}$$

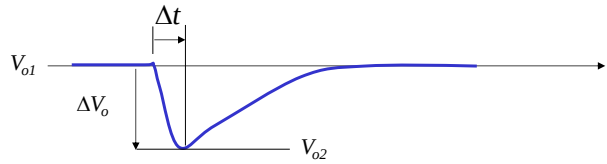
Generally, identical to the customizable specifications of ΔVo and Δt s in terms of design, ΔPo can be set by $0.9P_{o,max}$. It is necessary to use the maximum value of the capacitance value determined by the above voltage ripple specification and power performace as the

ultimate capacitance value. In general, capacitance value of the lower ESP capacitor is decided by the storage capacity of capacitor.

Figure 4.13 (a) When load rises accidentally and inductance current is Not able to catch up for replenish yet, load current will be provided by capacitor.



(b) Transient state waveform of capacitance voltage



Circuit Simulation

The circuit parameters of buck converter are as follows:

V_d=50V, V_{tri}=5V_{pp}/40kHz, L=365uH, C=300μF, R=24*24/10Ω

Open-loop control simulating circuit is shown as the figure 4.14, whereas the simulating result is shown as the figure 4.15.

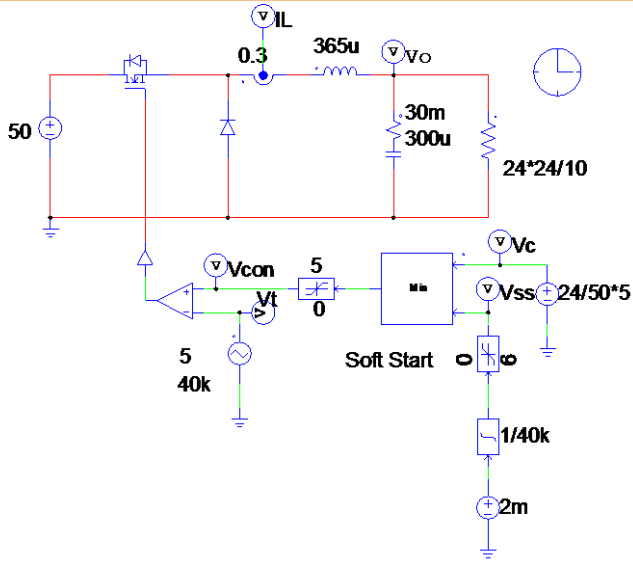


Figure 4.14 The simulating circuit utilizing unipolar voltage switching

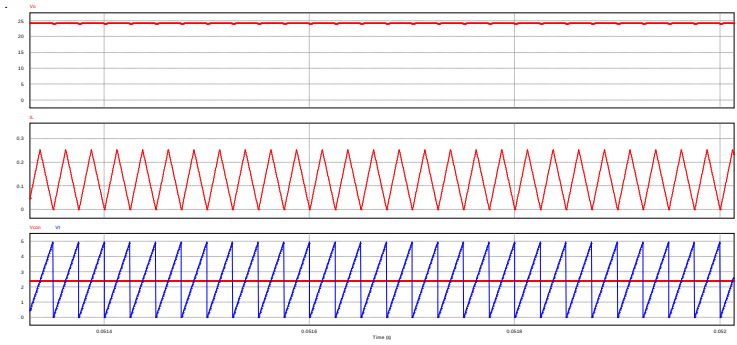


Figure 4.15 The result of simulation by utilizing unipolar voltage switching

SimCoder Program Layout

Based on the simulating circuit of analog unipolar voltage switching indicated in the figure 4.14, the SimCoder circuit layout of control circuit (figure 4.16) is realized by TI F28335, and the gain hardware setting of sense circuit is as follows:

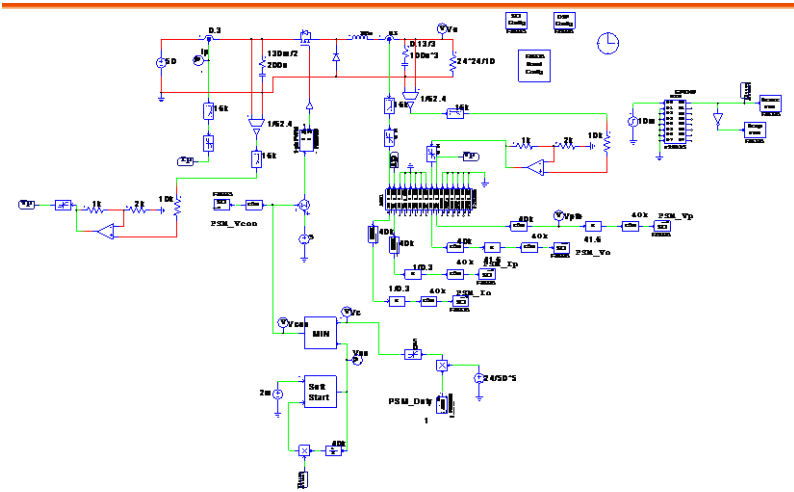
Current sense gain K_s=1/3.33

Voltage sense gain K_v=1/62.4

Sense signal of voltage/current has to pass through a limiter, which forces input voltage clamped at 0~3V, before entering the DSP A/D pin.

The above hardware circuit is merely for SimCoder simulation. Due to the fact that DSP of actual circuit only accpets 0~3V signal, the AC signal will be rising to 1.5V followed by 3V clamp to enter the A/D pin, which means DSP, originally 1.5V, will be regarded 0 to AC signal.

The setting of each component of SimCoder is as follows.



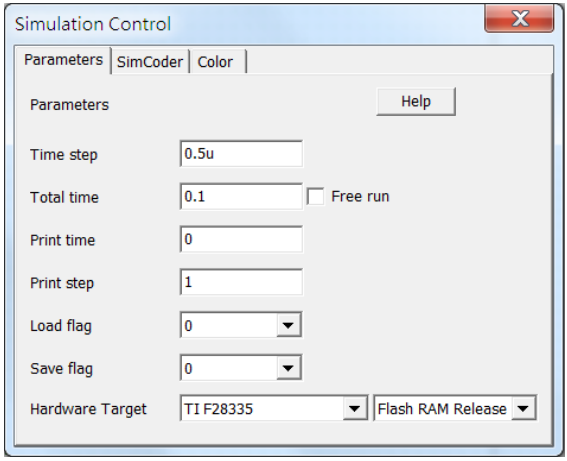
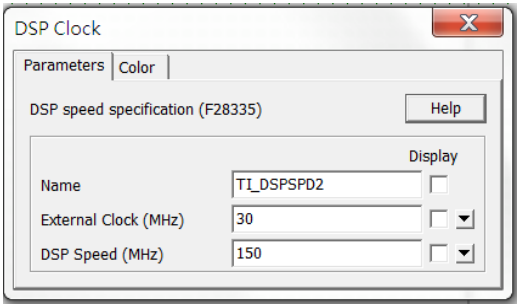


Figure 4.16 The SimCoder simulating circuit utilizing unipolar voltage switching

DSP Clock Setting

DSP Clock is available for external or built-in setting; external setting asks user to manuall modify parameters of External Clock (default=30MHz), whilst built-in setting requests DSP speed to be 150MHz. The experiment adopts the built-in setting.



28335 Hardware Config

The hardware setting of this experiment DSP F28335 requires tick for each cell within the following table.

- Use a set of PWM, PWM1(GPIO 0, GPIO 1).
- Use a set of DI (Digital Input，GPIO 49), and PWM can be activated via external circuit.
- When circuit is active, use a set of serial communication (SCI C, GPIO62, 63) to send signal to computer through RS232-USB to monitor system status.

GPIO 0	Digital Input	Digital Output	V	PWM		
GPIO 1	Digital Input	Digital Output	V	PWM	Capture	
GPIO 2	Digital Input	Digital Output		PWM		
GPIO 3	Digital Input	Digital Output		PWM	Capture	
GPIO 4	Digital Input	Digital Output		PWM		
GPIO 5	Digital Input	Digital Output		PWM	Capture	
GPIO 6	Digital Input	Digital Output		PWM		
GPIO 7	Digital Input	Digital Output		PWM	Capture	
GPIO 8	Digital Input	Digital Output		PWM		
GPIO 9	Digital Input	Digital Output		PWM	Capture	Serial Port
GPIO 10	Digital Input	Digital Output		PWM		
GPIO 11	Digital	Digital		PWM	Capture	Serial

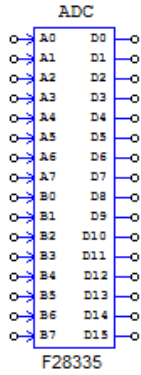
	Input	Output			Port
GPIO 12	Digital Input	Digital Output	Trip-Zone		
GPIO 13	Digital Input	Digital Output	Trip-Zone		
GPIO 14	Digital Input	Digital Output	Trip-Zone	Serial Port	
GPIO 15	Digital Input	Digital Output	Trip-Zone	Serial Port	
GPIO 16	Digital Input	Digital Output	Trip-Zone	SPI	
GPIO 17	Digital Input	Digital Output	Trip-Zone	SPI	
GPIO 18	Digital Input	Digital Output	Serial Port	SPI	
GPIO 19	Digital Input	Digital Output	Serial Port	SPI	
GPIO 20	Digital Input	Digital Output	Encoder		
GPIO 21	Digital Input	Digital Output	Encoder		
GPIO 22	Digital Input	Digital Output	Encoder	Serial Port	
GPIO 23	Digital Input	Digital Output	Encoder	Serial Port	
GPIO 24	Digital Input	Digital Output	PWM	Capture	Encoder
GPIO 25	Digital Input	Digital Output	PWM	Capture	Encoder
GPIO 26	Digital Input	Digital Output	PWM	Capture	Encoder
GPIO 27	Digital Input	Digital Output	PWM	Capture	Encoder
GPIO 28	Digital Input	Digital Output	Serial Port		
GPIO 29	Digital Input	Digital Output	Serial Port		
GPIO 30	Digital Input	Digital Output			
GPIO 31	Digital	Digital			

		Input	Output		
GPIO 32		Digital Input	Digital Output		
GPIO 33		Digital Input	Digital Output		
GPIO 34		Digital Input	Digital Output	PWM	Capture
GPIO 35		Digital Input	Digital Output	Serial Port	
GPIO 36		Digital Input	Digital Output	Serial Port	
GPIO 37		Digital Input	Digital Output	PWM	Capture
GPIO 38		Digital Input	Digital Output		
GPIO 39		Digital Input	Digital Output		
GPIO 40		Digital Input	Digital Output		
GPIO 41		Digital Input	Digital Output		
GPIO 42		Digital Input	Digital Output		
GPIO 43		Digital Input	Digital Output		
GPIO 44		Digital Input	Digital Output		
GPIO 45		Digital Input	Digital Output		
GPIO 46		Digital Input	Digital Output		
GPIO 47		Digital Input	Digital Output		
GPIO 48		Digital Input	Digital Output	PWM	Capture
GPIO 49	V	Digital Input	Digital Output	PWM	Capture
GPIO 50		Digital Input	Digital Output	Encoder	
GPIO 51		Digital	Digital	Encoder	

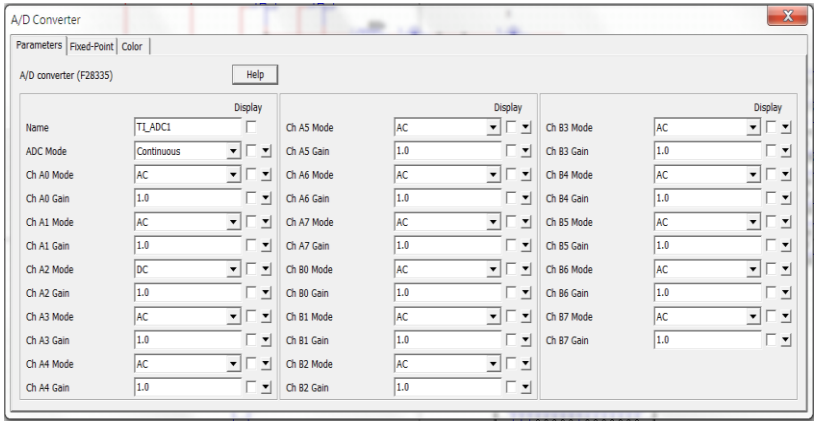
	Input	Output			
GPIO 52	Digital Input	Digital Output		Encoder	
GPIO 53	Digital Input	Digital Output		Encoder	
GPIO 54	Digital Input	Digital Output		SPI	
GPIO 55	Digital Input	Digital Output		SPI	
GPIO 56	Digital Input	Digital Output		SPI	
GPIO 57	Digital Input	Digital Output		SPI	
GPIO 58	Digital Input	Digital Output			
GPIO 59	Digital Input	Digital Output			
GPIO 60	Digital Input	Digital Output			
GPIO 61	Digital Input	Digital Output			
GPIO 62	Digital Input	Digital Output	V	Serial Port	
GPIO 63	Digital Input	Digital Output	V	Serial Port	
GPIO 64	Digital Input	Digital Output			
GPIO 65	Digital Input	Digital Output			
GPIO 66	Digital Input	Digital Output			
GPIO 67	Digital Input	Digital Output			
GPIO 68	Digital Input	Digital Output			
GPIO 69	Digital Input	Digital Output			
GPIO 70	Digital Input	Digital Output			
GPIO 71	Digital	Digital			

	Input	Output		
GPIO 72	Digital Input	Digital Output		
GPIO 73	Digital Input	Digital Output		
GPIO 74	Digital Input	Digital Output		
GPIO 75	Digital Input	Digital Output		
GPIO 76	Digital Input	Digital Output		
GPIO 77	Digital Input	Digital Output		
GPIO78	Digital Input	Digital Output		
GPIO 79	Digital Input	Digital Output		
GPIO 80	Digital Input	Digital Output		
GPIO 81	Digital Input	Digital Output		
GPIO 82	Digital Input	Digital Output		
GPIO 83	Digital Input	Digital Output		
GPIO 84	Digital Input	Digital Output		
GPIO 85	Digital Input	Digital Output		
GPIO 86	Digital Input	Digital Output		
GPIO 87	Digital Input	Digital Output		

AD Converter (ADC) Setting

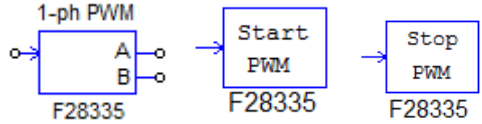


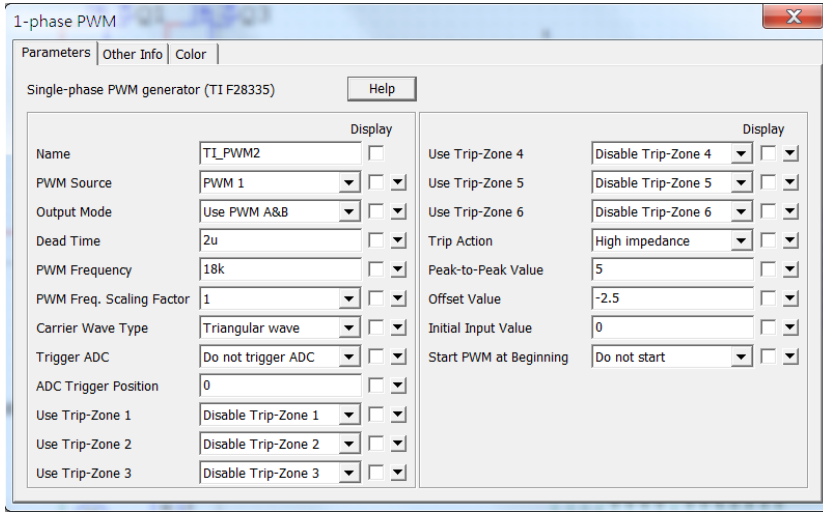
F28335 contains 16 groups of ADC, which can be divided into A0~A7 and B0~B7 channels, respectively. ADC module requires setting ADC sampling mode where Continuous sampling mode, input mode and Gain mode of each channel are necessary for setting. The experiement feedbacks 4 signals in total, which are load current (I_L, A0)), inductor current (I_0, A1)), input voltage (V_d, A2) and output voltage (V_0, B0), where only input voltage is defined as DC mode, whilst the rest 3 are AC mode. The gain of each ADC is set 1.



PWM Setting

The single-phase PWM adopts 40kHz trigangle wave with amplitude setting: Vp=5V, i.e., the triangle wave between -0V~+5V. The initial status of PWM is auto-deactivation; instead, it activates and stops via control of 2 modules: Start PWM and Stop PWM.

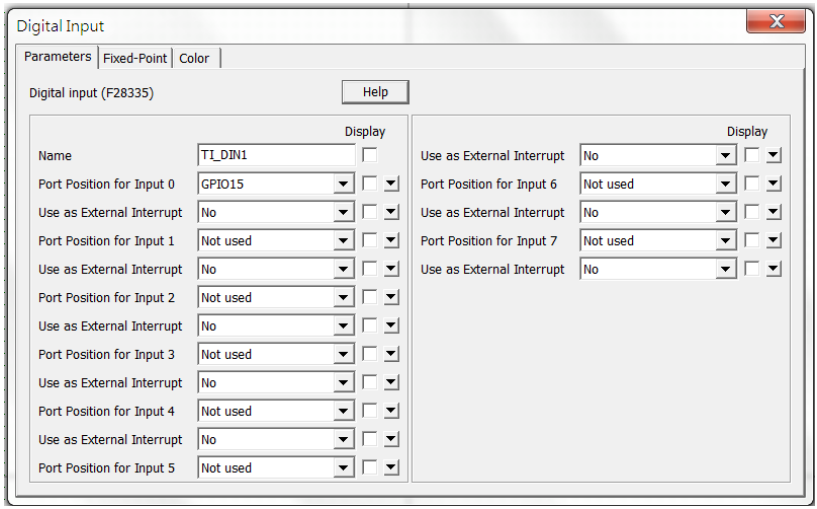




PWM

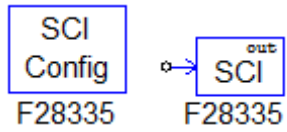
Digital Input Setting

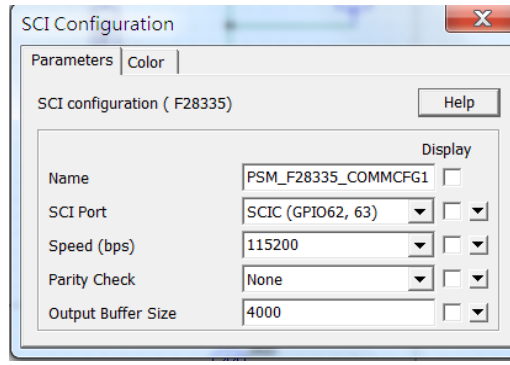
The experiment enables or disables PWM1 and PWM2 via DI (by GPIO 49). DI input signal is generated from DSP external signal.

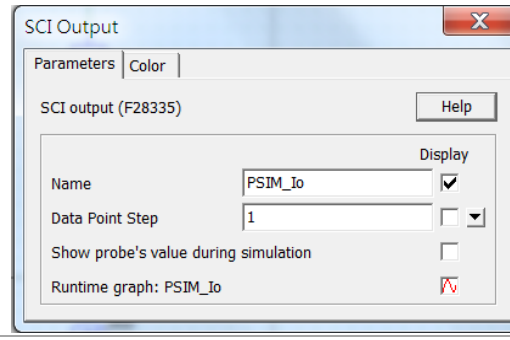


SCI Setting

The experiment send signal back to computer via SCI. The settings of 2 modules, SCI Config and SCI out, are as the following. The SCI communication speed is 115200(bps) without parity check and its buffer size is defined as 4000 points. SCI output, on the other hand, is set to send signal in every single point.

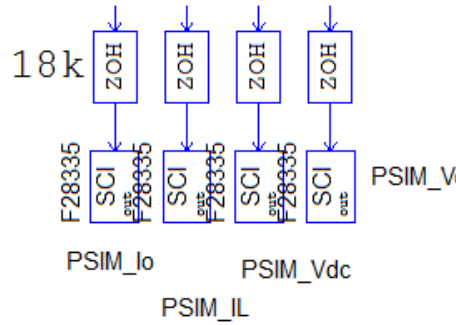






Note

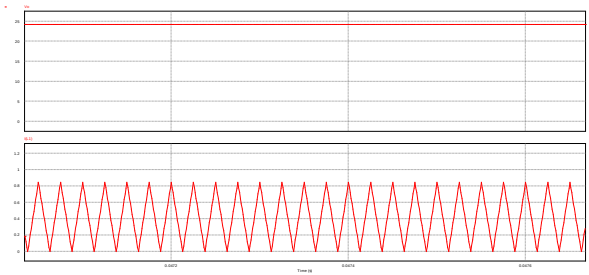
SCI out module must work with ZOH module, which is used to define breaking interval of SCI.



Simulating result of SimCoder circuit

Figure 4.17

Figure 4.16 The simulating result of SimCoder circuit



Code Autogeneration

Convert the SimCoder control circuit of the above inverter circuit into the C Code via Simulate => Generate Code under PSIM. PSIM will generate a subdirectory named aftered the simulating file in the same directory with the simulating circuit. The auto-generated Code along with the related files for next project of TI Code Composer will be collectively saved into the subsirectory.

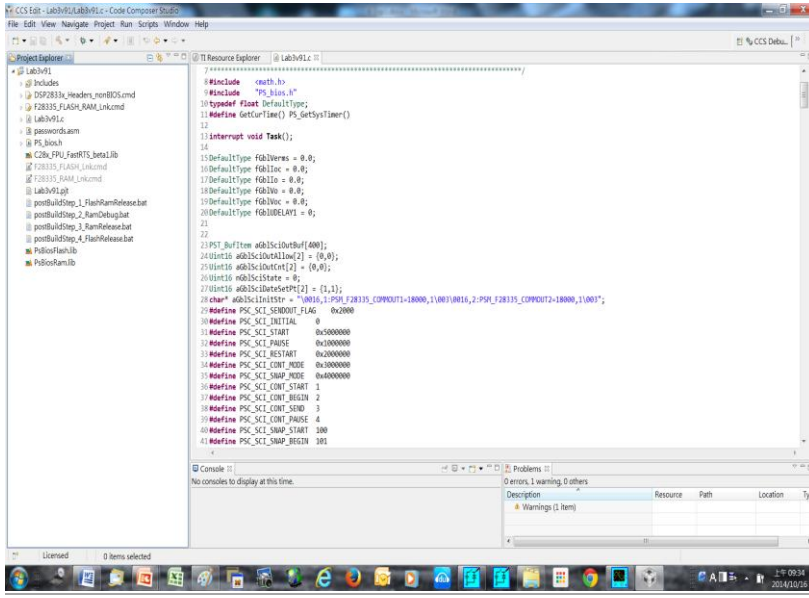
For example, Lab1.psimsch generates a subdirectory named “Lab1”.

Compile and burn via TI Code Composer

Enter the TI Code Composer Studio

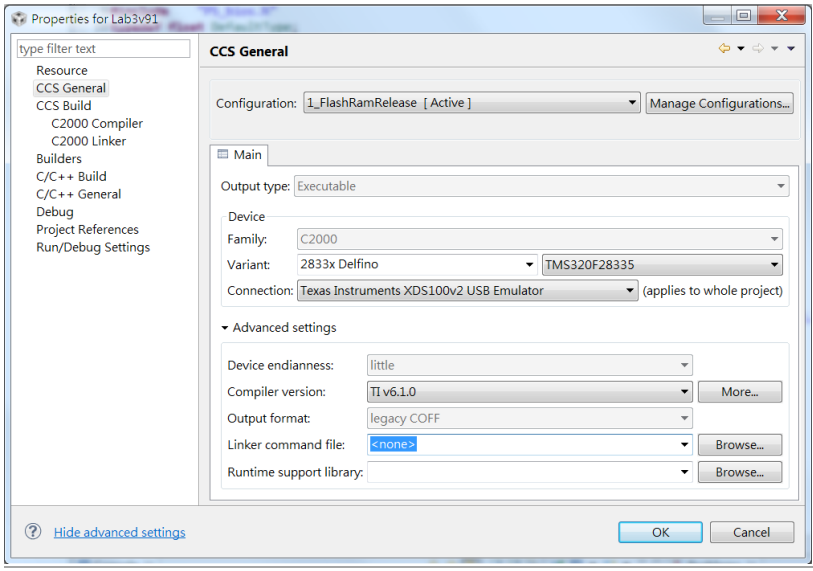
1. Bring up project: Lab1.pjt of the previous subdirectory (Lab1) by the following steps: Project => Import Legacy CCSv3.3 Project => Lab1.pjt under the subdirectory => Next => Finish.

The following screen will therefore appear where clicking Lab1.c is able to check the C file generated from SimCoder.



2. Click Lab1[Active, FlashRamRelease] => Build all to check if any error occurred. Warnings can be simply omitted.

3. Click Lab1[Active, FlashRamRelease]=> Right button => Set as follows



4. RUN => Debug => Burn program to DSPIC => Remove JTAG => Execute Experiment

Experiment Measurement

The experimental devices and teaching aid layout are illustrated as the figure 4.18. DC power supply, PSW 160-7.2, connects to the input terminal J201 of buck converter teaching aid. The output terminal J202 connects to electronic load PEL-2040 and utilizes constant resistance mode. The waveforms of output voltage and inductor current are indicated in the figure 4.19.

Figure 4.18 Experiment devices layout

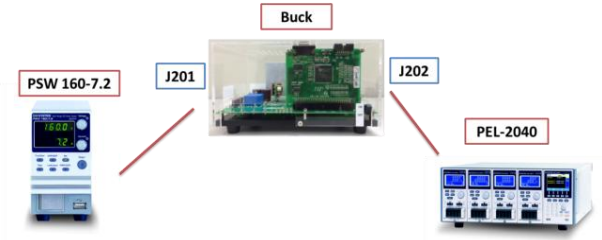
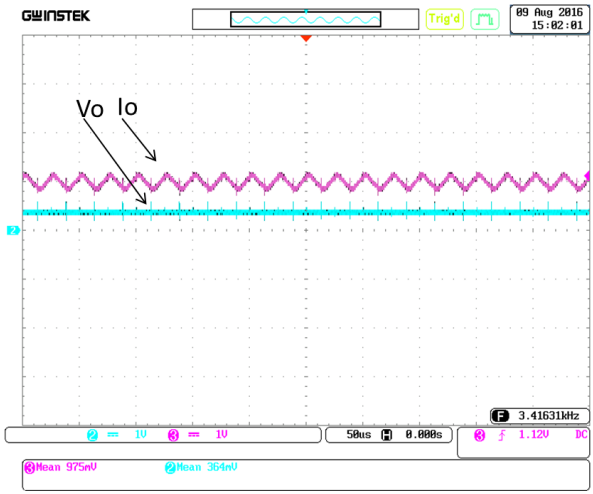


Figure 4.19 The measured waveform of converter output voltage and inductor current



It is allowd to turn on DSP Oscilloscope under PSIM when hardwae circuit is active so that the signal feedbacked from RS232-USB will be shown on computer.

Method to open DSP oscilloscop:

Utilities => DSP Oscilloscope => Refer to figure 4.20 for setting Serial port, which can be retrieved from the Device Manager under Control Panel, Baud rate, which requires to integrate with SCI Configuration,

Parity check, which requires to integrate with SCI Configuration => Press Connect once completing setting. The screen shows as figure 4.21, and 4.22 in which green light and signal feedbacked screen show when connecting successfully. If it needs to access to DSP Oscilloscope result, refer to the instructions as figure 4.23 by clicking Save to select a location for file storage followed by observing and processing to these signals via SIMVIEW.

Figure 4.20 DSP Oscilloscope setting

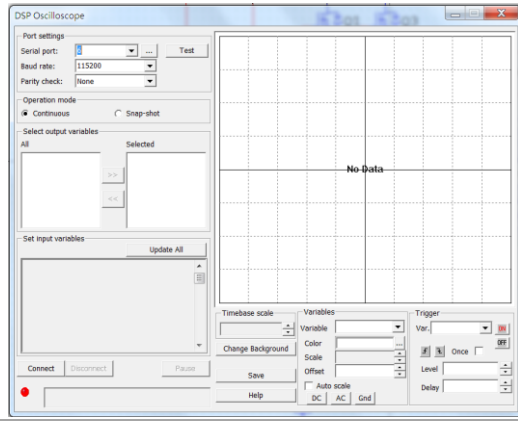


Figure 4.21 The converter output voltage and current waveforms from DSP Oscilloscope

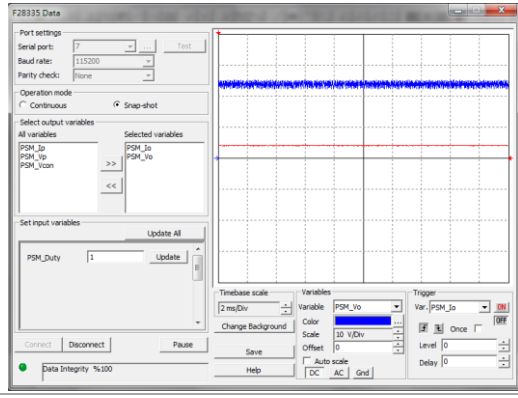


Figure 4.22 The converter input voltage and current waveforms from DSP Oscilloscope

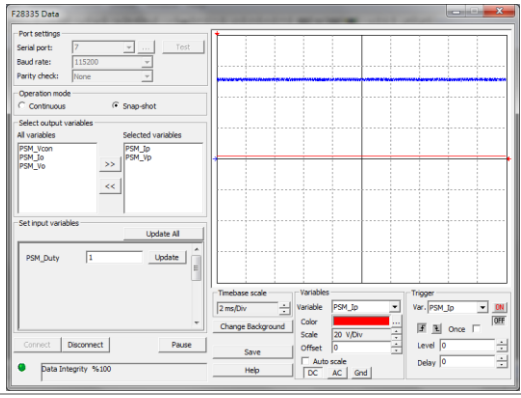
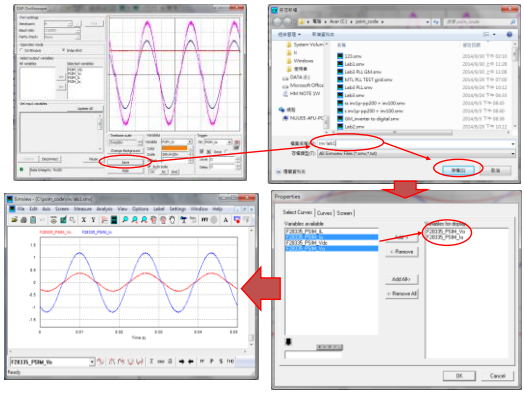


Figure 4.23 The method of converting DSP Oscilloscope waveforms to SIMVIEW



Experiment 2 – Buck Converter of Voltage Mode Control

The purpose of experiment

Realizes the derivation method for small-signal module of Buck converter, the method of bode plot scanning by AC sweep, the design of voltage loop controller, the hardware layout and SimCoder programming, etc.

The principle of experiment

Voltage Mode Control Architecture of Buck Converter

The circuit architecture of buck converter controlled by voltage mode is illustrated as the figure 5.1, which stratified samples output voltage V_o via kv, also through a low-pass filter (LPF), to obtain feedback output voltage V_{fb}, which is then compared with reference voltage V_{ref}. V_{ref} will go through adjustment by error amplifier (E/A) and a limiter (LIM) to get a control voltage V_{con}, which then goes through PWM comparator and compares with constant cyclic sawtooth wave V_{st} to earn the switch trigger signal V_{gate}. Through pulse wave, the dudty cycle V_{gate} adjusts output voltage V_o, which can be thus maintained steady and accurate even under either load change (R) or input voltage change (V_d).

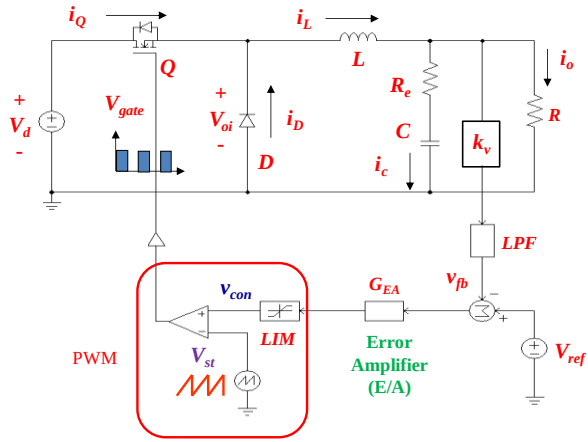


Figure 5.1 The buck converter of voltage mode control

Small signal module

The buck converter utilizing PWM switch control makes use of state average method to derive the small signal module, which can be used as basis of design to voltage loop error amplifier. Refer to the process below:

Step 1: State Average

The figure 5.2 demonstrates the buck converter switch and the state average circuit of diode under CCM. We can get the equations as follows in light of switch conduction and cut-off state:

$$\begin{aligned} i_a(t) &= i_c(t) \quad 0 < t < dT_s \\ &= 0 \qquad dT_s < t < T_s \end{aligned} \tag{5.1}$$

$$\begin{aligned} v_{cp}(t) &= v_{ap}(t) \quad 0 < t < dT_s \\ &= 0 \qquad dT_s < t < T_s \end{aligned} \tag{5.2}$$

We can further obtain as follows by state average of input current (i_a) and output voltage (v_{cp}):

$$i_a = di_c \tag{5.3}$$

$$v_{cp} = dv_{ap} \tag{5.4}$$

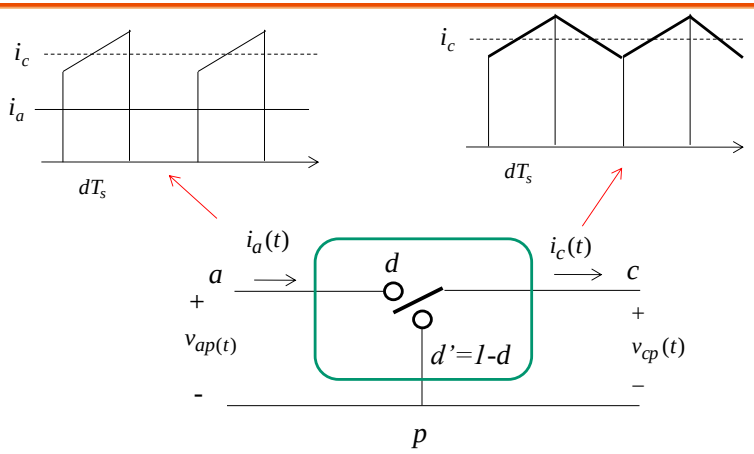


Figure 5.2 (a)

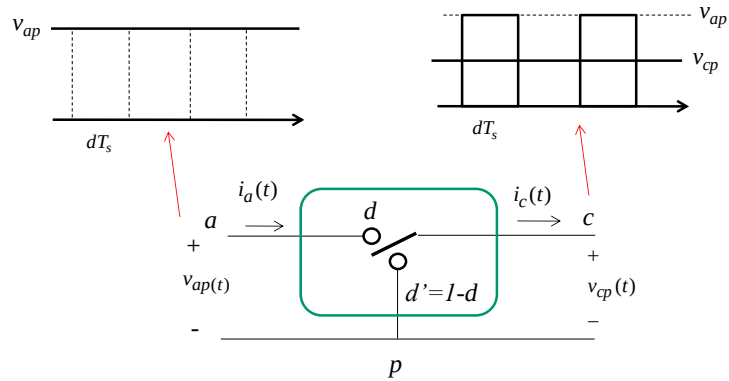


Figure 5.2 (b)

Figure 5.2 Buck converter switch and state average circuit of diode

Step 2: Add perturbation in work point to get the small signal module of steady state work point

$$i_a = I_a + \tilde{i}_a = di_c = (D+\tilde{d})(I_c+\tilde{i}_c) = DI_c + D\tilde{i}_c + \tilde{d}I_c + \tilde{d}\tilde{i} \qquad (5.5)$$

$$v_{cp} = V_{cp} + \tilde{v}_{cp} = dv_{ap} = (D+\tilde{d})(V_{ap}+\tilde{v}_{ap}) = DV_{ap} + D\tilde{v}_{ap} + \tilde{d}V_{ap} + \tilde{d}\tilde{v}_{ap} \qquad (5.6)$$

Where:

I, V, D: DC steady state work point

$\tilde{i},\tilde{v},\tilde{d}$: AC small signal perturbation quantity

The steady state work point can be obtained via the DC item of (2.5) and (2.6). The small signal equation of circuit as follows can be further obtained via the AC item of (5.5) and (5.6) with ignoring the multiplied items by 2 small signals.

$$\tilde{i}_a = D\tilde{i}_c + I_c\tilde{d} \tag{5.7}$$

$$\tilde{v}_{ap} = \frac{\tilde{v}_{cp}}{D} - \frac{V_{ap}}{D}\tilde{d} \tag{5.8}$$

Refer to the figure 5.3 where switch and small signal module circuit of diode can be drawn by (5.7) and (5.8).

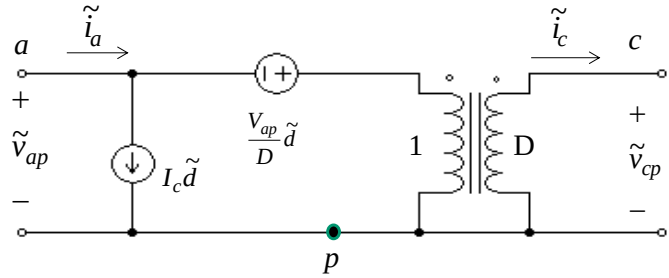


Figure 5.3 Switch and small signal module of diode circuit

Step 3: Merge the switch and diode equivalent circuit with output filter to obtain the small signal module of buck converter under CCM.

Refer to the figure 5.4 where merging the switch, via the figure 5.3, and diode equivalent circuit with output LC filter can obtain the small signal module of buck converter under CCM.

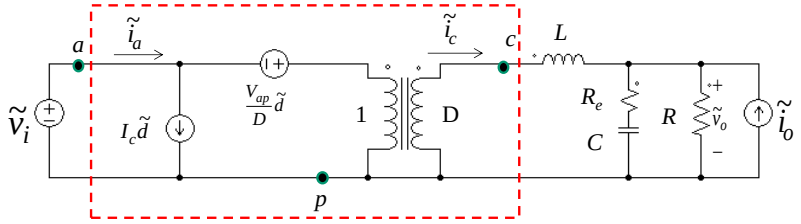


Figure 5.4 The small signal module of buck converter under CCM

The following transfer function can be obtained via the figure 5.4:

- Control to output transfer function, used in control loop design

$$G_{vd}(s) = \frac{\tilde{v}_o}{\tilde{d}}\Big|_{\tilde{v}_i=\tilde{i}_o=0} \tag{5.9}$$

- Output impedance, used in transient response design

$$Z_o(s) = \frac{\tilde{v}_o}{\tilde{i}_o}\Big|_{\tilde{v}_i=\tilde{d}=0} \tag{5.10}$$

- Line to output, used in input voltage ripple rejection design

$$G_{vd}(s) = \frac{\tilde{v}_o}{\tilde{v}_i}\Big|_{\tilde{d}=\tilde{i}_o=0} \tag{5.11}$$

From the figure 5.4 where the output voltage $\tilde{v}_o$ of small signal module of buck converter under CCM is influenced by the three perturbation items including input voltage $\tilde{v}_i$, load current $\tilde{i}_o$ and duty cycle $\tilde{d}$ .In order to get the transfer function from control to output, makes $\tilde{v}_i$ =$\tilde{i}_o$ =0. And get the equivalent circuit of the figure 5.5 via the figure 5.4. Refer to the figure 5.5 for the transfer function from control to output as follows:

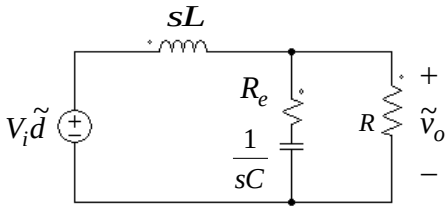
$$G_{vd}(s) = \frac{\tilde{v}_o}{\tilde{d}} = V_i \frac{1+\frac{s}{\omega_z}}{1+\frac{s}{Q\omega_o}+\frac{s^2}{\omega_o^2}} \tag{5.12}$$

Where

$$\omega_z = \frac{1}{R_e C},\ \omega_o = \frac{1}{\sqrt{LC}},\ Q = \frac{1}{\omega_o}\frac{1}{\frac{L}{R} + R_e C} \approx \frac{R}{\omega_o L} \tag{5.13}$$

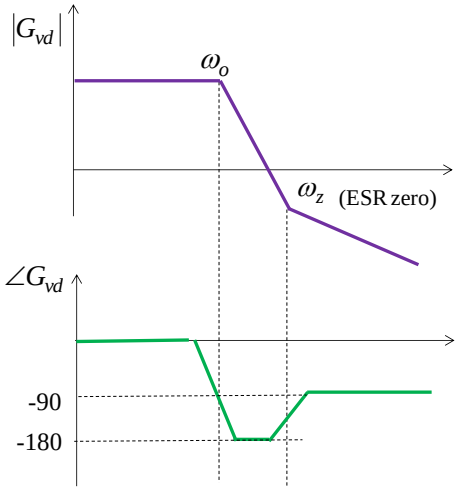
The pole ω_o is determined by the output LC filter, whereas zero point ω_z is decided by the output capacitance and ESR.

Figure 5.5 The equivalent circuit used to obtain transfer function from control to output



Refer to the figure 5.6 for the bode plot of transfer function from control to output drawn by (5.12).

Figure 5.6 The bode plot of transfer function from control to output



In order to get the transfer function of output impedance, makes $\tilde{v}_i = \tilde{d} = 0$. And get the equivalent circuit of the figure 5.7 via the figure 5.4. Refer to the figure 5.7 for the transfer function of output impedance:

$$Z_o(s) = sL\frac{1+\frac{s}{\omega_z}}{1+\frac{s}{Q\omega_o}+\frac{s^2}{\omega_o^2}} \tag{5.14}$$

$$\omega_z = \frac{1}{R_eC},\ \omega_o = \frac{1}{\sqrt{LC}},\ Q = \frac{1}{\omega_o}\frac{1}{\frac{L}{R}+R_eC} \approx \frac{R}{\omega_o L} \tag{5.15}$$

Refer to the figure 5.8 for the bode plot of transfer function of output impedance drawn by (5.14).

Figure 5.7 The equivalent circuit used to obtain transfer function of output impedance

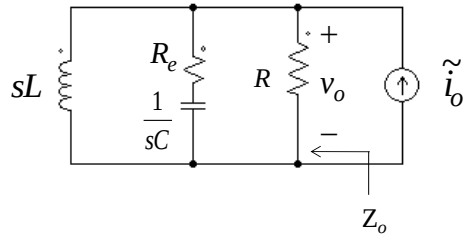
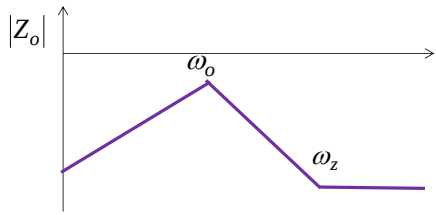


Figure 5.8 The bode plot of output impedance



In order to get the transfer function from input to output, makes $\tilde{i}_o = \tilde{d}$ =0. And get the equivalent circuit of the figure 5.9 via the figure 5.4. Refer to the figure 5.9 for the transfer function from input to output:

$$G_{vv}(s) = \frac{\tilde{v}_o}{\tilde{v}_i} = D\frac{1+\frac{s}{\omega_z}}{1+\frac{s}{Q\omega_o}+\frac{s^2}{\omega_o^2}} \tag{5.16}$$

$$\omega_z = \frac{1}{R_e C},\ \omega_o = \frac{1}{\sqrt{LC}},\ Q = \frac{1}{\omega_o}\frac{1}{\frac{L}{R}+R_e C} \approx \frac{R}{\omega_o L} \tag{5.17}$$

Refer to the figure 5.10 for the bode plot of transfer function from input to output drawn by (5.16).

Figure 5.9 The equivalent circuit used to obtain transfer function from input to output

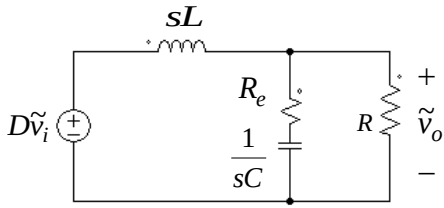
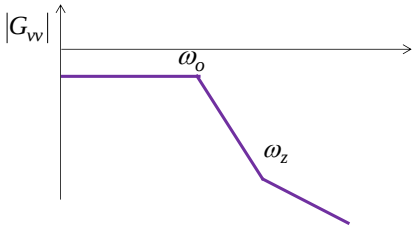


Figure 5.10 The bode plot of transfer function from input to output



Loop gain and voltage error amplifier

The control block diagram of buck converter utilizing voltage mode control is illustrated as the figure 5.11 where feedback outputs voltage (sampling block) and feedback voltage (V_{FB}) compares with reference voltage (V_{ref}) followed by obtaining the PWM control voltage (V_{con}) via adjustment of error amplifier. The switch trigger signal will be further obtained through comparison between PWM and sawtooth wave (V_t) from control voltage.

G_s is sampling circuit gain; G_s is transfer function of error amplifier; G_s is PWM gain; G_{vd} is the previous transfer function from control to output. The control loop diagram of figure 5.12 is obtained from the figure 5.11; via the previous transfer function, the detailed control loop block diagram can be presented as the figure 5.13 show.

Figure 5.11 The control block diagram of buck converter utilizing voltage mode control

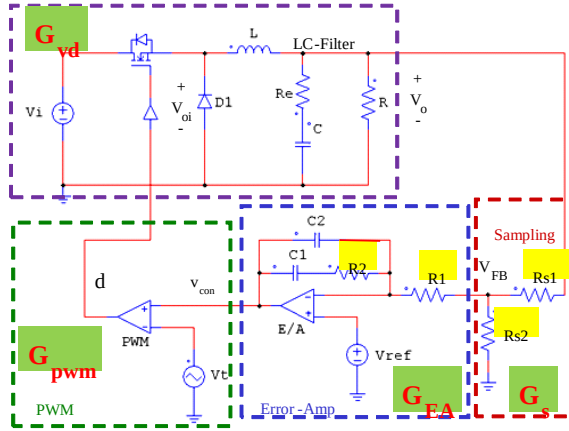


Figure 5.12 The control loop block diagram utilizing voltage mode control

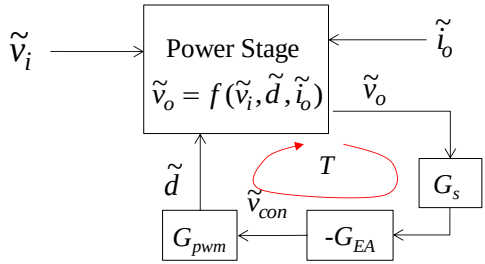
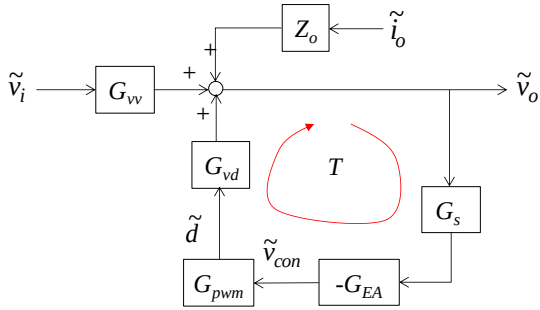


Figure 5.13 The detailed control loop block diagram utilizing voltage mode control



Loop Gain

The voltage closed-loop gain is illustrated as the figure 5.13:

$$T = G_s G_{EA} G_{pwm} G_{vd} \tag{5.18}$$

The design of conventional error amplifier (GEA) is based on the loop gain T, of which the bode plot is shown as the figure 5.14

where the frequency of zero dB point is called zero crossover frequency (f_{co}), which is equal to the bandwidth of voltage control loop (-3dB closed to 0dB). The deviation between the phase of zero crossover point and -180° is called phase margin (PM); when phase passes frequency of -180°, the gap between T gain and 0db is called gain margin (GM).

5. Loop Gain Requirement

- Lower frequency comes with bigger gain and better voltage regulation
- Wider bandwidth results in faster voltage response
- PM>45
- GM>10~20Db

G_{EA} is designed to make T satisfied with the previous requirements.

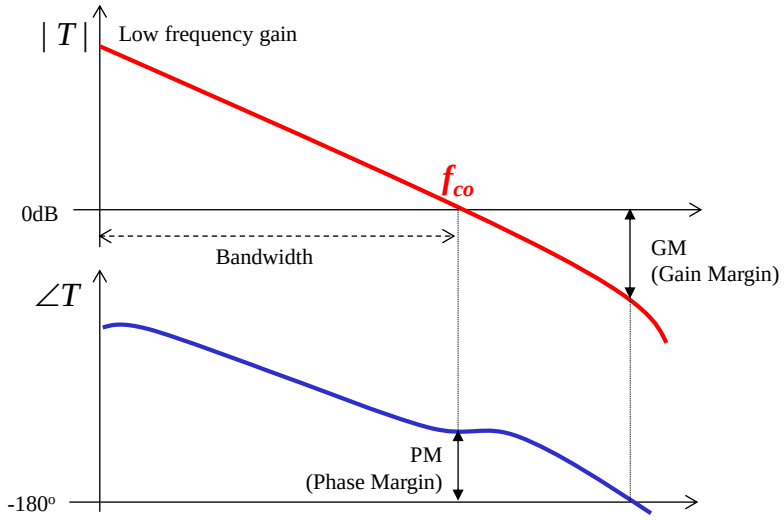


Figure 5.14 Loop gain bode plot

6. Experiment System Design

Experiment system control block and controller design

The control block diagram of experiment circuit voltage mode is illustrated as the figure 5.15 where G_{pwm} represents the gain from converter control voltage to converter output. Also, the low-pass filter LPF1 represents the low-pass filter added in voltage sensing circuit with bandwidth of 16kHz, p_1=2π*16k rad/s, whilst LPF2 is the low-pass filter standing for the bandwidth of voltage sensing component with bandwidth of 10kHz, p_2=2π*10k rad/s, both of which are the very needs for circuit completion to maintain loop stability and compensate by 2 zero points. FF is the feedforward controller containing one zero point (z_1) and the other (p_3). GV is the proportional integral (PI) controller convering another zero point (z_2) in addition to integral. The switch frequency is 40kHz and the Matlab program controlling loop design is illustrated below. The zero crossover frequency, based on the characteristics of H1 and FB from the figure 5.15, is set *fco* =700. The parameter setting of FF and *Gv* is z_1= 200* 2π in which z2 =300 and p_3 = 10e3 * 2π. The Km value can be therefore obtained. The bode plot, which is drawn based on the design and shown as the figure 5.16, solidly meets the previously mentioned design that *fco* is exactly 7000Hz, and PM-80 °.

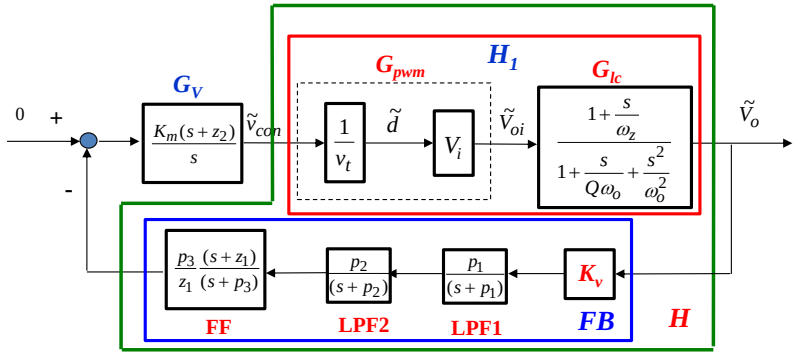


Figure 5.15 The voltage mode control block diagram of actual circuit

Program: Buck2.m

```
% Buck with Type 3 Voltage Mode Control
clf;
clc;
```

```
PI = 3.1416;
Vd=50;
Vo=24;
Po=100;
Io=Po/Vo;
Iomin = Io * 0.1;
fs=40e3;
ws = 2* PI * fs;
Ts=1/fs;
Vt=5;
% PWM
D = Vo/Vd;
Vcon = D * Vt;
% LC
R = Vo/Io;
L = Ts * Vo * (1-D)/(2*Iomin);
L = 365e-6;
Re = 0.13/3;
C = 300e-6;
% Small signal model
Gpwm = Vd/Vt;
wz = 1/(Re * C);
fz = wz/(2*PI)
wo = 1/sqrt(L*C);
fo = wo/(2*PI)
Q = R/(wo*L);
numLC = [1/wz 1];
denLC = [1/wo^2  1/(Q*wo)  1];
numH = Gpwm * numLC;
denH = denLC;
H1=tf(numH, denH);
% Controller Design
fco =700
wco = 2 * PI * fco;
Hr = freqresp(H, wco);
GainH = abs(Hr);
Hdb = 20 * log10(GainH);
GainGv = 1/GainH;
Kv = 1/40;
p1 = 16e3 * 2 * PI
```

```
p2 = 10e3  * 2 * PI
numFB1 = Kv * p1;
denFB1 = [1 p1];
FB1=tf(numFB1, denFB1);
numFB2 = p2;
denFB2 = [1 p2];
FB2=tf(numFB2, denFB2);
FB = series(FB1, FB2);
H = series(H1, FB);
z1= 200* 2 * PI
z2 =300
p3 = 10e3 * 2 * PI
tu = 1/z2
Am = p3/z1
% Type 3 Gv(s)= Am*(s+z1)/(s+p3) * Km* (s+z2)/s
% Type 3 Gv(s)= FF* PI
% FF = p3/z1*(s+z1)/(s+p3)  = Am * (s+z1)/(s+p3)
% PI = Km * (s+z2)/s
numFF = Am * [1  z1];
denFF = [ 1  p3];
FF = tf(numFF, denFF);
numGv1 = [1 z2];
denGv = [1   0];
Gv1 = tf(numGv1, denGv);
Gv2 = series(Gv1, FF);
Gv2r = freqresp(Gv2, wco);
GainGv2r = abs(Gv2r);
Km = GainGv/GainGv2r
Gv = Km * Gv2;
GvH = series(Gv, H);
GvHr = freqresp(GvH, wco);
phaseGvH = angle(GvHr) * 180/PI
wmin = 1 * 2* PI;
wmax = 100e3 * 2 *PI;
bode(H, Gv, GvH, {wmin, wmax});
grid;
```

=>

```
fz = 1.2243e+004
fo = 480.9634
```

fco = 700
p1 = 1.0053e+005
p2 = 62832
z1 = 1.2566e+003
z2 = 300
p3 = 62832
tu = 0.0033
Am = 50.0000
Km = 1.2688
phaseGvH = -103.0929

The design result of Matlab is cleaerly shown as follows:

Circuit parameter	V_d=50, V_o=24, f_s=40kHz, V_t=5, L = 365μH, R_e = 0.13/3Ω, C = 300μF;
Feedback parameter	K_v=1/40, $\mathrm{LPF1}=\frac{(s+2\pi\times16k)}{s}$, $\mathrm{LPF2}=\frac{(s+2\pi\times10k)}{s}$, $\mathrm{FF}=\frac{62832}{1256}\frac{(s+1256)}{(s+62832)}=50\frac{(s+1256)}{(s+62832)}$
Controller parameter	$G_v=\frac{1.2688(0.0033s+1)}{0.0033s}$

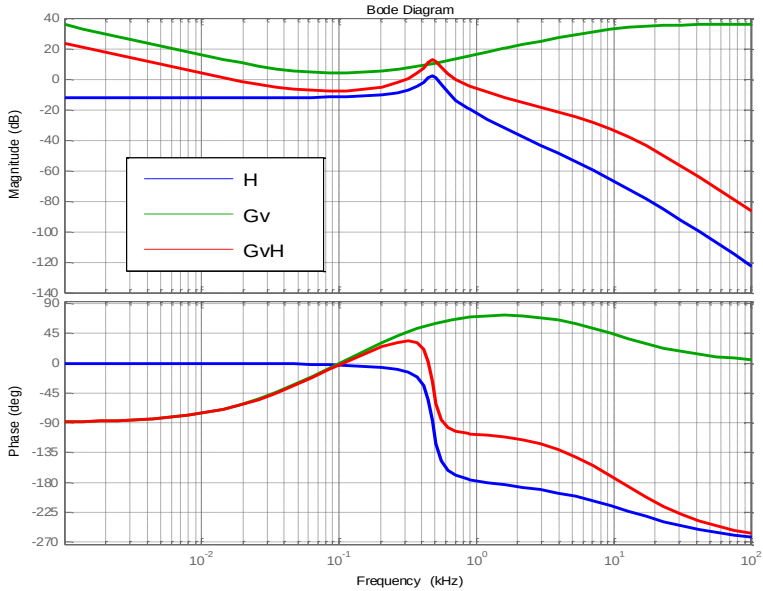


Figure 5.16 Voltage control loop bode plot

Circuit Simulation

The PSIM simulating circuit, which is based on the previous design result and shown as the figure 5.17, contains a soft starter circuit utilizing the linear rise of voltage command to proceed to (VSS), which selects, via a minimum value select box along with the original voltage command, the final voltage command (VC). Refer to the figure 5.18 for the simulating result of change from 50W to 100W. To adjust soft starter circuit, it needs the requirements of start time and start current with availability of 1m value modification for adjustment.

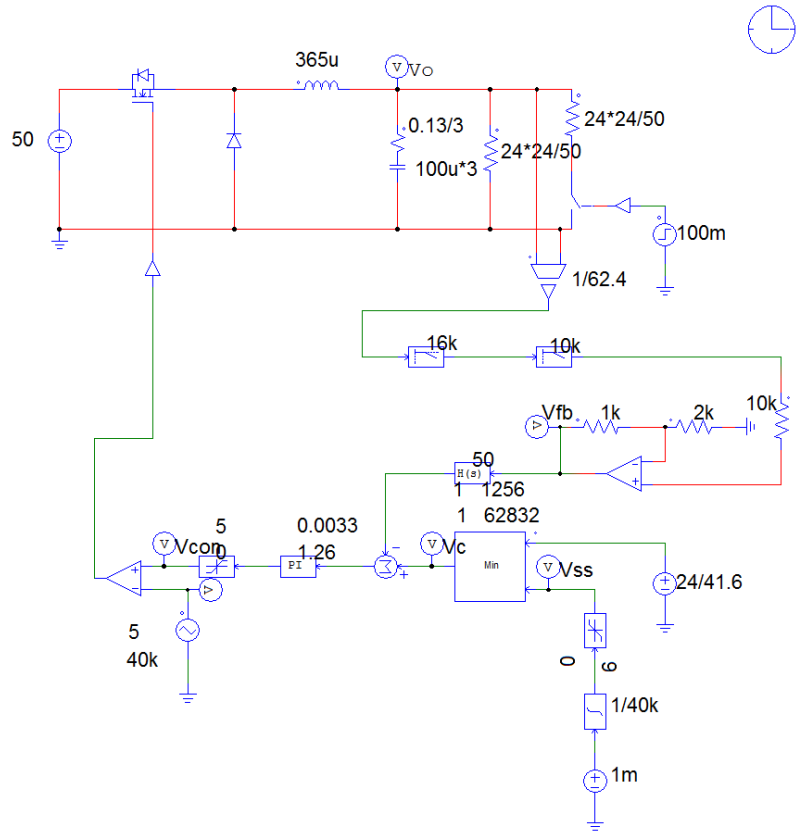


Figure 5.17 Analog PSIM simulating circuit of buck converter voltage mode control (buck2.psimsch)

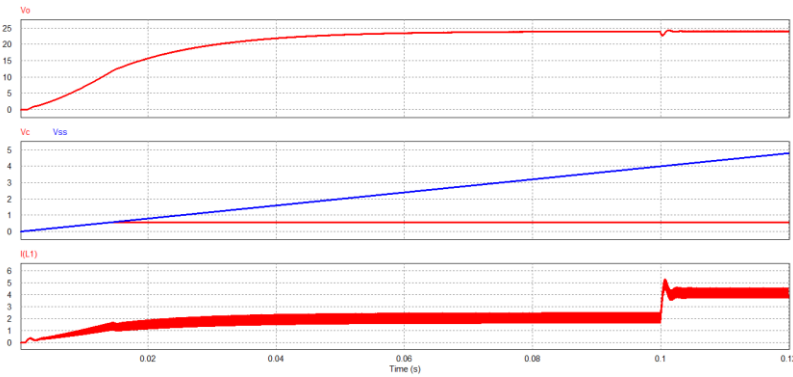


Figure 5.18 (a)

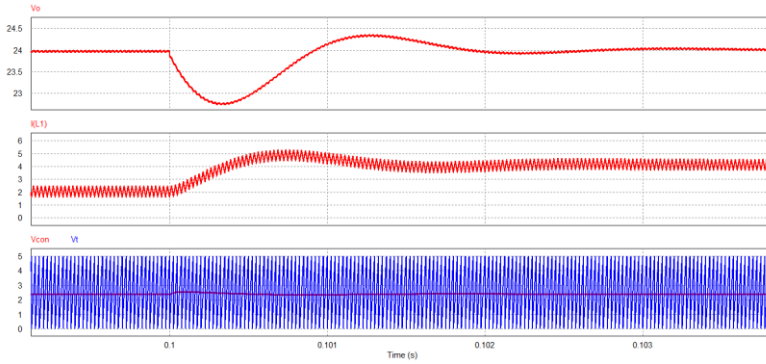


Figure 5.18 (b)

Figure 5.18 Analog PSIM simulation of buck converter voltage mode control

In order to validate the accuracy of control loop design, the AC sweep of voltage loop is proceeded, as the figure 5.19 shown, with the sweep result as the figure 5.20 shown, which is identical to the result of bode plot of Matlab as the figure 5.16.

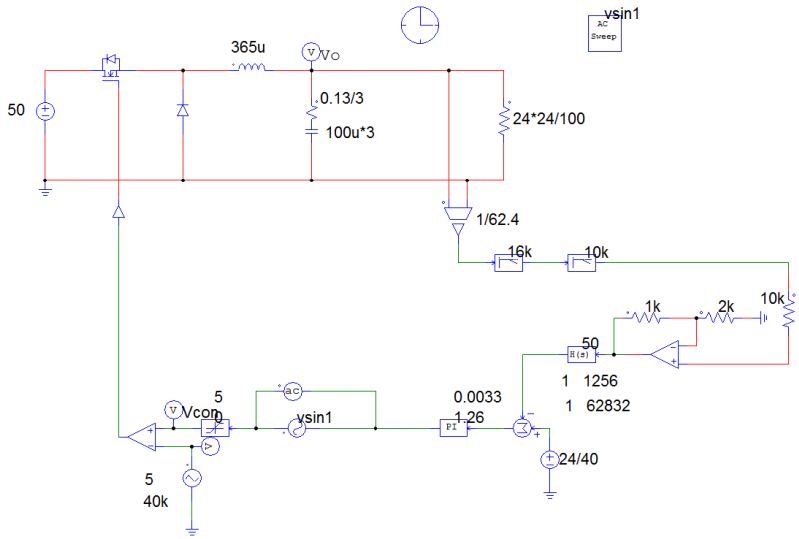


Figure 5.19 AC sweep of voltage loop of buck converter (buck2_AC.psimsch)

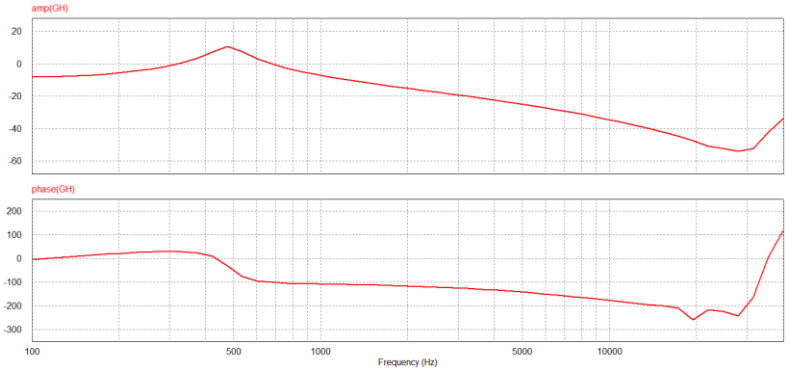


Figure 5.19 AC sweep result of voltage loop of buck converter

In addition to constant voltage (CV) control of buck converter shown in the figure 5.12, the PSIM simulating program of constant current (CC) control, of which level setting is 5A, is also added.

The simulating result of change of load resistor from 6Ω (4A for 24V) to 3Ω (8A for 24V) is shown as the figure 5.22; when load current is equal to 4A, CV activates and voltage maintains in 24V, whilst CC activates to limit output current within 5A, due to 5A

above, when load changes to 3Ω; the output voltage, therefore, reduces to 15V (=3Ω x 5A).

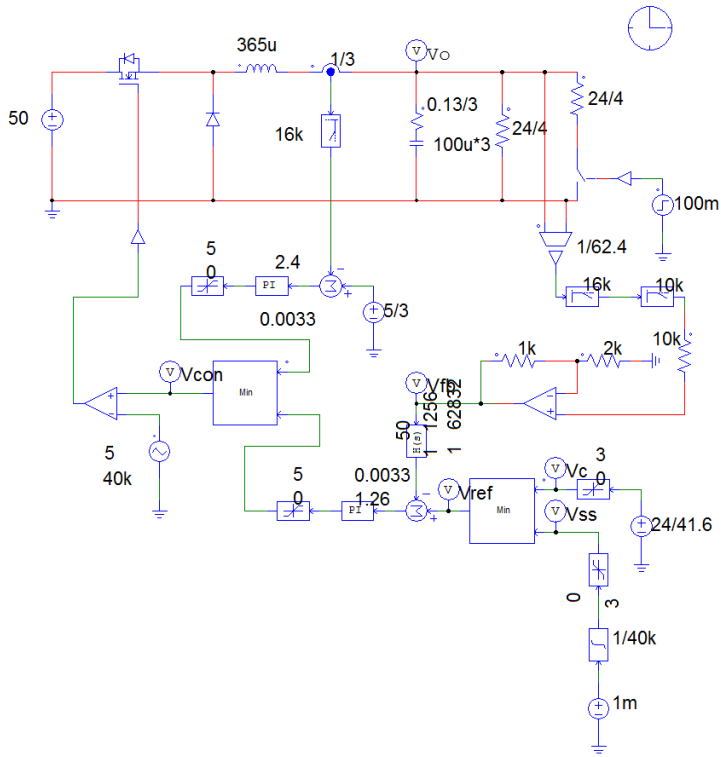


Figure 5.21 PSIM simulating program of buck converter containing CV and CC controls (buck_2_I_Limit.psimsch)

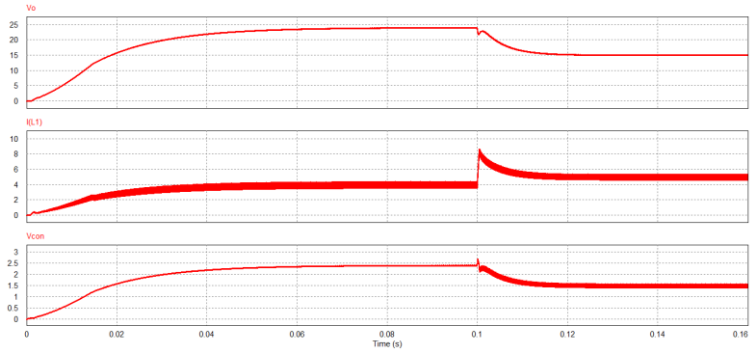


Figure 5.22 CV and CC Simulating results

SimCoder Program Layout

The voltage mode control SimCoder program of buck converter shown in the figure 5.23 is established by blocks of code converted from the previous analog simulating circuit utilizing TI F2833X Target and PSIM.

The G_V (PI controller) and FF ($\frac{p_3}{z_1}\frac{(s+z_1)}{(s+p_3)}$) can be converted to digital control block via PSIM>Utility>s2z Converter.

In terms of skills, there are mainly 3 points to notice for conversion from s to z of PI as the figure 5.24 shown: (1) It suggests adopting Back Euler digital conversion. (2) A limiter, which is both positive and negative and able to meet the limit value of PI, is required to add in integral (accumulation). For example, the limit value of PI is 0~5, the limit value of integral, accordingly, is set -5~+5. (3) The integral (accumulation) signal, which starts operation after PWM activates whilst it is reset to zero when PWM stops, is multiplied by a Run signal.

The conversion from s to z of FF, which utilizes the Domain Function of General (1st-Order) and the conversion of Bilinear (Tunstin), is shown as the figure 2.25. The parameter setting of s-Domain is identical to the analog setting with sampling frequency equal to switch frequency f_s=40kHz.

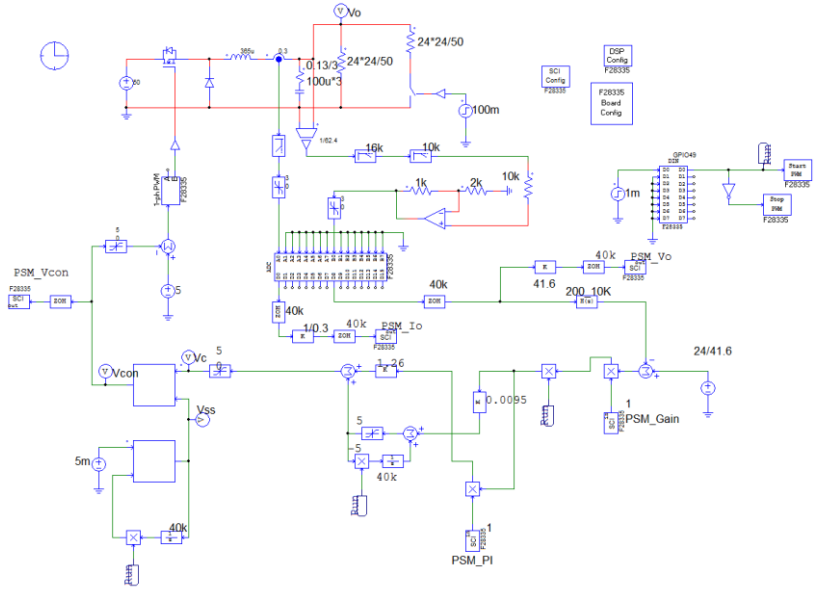


Figure 5.23 SimCoder program of voltage mode control of buck converter (Lab2.psimsch)

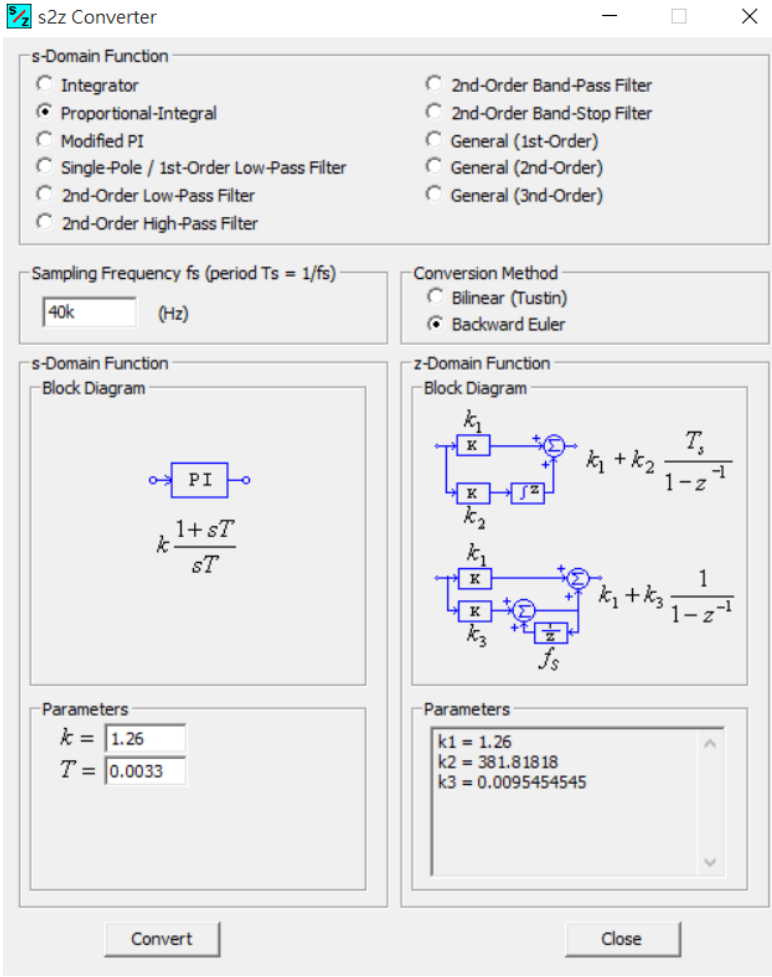

s2z Converter
s-Domain Function
Integrator
Proportional-Integral
Modified PI
Single-Pole / 1st-Order Low-Pass Filter
2nd-Order Low-Pass Filter
2nd-Order High-Pass Filter
2nd-Order Band-Pass Filter
2nd-Order Band-Stop Filter
General (1st-Order)
General (2nd-Order)
General (3nd-Order)
Sampling Frequency fs (period Ts = 1/fs)
40k
(Hz)
Conversion Method
Bilinear (Tustin)
Backward Euler
s-Domain Function
Block Diagram
PI
$k\frac{1+sT}{sT}$
z-Domain Function
Block Diagram
$k_1 + k_2 \frac{T_s}{1-z^{-1}}$
$k_1 + k_3 \frac{1}{1-z^{-1}}$
Parameters
k = 1.26
T = 0.0033
Parameters
k1 = 1.26
k2 = 381.81818
k3 = 0.0095454545
Convert
Close

Figure 5.24 (a)

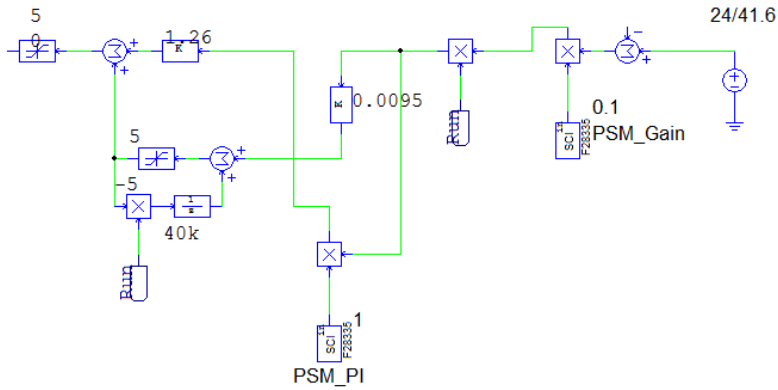


Figure 5.24 (b)

Figure 5.24 Conversion from s to z of PI: (a) s2z Converter setting (b) SimCoder program

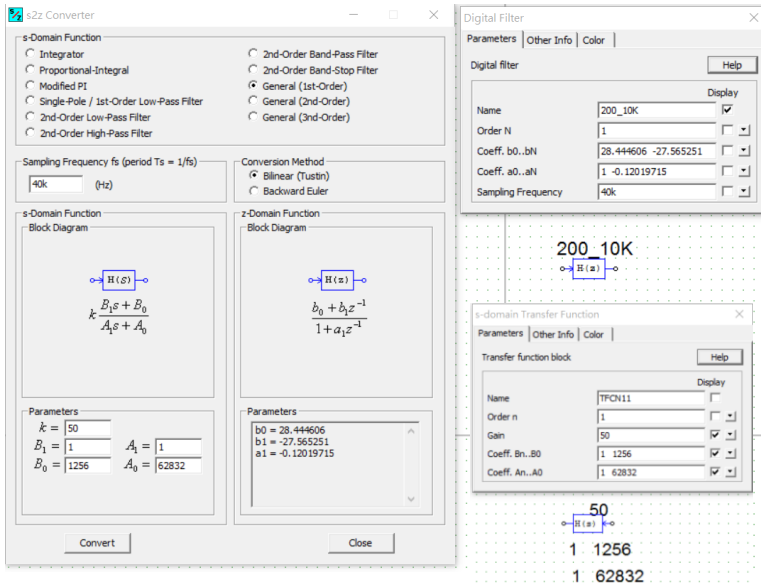


Figure 5.25 Conversion from s to z of FF

StartPWM and StopPWM settings are illustrated within the figure 5.23 and configured by the DI of GPIO 49, which connects to the start switch of hardware; PWM activates after switch starts and switch is activated for 1ms in simulation.

What makes difference from analog is that soft starter is executed by the limit of control voltage; either way is available.

The accuracy of SimCoder program is validated via simulation; the simulating result of the figure 5.23, which is shown as the figure 5.26, is in proximity to the analog simulation of the figure 5.18 to verify the validity of program.

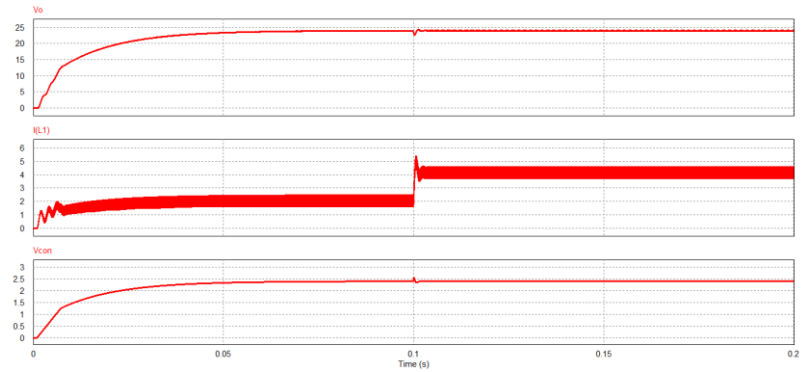


Figure 5.26 (a)

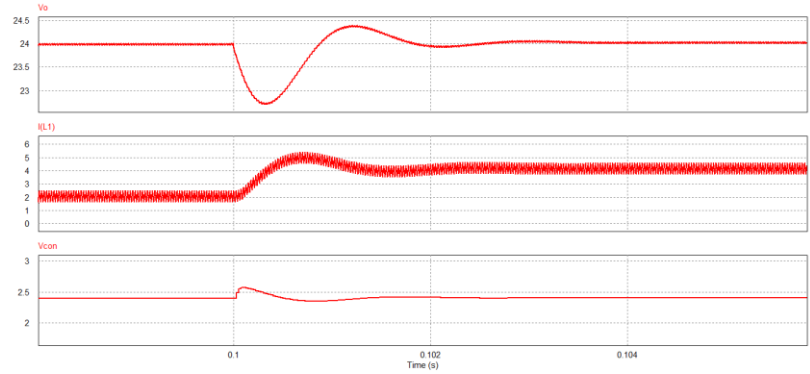


Figure 5.26 (b)

Figure 5.26 Simulating result of voltage mode digital control (figure 5.21) of buck converter

The SimCoder program with CV and CC loops, which is shown as the figure 5.27, can be obtained by the analog circuit of the figure 5.21 through s2z conversion. The simulating result, which is shown as the figure 5.28, is in proximity to the analog simulation.

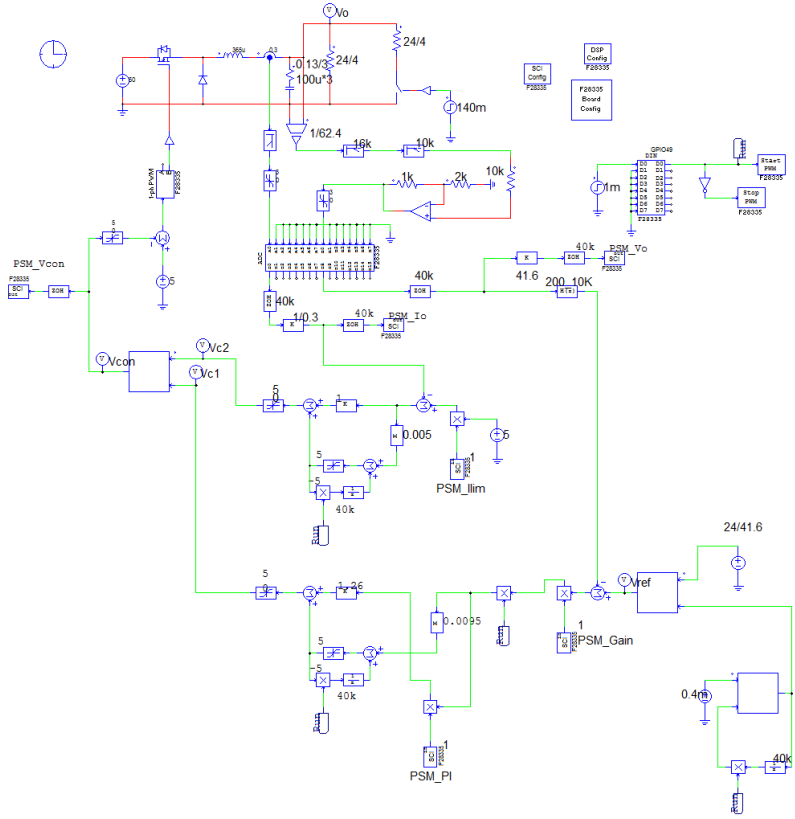


Figure 5.26 (b)

Figure 5.27 Buck converter containing SimCoder program convering CV and CC controls (Lab2_limit.psimsch)

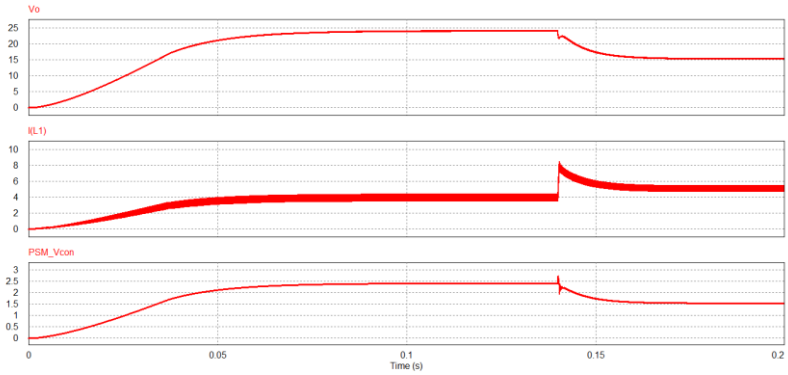


Figure 5.28 Simulating result of the figure 5.27

Experiment Measurement

The experimental devices and teaching aid layout are illustrated as the figure 5.29. DC power supply, PSW 160-7.2, connects to the input terminal J201 of buck teaching aid. The output terminal J202 connects to the DC electrical load, PEL-2040, and utilizes constant resistance mode. The output voltage and inductive current measured waveform are shown in the figure 5.30.

Figure 5.29 Experiment devices layout

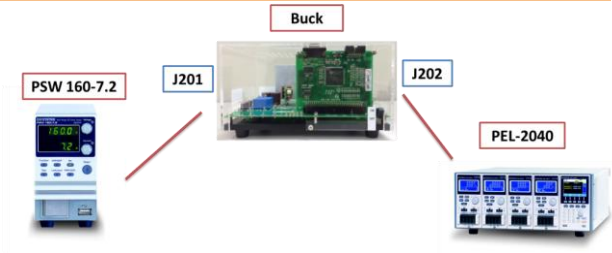
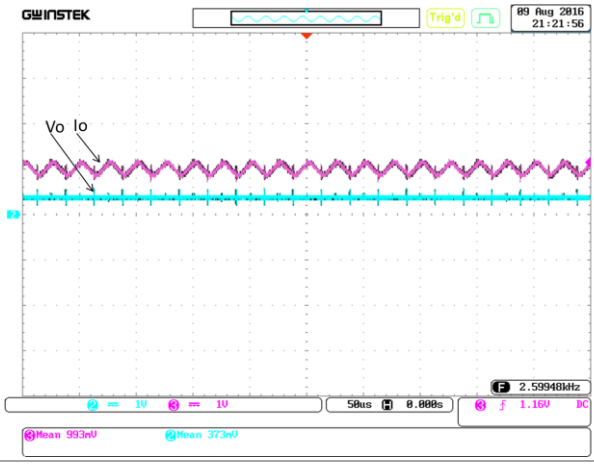


Figure 5.30 Output voltage of converter and measured waveform of inductive current



Experiment 3 – Average Current Mode Control

The purpose of experiment

To learn the control method of average current mode from buck converter including model derivation of current loop and voltage loop, controller design, hardware layout and SimCoder programing, etc.

The principle of experiment

Current mode control method

As the figure 6.1 shown, the current mode control architecture of buck converter utilizes dual-loop design where outer loop is voltage loop which is used to adjust voltage error and produce current command (V_c) of current inner loop. The error of current loop command and sensing current ($I_L R_i$) further passes through PWM to produce drive signal of switch; the sensing current may be either switch current or inductive current depending on the adotped control method.

The methods of current mode control cover the following ways shown in the figure 6.2: peak current mode control, valley current mode control, constant on-time control, constand off-time contril, hysterestic current control, average current control, etc. In addition, charge control, V2 constant on-time control are also included, whilst this experiment only focuses on the part of average current control. Refer to the following contents for details:

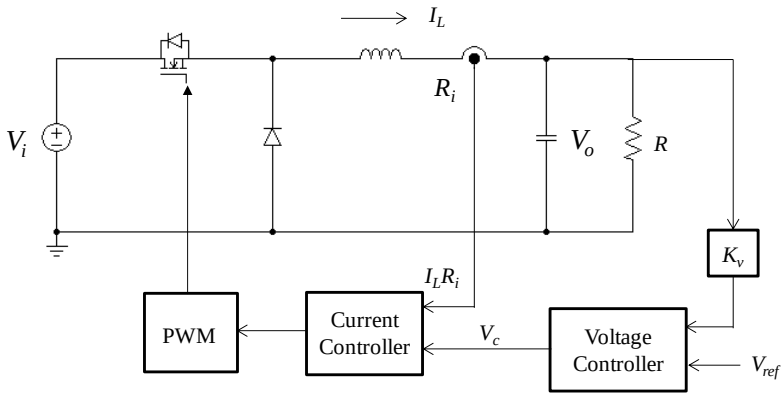
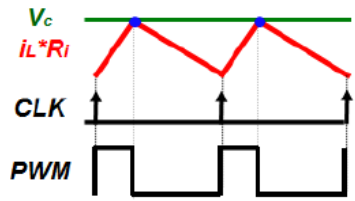
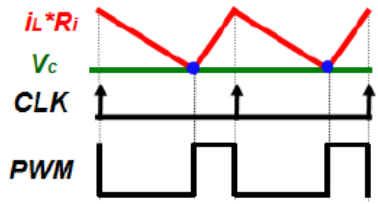


Figure 6.1 Current mode control architecture of electrical converter

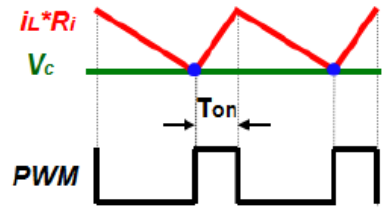
Figure 6.2 Main method of current mode control: (a) peak current mode control



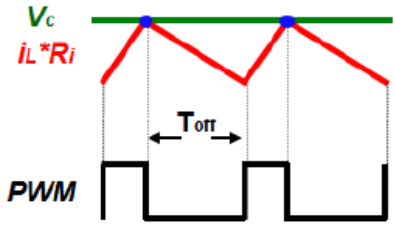
(b) valley current mode control



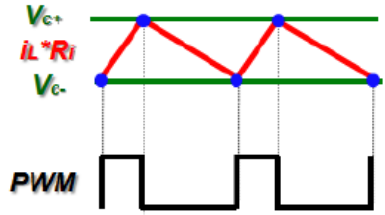
(c) constant on-time control



(d) constant off-time control



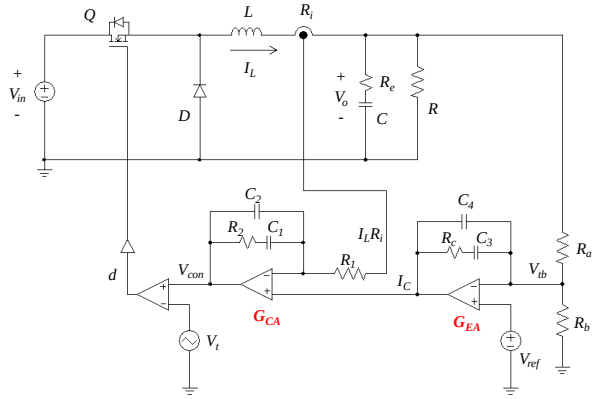
(e) hysterestic current control



The principle of average current control

As the figure 6.3 shown, the control block diagram of average current control generates inductive current command (I_c) via outer loop voltage error amplifier (G_{EA}) for voltage adjustment followed by comparing sensing inductive current ($I_L R_i$) with I_c and generating the control voltage (V_{con}) that PWM requires after going through adjustment from current error amplifier (G_{CA}). In the end, the trigger signal of switch is obtained through comparison between V_{con} and PWM sawtooth wave (V_t).

Figure 6.3
Average current control



Current loop design

With the state average method, we may obtain the follows from the figure 6.3:

$$L\frac{dI_L}{dt} = dV_{in} - V_o \tag{6.1}$$

By ignoring the changes of V_o and V_{in}, we may obtain the follows from the (6.1):

$$\frac{\tilde{I}_L}{\tilde{d}} = \frac{V_{in}}{sL} \tag{6.2}$$

Taking the current sensing ratio and PWM gain into account, we may obtain as the following:

$$H_i(s) = \frac{\tilde{I}_L R_i}{\tilde{V}_{con}} = \frac{\tilde{I}_L R_i}{\tilde{d}V_t} = \frac{R_i V_{in}}{sLV_t} \tag{6.3}$$

In respect to first-class system, current error amplifier (G_{CA}) can be designed via the method of second-class error amplifier as the figure 6.4 shown; due to the fact that PWM control voltage interconnects with sawtooth wave signal for one time a cycle, the maximum bandwidth (ω_{co}) of current loop, therefore, is affected by the limit of rising slope where V_{con} rising slope is smaller than PWM sawtooth wave (V_t). The rising slope of V_{con} can be determined by the falling slope of, via G_{CA} amplification, sensing inductive current, and we may obtain as follows from the previous limit:

$$(V_o / L)R_i G_{CA,\max}(\omega_{co}) = V_t f_s \tag{6.4}$$

(6.4) After refresh we can obtain the following:

$$G_{CA,\max}(\omega_{co}) = \frac{\tilde{V}_{con}}{R_i \tilde{I}_L} = \frac{V_t f_s L}{V_o R_i} \tag{6.5}$$

Via (6.3) and (6.5) with utilizing $G_{CA,\max}(\omega_{co})H_i(\omega_{co}) = 1$ we can obtain as follows:

$$\frac{V_t f_s L}{V_o R_i}\frac{R_i V_{in}}{\omega_{co} L V_t} = 1 \tag{6.6}$$

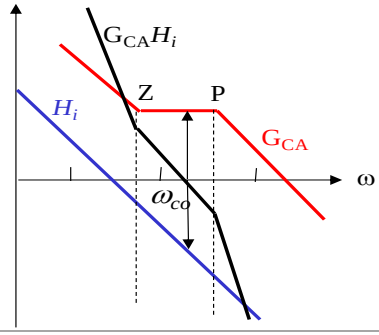
(6.6) After refresh we can obtain the following:

$$\omega_{co,\max} = \frac{V_{in} f_s}{V_o} \text{ (rad/s)} \quad (6.7)$$

$$f_{co,\max} = \frac{f_s}{2\pi D} \quad (6.8)$$

From (6.8), if designed by the rising slope limit of control voltage V_{con}, the maximum current loop bandwidth, theoretically, will be possibly either higher or close to switch frequency and thus we do Not design via this value. Generally, by limiting within noise ratio, bandwidth selection (ω_{co}) can be set at 1/4 ~ 1/8 of the switch frequency. Once bandwidth (ω_{co}) is selected, it is available to utilize K-factor to make the second-class error amplifier $z = \omega_{co}/K$, $p = \omega_{co}/K$.

Figure 6.4 Current loop design of average current control



Voltage Loop Design

The general response speed of voltage loop is far slower than that of current loop; hence, when modeling voltage loop, we view current loop as ideal, that is, sensing inductive current with the command response is regarded as 1 as follows:

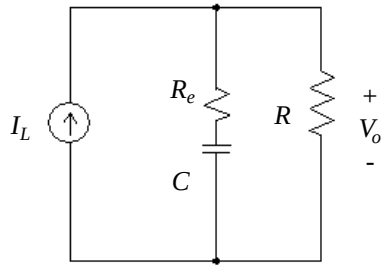
$$\frac{R_i \tilde{I}_L(s)}{\tilde{I}_c(s)} = 1 \quad (6.9)$$

Based on the presumption, the voltage loop equivalent circuit of average current control can be simplified as the figure 6.5 (a) shown as follows:

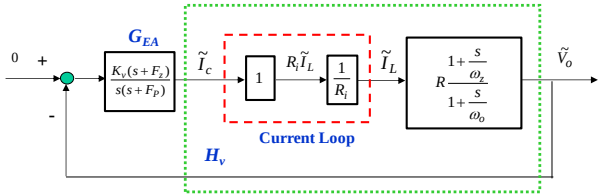
$$\frac{\tilde{V}_o}{\tilde{I}_L} = R\frac{1+\frac{s}{\omega_z}}{1+\frac{s}{\omega_o}},\ \omega_z = \frac{1}{CR_e},\ \omega_p = \frac{1}{CR} \tag{6.10}$$

The control block diagram of voltage loop, via (6.9) and (6.10), can be drawn as the figure 6.5 (b) shown. The voltage error amplifier (G_{EA}) can also be designed by adopting the previous second-class error amplifier as shown in the figure 6.5 (c). The bandwidth of voltage loop can be designed at the 1/3~1/5 of current loop bandwidth.

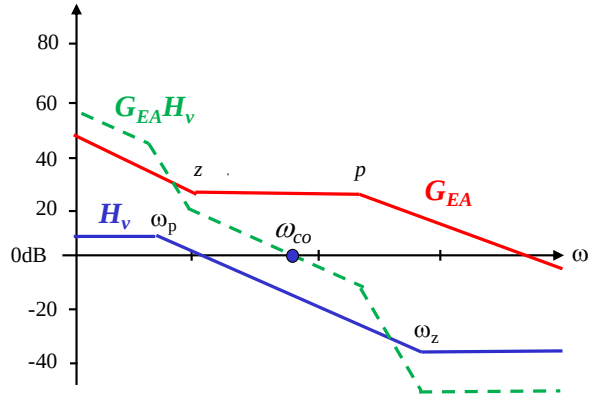
Figure 6.5 Voltage error loop design: (a) voltage loop equivalent circuit



(b) voltage loop control block diagram



(c) voltage loop bode plot



The spec of buck converter of average current control in the experiement is shown as follows. Based on the previous design method, please design the voltage and current error amplifier and validate with simulation:

V_i = 50V

V_o = 24V

f_s = 40kHz

K_s (R_i)= 0.3

K_v = 1/40

L = 365μH

C = 300μF(130mΩ/3)

V_t = 5V

$I_{o,max}$ = 100W/24A (6.11)

Based on the previous voltage and current loop models and the design of second-class error amplifier, the design program composed in MATLAB is as follows:

(Buck_average.m)

Matlab program design of average current control is as the following:

```
% Buck with average current control
clf;
clc;
```

```
PI = 3.1416;
Vd=50;
Vo=24;
Po=100;
Io=Po/Vo;
fs=40e3;
ws = 2* PI * fs;
Kv = 1/40;
Ks = 0.3;
Ts=1/fs;
Vt=5;
Vref=Kv * Vo;
% PWM
D = Vo/Vd;
Vcon = D * Vt;
% LC
L = 365e-6;
Re = 100e-3;
C = 300e-6;
R = Vo/Io;
% Hi
num1= Ks*Vd/(Vt*L) ;
den1= [1 0];
Hi=tf(num1,den1);
% Gca Design - fcoi = fs/20;
% Type 2 control Gca=K(s+z)/s(s+p)
% set the z to be wcoi/5
% set the p to be LPF
fcoimax=fs/(2*PI*D);
wcoi =  2*PI*fs/20;
```

```
fcoi = wcoi/(2*PI)
z= wcoi/5
p= 2* PI * 16e3 ;
Gain1 =  1/abs(freqresp(Hi, wcoi));
numGca1= [1 z];
denGca=[1 p 0];
Gca1=tf(numGca1, denGca);
Gain2 = abs(freqresp(Gca1, wcoi));
K1 = Gain1/Gain2;
Km1 = K1/p
Gca = K1 * Gca1;
GHi=Gca*Hi;
GHio =  freqresp(GHi, wcoi);
phaseGHio = angle(GHio) * 180/PI;
PMi = 180 + phaseGHio
figure(1);
bode(Hi, Gca, GHi, {100 5000000});
grid;
% Hv
wz = 1/(Re*C);
wp = 1/(R*C);
num2= R*[1/wz  1];
den2= [1/wp 0];
Hv1=tf(num2, den2);
p1 = 16e3 * 2 * PI
p2 = 10e3  * 2 * PI
numFB1 = Kv * p1;
denFB1 = [1 p1];
FB1=tf(numFB1, denFB1);
numFB2 = p2;
```

```
denFB2 = [1 p2];
FB2=tf(numFB2, denFB2);
FB = series(FB1, FB2);
Hv = series(Hv1, FB);
% PI control G=Km2(s+z)/s
fcov = fcoi/20
wcov=2*PI*fcov;
z= wcov/5
tu = 1/z
Gain3 = 1/abs(freqresp(Hv, wcov));
numGea1= [1 z];
denGea=[1 0];
Gea1=tf(numGea1, denGea);
Gain4 = abs(freqresp(Gea1, wcoi));
Km2 = Gain3/Gain4
Gea = Km2 * Gea1;
GHv=Gea*Hv;
GHvo =  freqresp(GHv,wcov);
phaseGHvo = angle(GHvo) * 180/PI;
PMv = 180 + phaseGHvo
figure(2);
bode(Hv, Gea, GHv, {100 5000000});
grid;
```

■ The design result is as follows:

fcoi = 2000

z = 2.5133e+003

Km1 = 1.5109

PMi = 71.5653

p1 = 1.0053e+005

p2 =62832

fcov = 100

z = 125.6640

tu = 0.0080

Km2 = 7.5386

PMv = 78.8391 (6.12)

The bode plot of control loop utilizing average current control is as the figure 6.6 shown. The figure 6.6 (a) indicates current loop, whilst the figure 6.6 (b) stands for voltage loop.

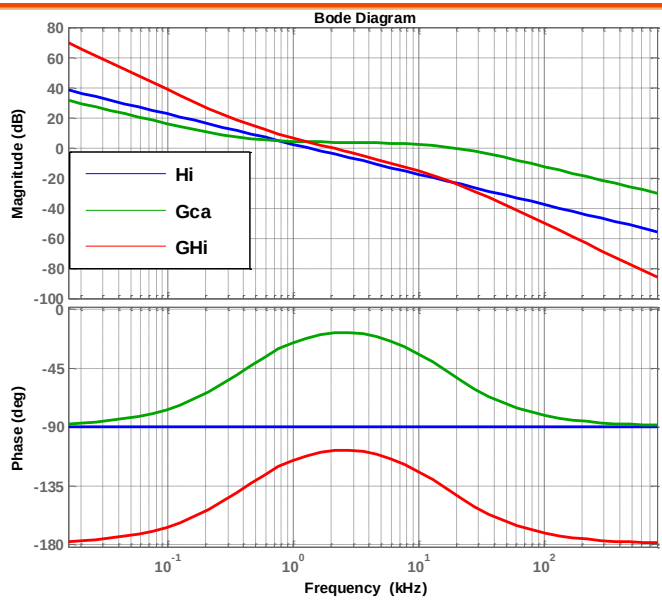


Figure 6.6 (a) Current loop

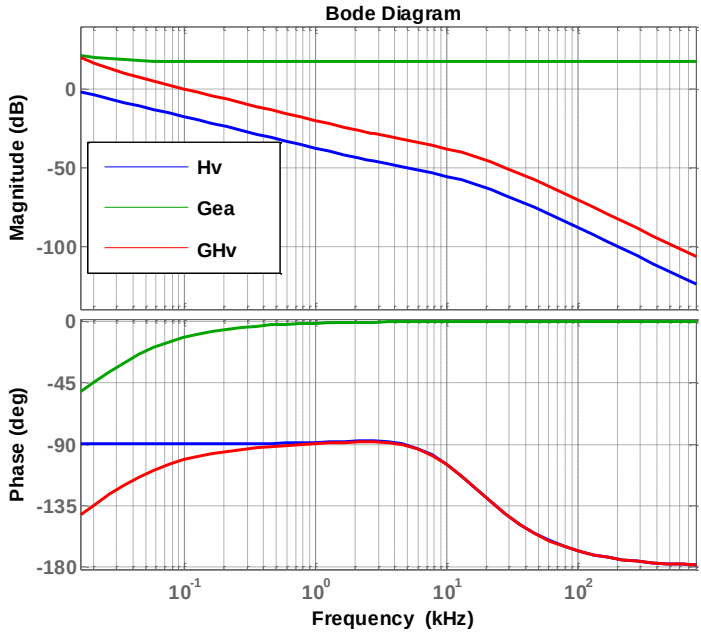


Figure 6.6 (b) Voltage loop

Figure 6.6 Bode plot of control loop utilizing average current control

Circuit Simulation

The PSIM simulating circuit constructed by the previous design is shown in the figure 6.7 with its simulating result as the figure 6.8 shown.

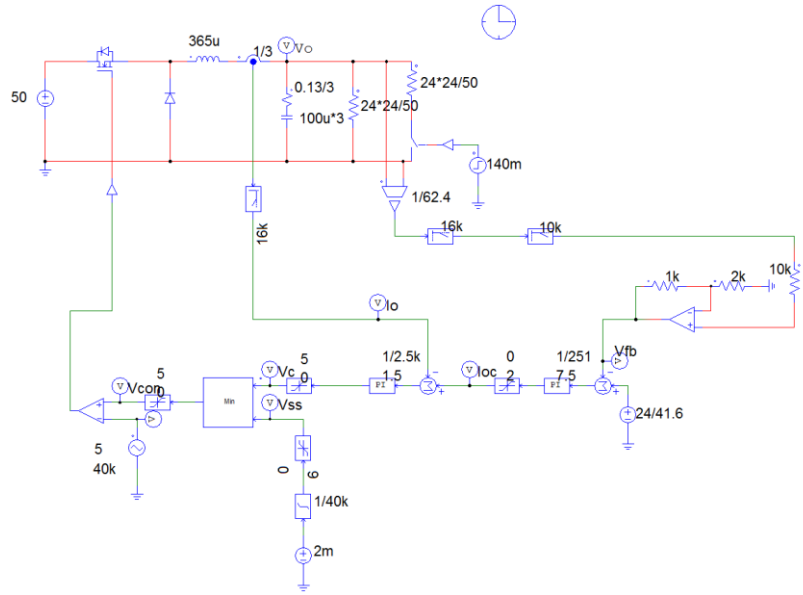


Figure 6.7 PSIM simulating circuit (buck3.psimsch)

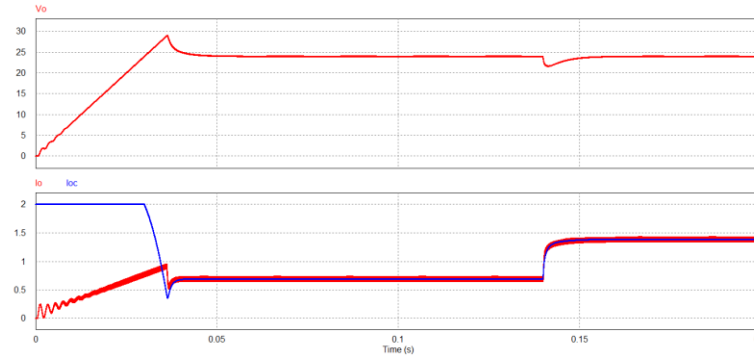


Figure 6.8 The simulating result of figure 6.7

SimCoder Program Layout

The program constructed by SimCoder is shown in the figure 6.9 with its simulating result, which is identical to analog simulation, as the figure 6.10 shown.

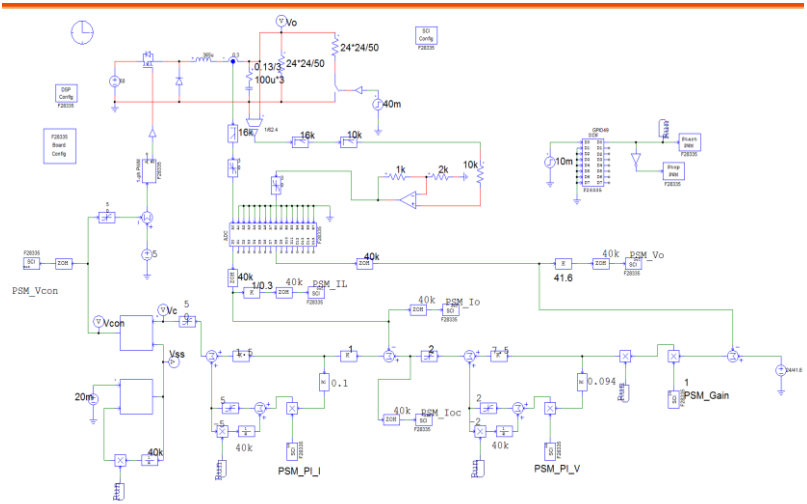


Figure 6.9 SimCoder program (Lab3.psimsch)

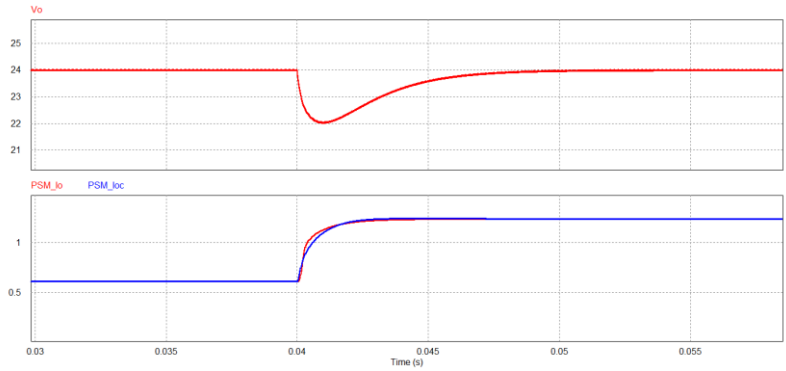


Figure 6.10 The simulating result of figure 6.9

Experiment Measurement

The experimental devices and teaching aid layout are illustrated as the figure 6.11. DC power supply, PSW 160-7.2, connects to the input terminal J201 of buck teaching aid. The output terminal J202 connects to the DC electrical load, PEL-2040, and utilizes constant resistive mode. The output voltage and inductive current measured waveform are shown in the figure 6.12.

Figure 6.11 Experiment devices layout

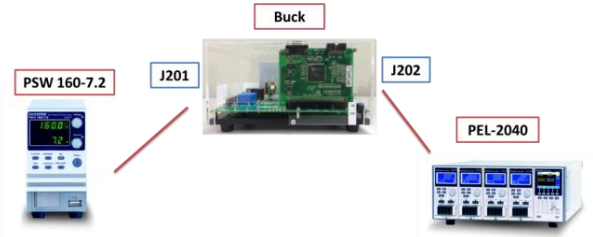
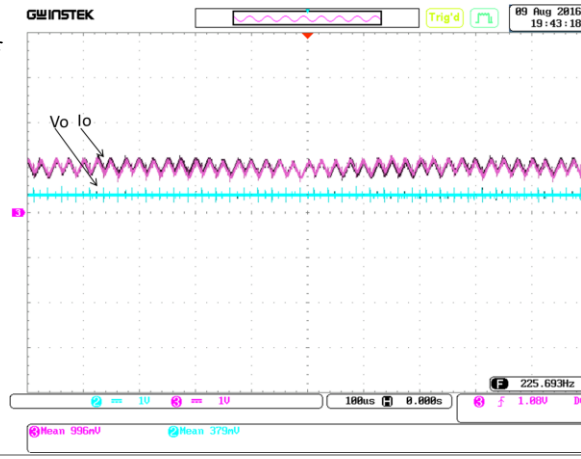


Figure 6.12 Output voltage of converter and measured waveform of inductive current



Experiment 4 – Maximum Power Point Tracking Control

The purpose of experiment

To learn the maximum powe r point tracking control method of PV module including the general MPPT control method, hardware layout and the control program of pertube and observe method, incremental conductance method, etc.

The principle of experiment

Introduction of PV module charateristics

The output characteristic of photovoltaic (PV) module is neither constant voltage, nor constant current, and its output power changes in light of working point. Therefore, it suggests adjusting working point at all times to make power generation reached the maximum, which is called maximum power point tracking (MPPT). We further elaborate the characteristics of PV module in the following contents as the reference for MIPPT controller design.

PV module is composed of several PV serial-parallels. Once PV is exposed to light, a current source carrying load power is generated. Refer to the figure 4.1 for PV equivalent circuit where I_{ph} indicates the current generated by PV, while D_j indicates a P-N junction diode. R_{sh} and R_s stand for the equivalent serial and parallel resistors of internal material, respectively. In general, during analysis process, value of R_{sh} is quite large, whilst value of Rs is

quite small. Therefore, in order to simplify analysis process, the values of R_{sh} and R_s can be omitted. I_p and V_p, on the other hand, represent the output current and voltage of PV, respectively.

The equivalent circuit of PV module, the characteristics of P-N junction diode and the output current of PV module can be represented in the following mathematical equation (7.1):

$$I_{pv} = n_p I_{ph} - n_p I_{sat}\left[\exp\left(\frac{q}{kTA}\frac{V_{pv}}{n_s}\right) - 1\right] \quad (7.1)$$

V_{ph}: It indicates PV output voltage (V)

I_{pv}: It indicates PV output current (A)

T: It indicates PV surface temperature (°K)

A: It indicates PV ideal factor (A=1~5)

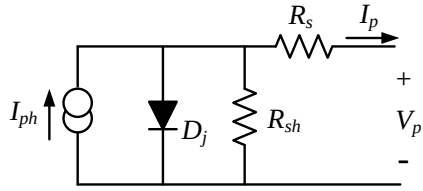
q: It indicates amount of electricity of an electron (1.6×10^{-19}C)

k: It indicates Boltzmann constant (1.38×10^{-23} J/°K)

n_p: It indicates number of PV battery in parallel

n_s: It indicates number of PV battery in serial

Figure 7.1 PV equivalent circuit



I_{sat}: It indicates reverse saturation current of solar photovoltaic board and its mathematical relation is shown as follows:

$$I_{sat} = I_{rr}\left(\frac{T}{T_r}\right)^3 \cdot \exp\left[\frac{qE_{gap}}{kA}\left(\frac{1}{T_r} - \frac{1}{T}\right)\right] \quad (7.2)$$

T_r: It indicates PV reference temperature (°K)

I_{rr}: It indicates reverse saturation current (A) when PV reference temperature is Tr

E_{gap}: It indicates the required energy when semiconductor material crosses energy gap

$$E_g = 1.16 - 7.02 \times 10^{-4} \frac{T^2}{T - 1108} \qquad (7.3)$$

$$I_{ph} = [I_{scr} + \alpha(T - T_r)] \frac{S}{100}$$

I_{scr}: It indicates the short-circuit current (A) when PV battery operates under the sunshine condition of reference temperature and 1kW/m²

α: It indicates temperature coefficient of PV module short-circuit current

S: It indicates amount of insolation (kW/m²)

Power output (P) can be calculated via the (7.3) as follows:

$$P_{pv} = V_{pv} \times I_{pv} \qquad (7.4)$$

We can obtain the following when multiplied by the (7.1) and (7.3):

$$P_{pv} = n_p V_{pv} I_{ph} - n_p I_{sat} V_{ph} [\exp(\frac{q}{ktA} \frac{V_{pv}}{n_s}) - 1] \qquad (7.5)$$

The characteristics of PV module can be realized via the previous equation (7.5), which depicts the curve diagram of output voltage, current and power from PV module under the circumstances of different amount of insolation and fluctuation of PV board surface temperature. Refer to the figure 7.1 for the 75W PV module manufactured by Shell:

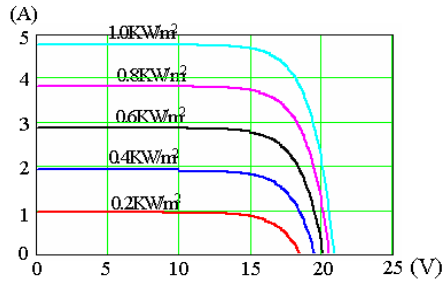
Electric Characteristics	Spec
Rated Power Output (W)	75
Rated Current (A)	4.4
Rated Voltage (V)	17.0
Short-circuit Current I_{sc} (A)	4.8
Open-circuit Voltage V_{oc} (V)	21.7

Normal Operating Temperature NOTC (˚C)	45.2
Short-circuit Current Temperature Coefficient Ki (mA/˚C)	2.06
Open-circuit Voltage Temperature Coefficient (V/˚C)	-0.77

Table 7.1 The specification of Shell SQ75 PV

When temperature is 25˚C and amount of insolation is 1KW/m², the electric characteristics is represented as the figure 7.1. The output voltage and current and output voltage and power curve diagram under vaired amount of insolation are indicated within the figure 7.2(a) and 7.2(b), respectively. Also, the output voltage and current and output voltage and power curve diagram under vaired temperature are indicated within the figure 7.3(a) and 7.3(b), respectively.

Figure 7.2 Under the constant environmental temperature (25°C) with varied amount of insolation (a) I_P-V_P characteristic curve



(b) P-V_P characteristic curve

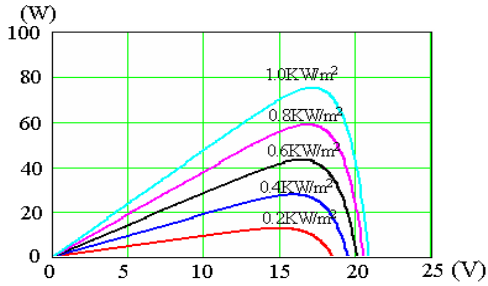
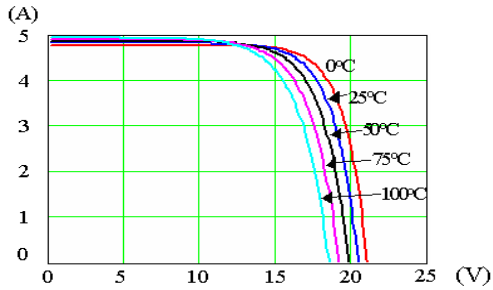
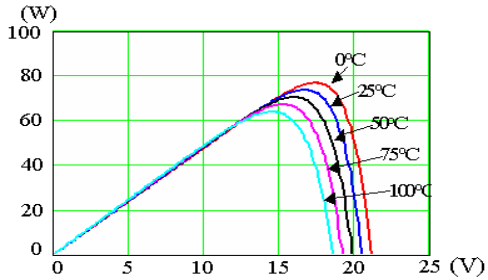


Figure 7.3 Under the constant amount of insolation (1kW/m^2) with varied environmental temperature (a) I_P-V_P characteristic curve



(b) P-V_P characteristic curve



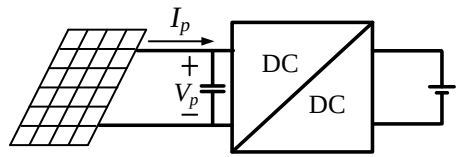
Control method of PV converter

We may understand from the characteristically simulating curve of PV module that the 2 reasons affecting power output of PV module are insolation density and environmental temperature, individually. Along with fluctuation of weather, both temperature and insolation density change at any time; therefore, in an attempt to output the maximum power of PV module, it is necessary to control the power converter of PV module when boosting electrical efficiency of PV module to gain the maximum power output in varied working environment, which is the control method called MPPT technology.

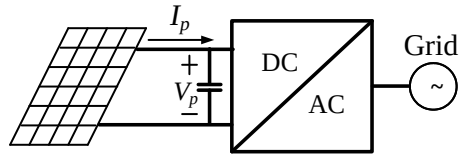
The power converter architectures of three typical PV power systems are illustrated in the figure 7.4. The figure 7.4(a) indicates a battery charging system, whilst both the figure 7.4(b) and (c) indicate grid-interconnected system. The MPPT control of all the three systems can be achieved by controlling input voltage V_p and input current I_p of PV module converter. All you need to do is to

calculate the voltage of maximum power point of PV module as command, and make it operated, via voltage loop control, in the MTTP point.

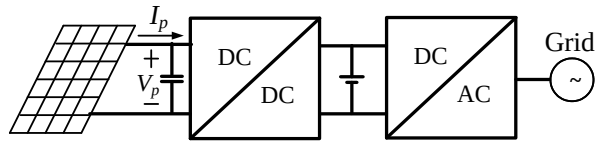
Figure 7.4 All kinds of PV module power converter system architecture (a) Battery charging system



(b) Grid-interconnected system

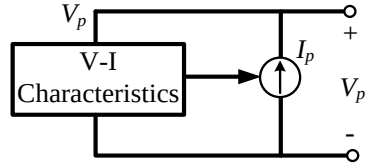


(c) Two-level grid-interconnected system

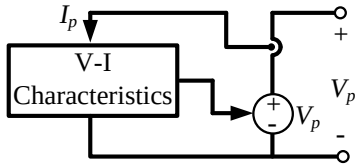


We can, from the characteristically simulating curve of PV module, realize that PV module is neither voltage source nor current source. When applying to the combination analysis of voltage source converter as diversified converters in the figure 7.4, PV module is regarded as a single current source, of which equivalent circuit is shown as the figure 7.5 (a). On the contrary, when applying to current source converter, PV module is viewed as a single voltage source, of which equivalent circuit is illustrated as the figure 7.5 (b).

Figure 7.5 Equivalent circuit of PV module (a) converter for voltage source



(b) converter for current source



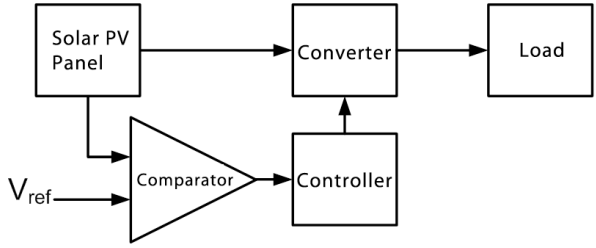
MPPT Method

Several methods, speaking to MPPT method, were raised previously including the following 6 methods: voltage feedback method, power feedback method, pertube and observe method, incremental conductance method, linear approximation method and practical measurement, all of which share the similar concept in that they utilize PV output voltage or current or both to proceed to the maximum power tracking method. The main difference among them is the dissimilarity of judgement and realization of maximum power point. Refer to the following descriptions for MPPT control method.

1. Voltage feedback method

As the figure 7.6 shown, voltage feedback method is the simplest way because the voltage scale of maximum power point under the known insolation density and temperature can reach, via adjustment of PV module output voltage, the goal of the maximum power tracking. While the major defect is energy loss when system can Not track the latest maximum power point automatically during environmental change.

Figure 7.6 Voltage feedback method block diagram



2. Power feedback method

As the figure 7.7 shown, power feedback method is quite similar to voltage feedback method. Due to the fact that voltage feedback method is Not able to track the latest power point under the fluctuating atmosphere, the judgement for change rate of output power to voltage is thus added in power feedback method to track the maximum power point even when atmosphere fluctuates. Compared with voltage feedback method, energy loss is mitigated with judgement for voltage change rate added, though. We can summarize that it is greatly superior to, in terms of efficieny promotion, voltage feedback method.

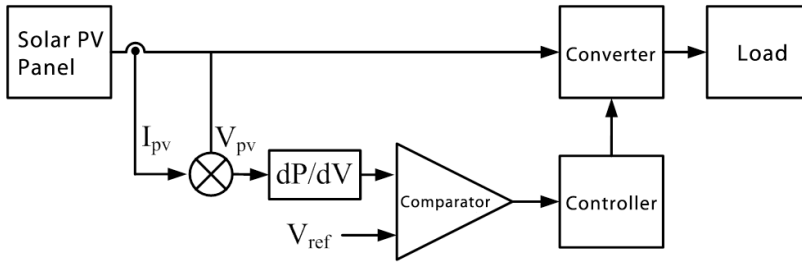


Figure 7.7 Power feedback method block diagram

3. Pertube and Observe method

As the figure 7.8 shown, the pertube and observe method, with simple structure, only needs to measure output voltage and current of PV module. It is, identical to the power feedback method, widely applied to the MPPT method for PV module.

The pertube and observe method, via periodically increasing or decreasing load scale, changes the output voltage and power of PV module; that is, it changes the working point of PV board in characteristic curve, and not only observe but compare the scales of output voltage and output power before and after the load changes, to determine the next move for load increase or decrease.

If pertubatioin causes the power output of PV module to increase more than previous, then properly increase or decrease load toward the same direction in the next cycle to make power output increased consecutively; by contrast, when power output decreases

less than previous, it is required to change the direction of load in the next cycle. Through repeating comparison of pertube and observe, PV module can reach the maximum power point, which is the very principle of the pertube and observe method. If response is faster, the voltage fluctuation will be more intense; that is to say, always be aware of the trade-off between accuracy and response speed.

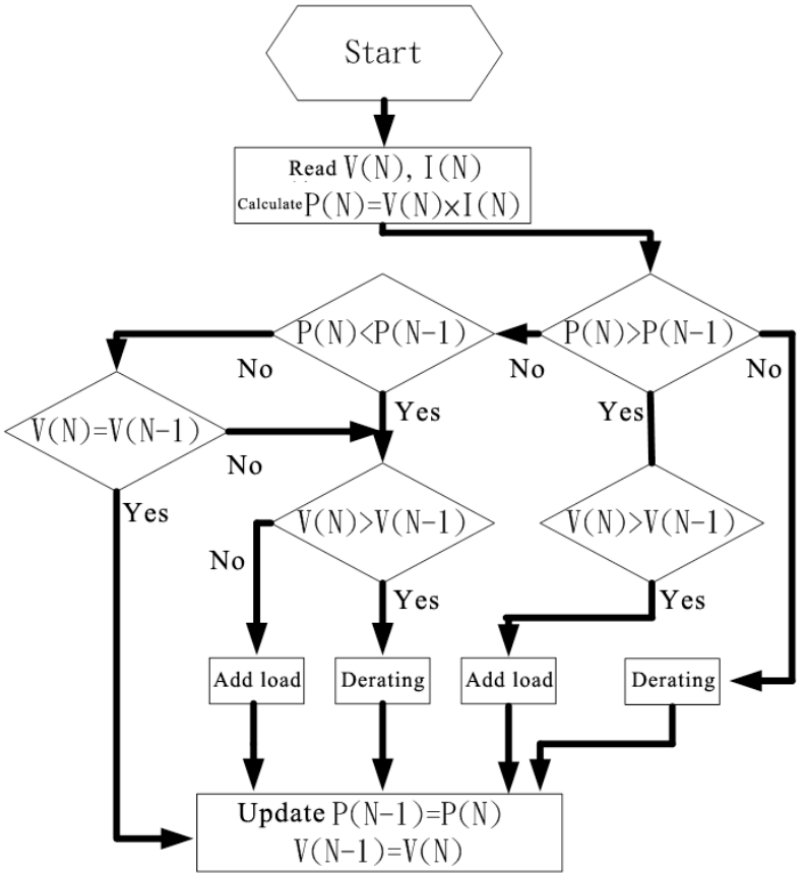


Figure 7.8 Control block diagram of pertube and observe method

4. (4) Increamental Conductance method (INC)

As the figure 7.9 shown, identical with the principle of power feedback method, the increamental conductance method produces

the following equation mainly adapted from the determine statement $dP_{pv}/dV = 0$:

$$\frac{dP_{pv}}{dV_{pv}} = \frac{d(I_{pv}V_{pv})}{dV} = I + V\frac{dI}{dV} = 0 \tag{7.9}$$

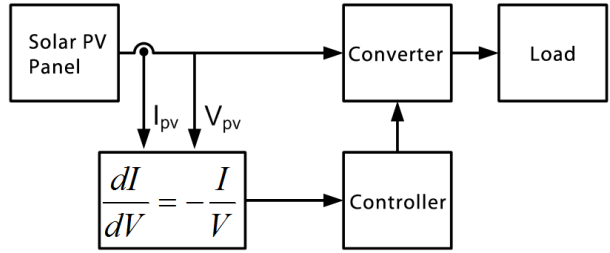
We may obtain the follows after arranging the equation (7.9):

$$\frac{dI}{dV} = -\frac{I}{V} \tag{7.10}$$

From the equation (7.10), *dI* indicates current changes measured before and after increment, whereas *dV* represents voltage changes measured before and after increment. The next change volume can be determined by measuring incremental value *dI/dV* and conductance *I/V* of transient PV. When incremental value and conductance have the relation of equivalently left and right side, the maximum power point is therefore met and next perturbation will be discarded, which is the principle of incremental conductance method.

Incremental conductance method, via altering output voltage of PV module, reaches the highest power tracking to meet the maximum power point, which is different from the logic of the pertube and observe method and is able to avoid the issue of fluctuation in the proximity of the maximum power tracking from the pertube and observe method.

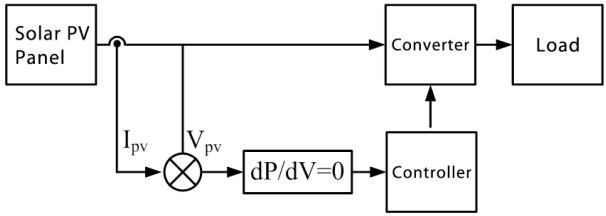
Figure 7.9 Block diagram of incremental conductance method



5. Linear Approximation method

As the figure 7.10 shown, linear approximation method, of which the basic principle utilizes the logical determine statement $dP_{pv}/dV = 0$, uses a linear to similize the maximum power point in various amounts of insolation of PV module under fixed temperature, further reaching the maximum power tracking via controlling the output current of PV module within the linear. Also, it infers, based on mathematics module, the approximate linear on the maximum power point of PV module, by doing which the accuracy of each parameter and component aging will deteriorate the accuracy of linear approximation method.

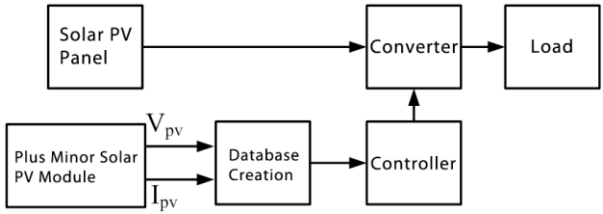
Figure 7.10 Block diagram of linear approximation method



6. Actual Measurement method

As the figure 7.11 shown, actual measurement method mainly utilizes the additional PV module to measure open-circuit voltage and short-circuit current of PV board periodically, further establishing the voltage and current of the maximum power point under insolation and temperature of the atmeospheric condition. Along with the control circuit, PV module working under the voltage and current can reach the precisely maximum power point. However, since this is only applicable to area with stable weather, it needs to establish database by remeasurement when environment changes.

Figure 7.11 Block diagram of actual measurement method



The principle of the maximum power tracking and the comparison of pros and cons are displayed as the following table 7.2:

MPPT Method	Working Principle	Pros	Cons
Voltage feedback method	Refer to the PV board characteristics by prior measurement	Simple architecture with low cost	Not available for auto tracking the latest maximum power point
Power feedback method	Indentical to the voltage feedback method, it increases power output to judge voltage change	Lessen energy consumption whilst increase the overall efficiency	Identical to the voltage feedback method, it has larger calculation amounts
Pertube and observe method	Increase or decrease load in cycle and observe power and voltage changes to determine load increase or decrease in the next step	Easy implement with simple architecture and principle	Fluctuating power loss occurs on the maximum power point
Incremental conductance method	Utilize the relation between PV *dI/dV* and *I/V* to determine incremental value	It lessens fluctuating power loss compared with pertube and observe method	It requests highly precise accuracy for measurement with wider errors in actual application

Linear approximation method	Via $dP/dV=0$, it utilizes a linear to similize PV maximum power point	Easy implement with simple architecture	Accuracy deteriorates when PV board and components have aged
Actual measurement method	Externally connect to a PC board to measure characteristics and establish reference model for control	Prevent PV from aging that deteriorates the accuracy of model	It requires remeasurement to establish database when environment changes

Table 7.2 The principle of the maximum power tracking and the comparison of pros and cons

7. Enhanced Incremental Conductance (INC) MPPT controls

As the figure 4.12 shown, this experiment regards the output curve of voltage and current of PV module as equivalent model to connect the voltage source VS, which adjusts in accord with brightness, with an internal resistor RS in series, further providing power to a DC-DC converter, which acts as a load RL here. From this experiment, power output Po from PV module under varied loads can be expatiated as below:

$$P_o = V_o \times I_o = V_o \times \frac{V_S - V_o}{R_S} = \frac{V_o \cdot V_S - V_o^2}{R_S} \qquad (7.11)$$

V_o represents output voltage, whilst I_o stands for output current. The output relation of voltage minus power is the curve *a* of figure 4.13 with the maximum power point occurring as the following:

$$\frac{dP_o}{dV_o} = \frac{V_S}{R_S} - 2\frac{V_o}{R_S} = 0 \Rightarrow V_o = \frac{V_S}{2} \qquad (7.12)$$

Therefore, when output voltage of PV module is $V_s/2$, the maximum power output is met. In addition, we obtain the follows based on voltage divider rule:

$$V_o = V_S\left(\frac{R_L}{R_S + R_L}\right) = \frac{V_S}{2} \Rightarrow R_L = R_S \quad (7.13)$$

It proves that when R_L is equal to R_S, PV module has the maximum power output, which is the impedance matching theory. In practice, the V_s and R_s values of PV module, as the curves from previous figures 4.2 and 4.3, dynamically change in accordance with different working points even under the identical insolation, the R_L value, therefore, will change dynamically as well. Nevertheless, the maximum power theory of voltage divider from the above 2 resistors is still applicable.

Figure 7.12 Equivalent circuit model of PV module

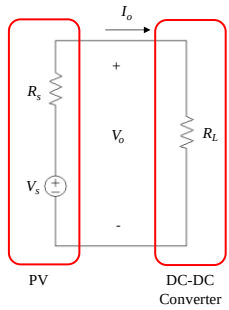
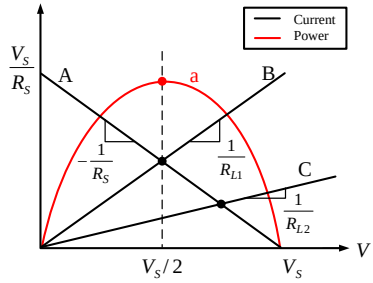


Figure 7.13 Relation of voltage, current and resistor of PV module



The MPPT method of PV module adopted by this experiment as the figure 7.14 shown utilizes the voltage current obtained from the operation of 2 load values, via slope method from the 2 points, to acquire internal resistance of PV module, as the figure 4.14 shown. First operate the DC-DC converter in varied duty cycle rate (D), which is equal to 2 varied load values. The input voltage current V_1, I_1 are detected when operating the first conductivity D1 followed by the V_2, I_2 detected when operating the second conductivity D2

with an interval ΔD of D1. And go through the following equation after acquiring the above 2 points:

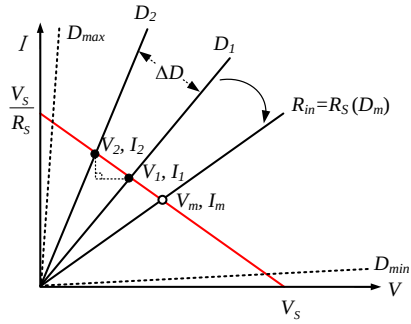
$$R_S = -\frac{V_1 - V_2}{I_1 - I_2} \tag{7.14}$$

The internal resistance R_S of PV module can be obtained. Also, it is viable to use linear regression method to calculate the internal resistance value after measuring several voltage current values.

Measure input voltage and current values to calculate input resistance R_{in} followed by adjusting conductivity to alter input resistance that will be almost identical to the internal resistance R_S or have a gap of minor value with the internal resistance R_S.

After the program has been operated for a course of period ($t>T$, t represents the endured time, whilst T stands for the set reexecuted time), it will remeasure input resistance to reach the $R_S=R_L$, which indicates the maximum power point. If regarding $1/R_s$ as the incremental conductance, then the resistance matching method is in fact equal to the previous INC MPPT method in terms of power efficiency.

Figure 7.14 PV resistance matching MPPT method



Although the maximum power point can be tracked based on the method of figure 7.14, the DC-DC converter, due to the duty cycle change, must experience a period of time for steady state of voltage followed by calculation of next point so that there will be no more misjudgement on direction. Therefore, the speed of MPPT will be limited by the speed of open-circuit response.

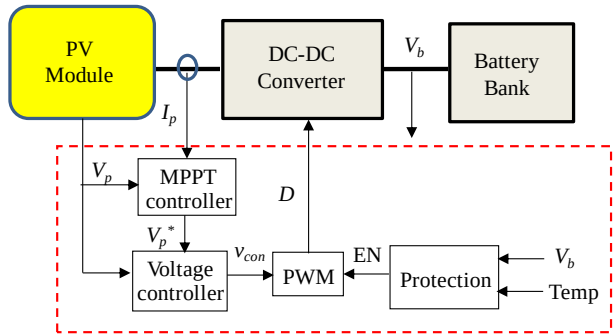
In order to boost speed of MPPT, it is required to shorten the time of reaching steady state after working point changes. The control architecture of our DC-DC converter, as the figure 7.15 shown,

adopts the dual-loop control and the outer loop is MPPT controller, of which sensing input voltage and current are usded for MPPT control to produce the voltage command (V_{p*}) of PV module.

Inner loop is voltage control loop, which utilizes the comparison between voltage command and feedback input voltage (V_p) followed by adjustment from error amplifier to acquire duty cycle of switch.

The control architecture with voltage loop offers a shorter period of time to reach steady state after voltage adjustment than that after direct change of duty cycle voltage. Therefore, it largely improves response speed and makes MPPT tracking more precise.

Figure 7.15 Control architectute of DC-DC converter



The tracking method of MPPT still utilizes the previous resistance matching method, which changes the adjustment of working point to voltage as the figure 4.15 shown.

It starts from setting initial value of voltage command as open-circuit voltage followed by entering the loop with cycle T and sampling voltage and current (V_1 *and* I_1) of PV module. The (V_2*), of which * represents command, will be then acquired by changing voltage command. The changed value of voltage command is -ΔV by default, but will become +ΔV or -ΔV after next cycle T depending on previous changed value of sampling voltage. If V_2*, after change, is greater than the default highest value V_{max} of PV module, the increased value turns out -ΔV. By contrast, if V_2*, after change, is smaller than the default lowest value V_{mix} of PV module, the increased value turns out +ΔV.

After that, it samples V_2 and I_2, and calculates R_S value via ($V1$, $I1$) and (V_2, I_2). Furthermore, it enters the loop of cycle time ΔT, and

continuously utilizes sensing (V_1, I_1) to calculate R_L value followed by adjusting voltage command via comparison between R_S *and* R_L values. When $RS \geq RL$, ΔV will be increased to amplify R_L for voltage adjustment; in contrast, when $R_S < R_L$, ΔV will be decreased to lower down R_L for voltage adjustment so that RL is able to track R_S. Before entering next loop of time T, it repeats the previously metioned process until the certain time cycle T.

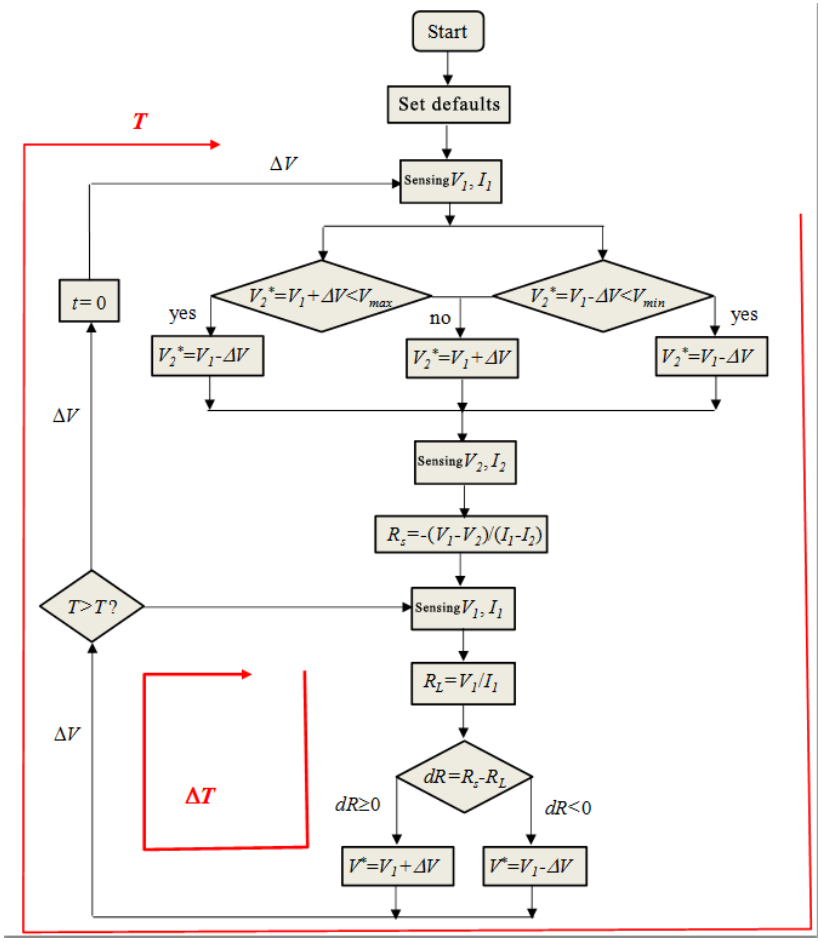


Figure 7.16 The procedure of MPPT method program utilizing dual-loop control resistance matching method

Circuit Simulation

The buck converter is designed in accordance with the above MPPT control method and the previous experiment. The P&O MPPT control circuit constructed by PSIM circuit is shown as the figure 7.17. The MPPT program, of which ΔT is equal to 1/200Hz, is shown as the appendixed program in the figure 7.17. The simulating result, in which the maximum power point (V_{mp}=32V, I_{mp}=3A, P_{mp}=96W) is precisely tracked in a quick manner, is shown as the figure 7.18.

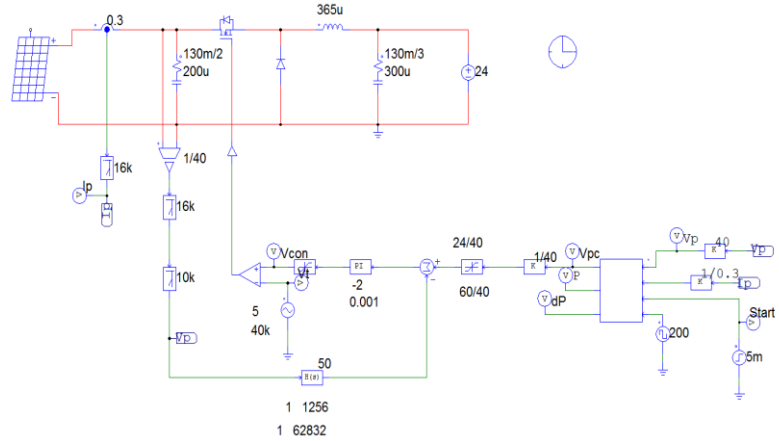


Figure 7.16 The simulating circuit (buck_4_P&O.psimsch) utilizing P&O MPPT control method

P&O MPPT program (figure 7.16)

```
static int n;
static double ymax = 50;
static double ymin = 24;
static double Vp, Ip, Vp1, Ip1, P, P1, dP, dv=1, Vpc, Vpc1, start, CLK,
CLK1;
start = x3;
Vp = x1;
Ip = x2;
CLK = x4;
P = Vp * Ip;
if (start <1)
{
```

```
Vpc = Vp - dv;
CLK1 = CLK;
}
if (start >0)
{
      if((CLK-CLK1)==1)
   {
        if (P > P1)
      {
         if (Vp > Vp1)
            { Vpc = Vp + dv; }
         else
            { Vpc = Vp - dv;  }
       }
   else
       {
         if (Vp > Vp1)
            { Vpc = Vp - dv; }
         else
            { Vpc = Vp + dv;  }
       }
   if (Vpc>=ymax)
     { Vpc= Vp - dv;}
   if (Vpc<=ymin)
     { Vpc= Vp + 3 * dv;}
    Vp1 = Vp;
    Vpc1 = Vpc;
    dP = P - P1;
    P1 = P;
     }
 CLK1 = CLK;
 }
y1=Vpc;
y2 = P;
y3 = dP;
```

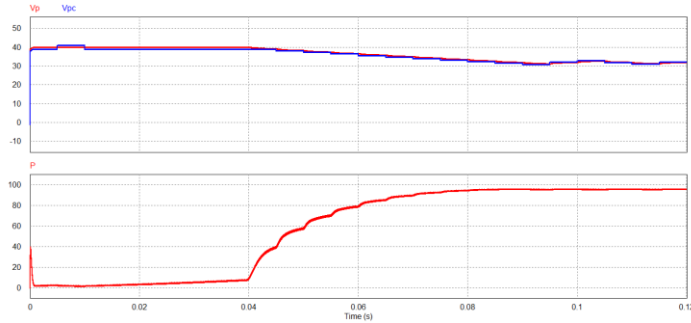


Figure 7.17 The simulating result from figure 7.16

The INC MPPT control circuit constructed by PSIM circuit is shown as the figure 7.18. The MPPT program, of which the frequency is 200Hz, is shown as the appendixed program in the figure 7.18. The simulating result, in which R_L and R_s can rapidly follow and thus precisely track the maximum power point (V_{mp}=32V, I_{mp}=3A, P_{mp}=96W), is shown as the figure 7.19.

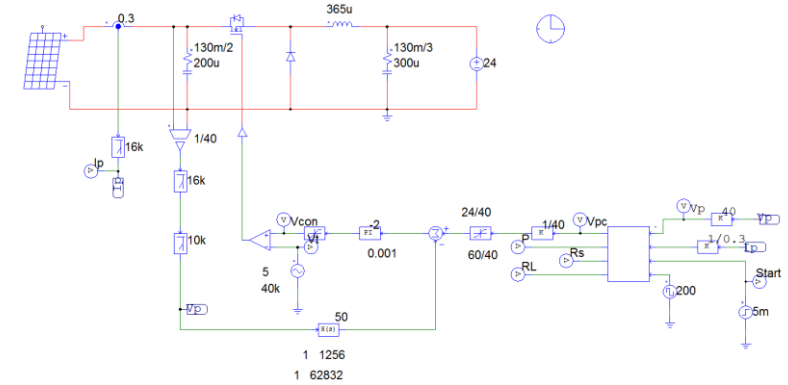


Figure 7.18 The simulating circuit (buck_4_INC.psimsch) utilizing INC MPPT control method

INC MPPT program (figure 7.18)

```
static double ymin = 24;
static double Vp, Ip, Vp1, Ip1, P, P1, Rs, RL, dV, dI, dv=1, Vpc, Vpc1, start,
CLK, CLK1;
start = x3;
```

```
Vp = x1;
Ip = x2;
CLK = x4;
P = Vp * Ip;
if (start <1)
{
Vpc = Vp - dv;
CLK1 = CLK;
}
if (start >0)
{
      if((CLK-CLK1)==1)
   {
      dV = Vp - Vp1;
      dI  = Ip - Ip1;
      Rs = dV/dI;
      if (Rs < 0)
        {  Rs = -Rs;
          if (Rs >= 2000)
          {Rs = 2000;}
        }
       RL = Vp/Ip;
       if (RL >= 5000)
         {RL = 5000;}
       if (Rs> RL)
       { Vpc = Vp + dv;}
       if (Rs <= RL)
        { Vpc = Vp - dv;}
        if (Vpc>=ymax)
        { Vpc= Vp - dv;}
         if (Vpc<=ymin)
         { Vpc= Vp + 3 * dv;}
        Vp1 = Vp;
        Vpc1 = Vpc;
        Ip1 = Ip;
        }
  CLK1 = CLK;
 }
y1=Vpc;
y2 = P;
y3 = Rs;
y4 = RL;
```

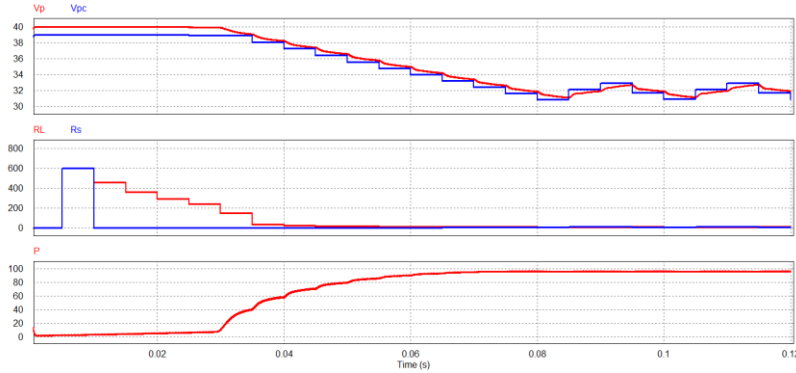


Figure 7.19 The simulating result from figure 7.18

SimCoder Program Layout

As the figure 7.20 shown, P&O MPPT control program, which is constructed by SimCoder circuit, is digitalized in circuit based on the figure 7.16. The MPPT program, of which the frequency is 200Hz, is shown as the appendixed program in the figure 7.20.

As the figure 7.21 shown, the simulating result, which is identical to that of analog program (figure 7.17), precisely and promptly tracks the maximum power point (V_{mp}=32V, I_{mp}=3A, P_{mp}=96W).

It is noticeable that the figure 7.20 is only for simulation due to the fact that 200Hz adjusting frequency of MPPT is way to fast for general PV simulator. The actual program in practice is illustrated as the figure 7.22 where adjusting frequency of MPPT is set 1Hz, which is way to slow and difficult for confirming response by simulation. Hence, the figure 7.22 provides actual implementation only.

As the figure 7.22 displayed, MPPT program, compared with MPPT 200Hz program, has adjusted its step voltage, in accord with power fluctuation, to lower down the fluctuation in the proximity of MPPT point.

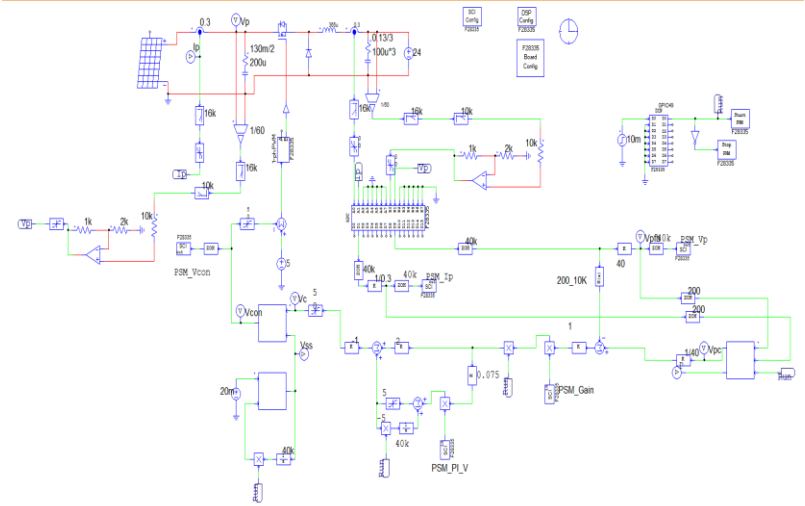


Figure 7.20 P&O MPPT control program constructed by SimCoder circuit

(Lab4_P&O.psimsch, for simulation only)

P&O MPPT program (figure 7.20)

```
static double ymax = 50;
static double ymin = 24;
static double Vp, Ip, Vp1, Ip1, P, P1, dv=1, Vpc, Vpc1, start;
start = x3;
Vp = x1;
Ip = x2;
P = Vp * Ip;
if (start <1)
{
Vpc = Vp - dv;
}
if (start >0)
{
        if (P >=P1)
      {
         if (Vp > Vp1)
            { Vpc = Vp + dv; }
         else
            { Vpc = Vp - dv;  }
       }
   else
       {
         if (Vp > Vp1)
            { Vpc = Vp - dv; }
         else
            { Vpc = Vp + dv;  }
       }
   if (Vpc>=ymax)
     { Vpc= Vp - 2 * dv;}
   if (Vpc<=ymin)
     { Vpc= Vp + 3 * dv;}
 P1 = P;
Vp1 = Vp;
Ip1 = Ip;
}
y1=Vpc;
y2 = P;
```

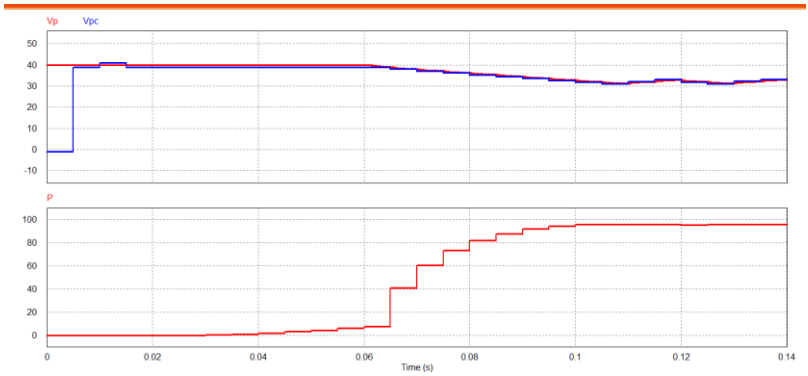


Figure 7.21 The simulating result from figure 7.20

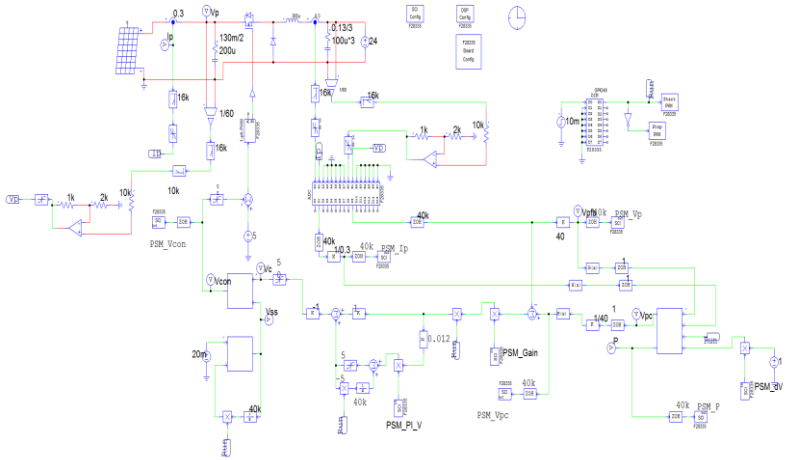


Figure 7.22 P&O MPPT control program constructed by SimCoder circuit

(Lab4_P&O_R.psimsch, for implementation only)

P&O MPPT program (Figure 7.22)

```
static double ymax = 50;
static double ymin = 24;
static double Vp, Ip, Vp1, Ip1, P, P1, dP, dv, Vpc, Vpc1, start;
start = x3;
Vp = x1;
Ip = x2;
P = Vp * Ip;
```

```
dv = x4;
if (start <1)
{
Vpc = Vp - dv;
}
if (start >0)
{
  dP=P-P1;
  if (dP<0)
    {dP = -dP;}
  if (dP>5)
    {dv = 0.5;}
  if ((dP<=5)&&(dP>2))
    {dv = 0.25;}
  if (dP<=2)
    {dv = 0.1;}
       if (P >=P1)
     {
        if (Vp > Vp1)
           { Vpc = Vp + dv; }
        else
           { Vpc = Vp - dv;  }
       }
   else
       {
        if (Vp > Vp1)
           { Vpc = Vp - dv; }
        else
           { Vpc = Vp + dv;  }
       }
    if (P<3)
       {Vpc = Vp - 1;}
  if (Vpc>=ymax)
    { Vpc= Vp - 2 * dv;}
  if (Vpc<=ymin)
    { Vpc= Vp + 3 * dv;}
 P1 = P;
Vp1 = Vp;
Ip1 = Ip;
}
y1=Vpc;
y2 = P;
```

As the figure 7.23 shown, INC MPPT control program, which is constructed by SimCoder circuit, is digitalized in circuit based on the figure 7.18. The MPPT program, of which the frequency is 200Hz, is shown as the appendixed program in the figure 7.23.

As the figure 7.24 shown, the simulating result, which is identical to that of analog program (figure 7.19), precisely and promptly tracks the maximum power point (V_{mp}=32V, I_{mp}=3A, P_{mp}=96W).

It is noticeable that the figure 7.23 is only for simulation due to the fact that 200Hz adjusting frequency of MPPT is way to fast for general PV simulator. The actual program in practice is illustrated as the figure 7.25 where adjusting frequency of MPPT is set 1Hz, which is way to slow and difficult for confirming response by simulation. Hence, the figure 7.25 provides actual implementation only.

As the figure 7.25 displayed, MPPT program, compared with MPPT 200Hz program, has adjusted its step voltage, in accord with power fluctuation, to lower down the fluctuation in the proximity of MPPT point.

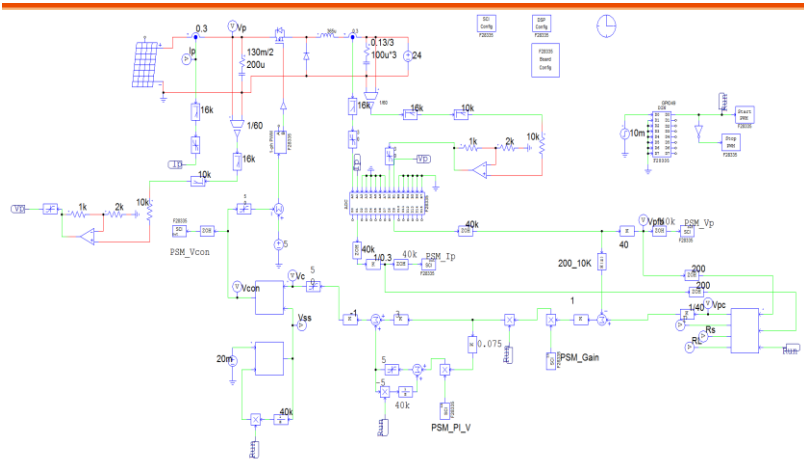


Figure 7.23 INC MPPT control program constructed by SimCoder circuit (Lab4_INC.psimsch, for simulation only)

INC MPPT program (Figure 7.23)

```
Static double ymax = 50;
static double ymin = 24;
```

```
static double Vp, Ip, Vp1, Ip1, P, dv=1, Vpc, Vpc1, dV, dI, Rs, RL, start;
start = x3;
Vp = x1;
Ip = x2;
P = Vp * Ip;
if (start <1)
{
Vpc = Vp - dv;
Ip1 = Ip - 0.01;
}
if (start >0)
{
      dV = Vp - Vp1;
      dI  = Ip - Ip1;
      Rs = dV/dI;
      if (Rs < 0)
        {  Rs = -Rs;
          if (Rs >= 2000)
          {Rs = 2000;}
        }
       RL = Vp/Ip;
       if (RL >= 5000)
         {RL = 5000;}
       if (Rs> RL)
       { Vpc = Vp + dv;}
      if (Rs <= RL)
       { Vpc = Vp - dv;}
       if (Vpc>=ymax)
       { Vpc= Vp - 2 * dv;}
        if (Vpc<=ymin)
        { Vpc= Vp + 3 * dv;}
       Vp1 = Vp;
       Vpc1 = Vpc;
       Ip1 = Ip;
  }
y1=Vpc;
y2 = P;
y3 = Rs;
y4 = RL;
```

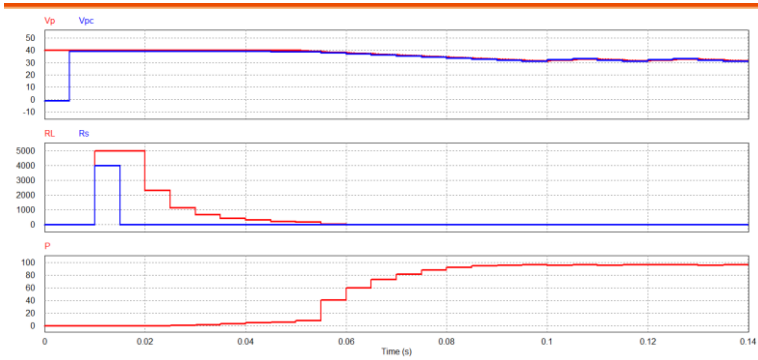


Figure 7.24 The simulating result from figure 7.23

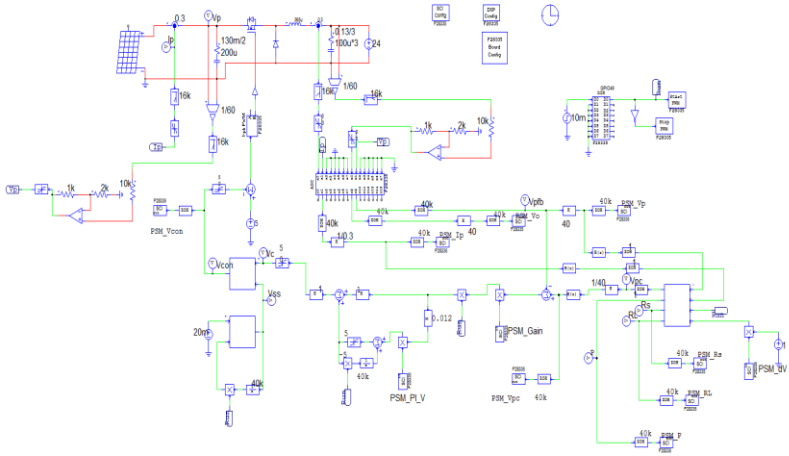


Figure 7.25 INC MPPT control program constructed by SimCoder circuit (Lab4_INC_R.psimsch, for implementation only)

INC MPPT program (Figure 7.25)

```
static double ymax = 50;
static double ymin = 24;
static double Vp, Ip, Vp1, Ip1, P, P1, dP, dv, Vpc, Vpc1, dV, dI, Rs, RL, Rs1,
Rs2, start;
start = x3;
Vp = x1;
Ip = x2;
dv = x4;
P = Vp * Ip;
if (start <1)
```

```
{
Vpc = Vp - dv;
Ip1 = Ip - 0.01;
}
if (start >0)
{
  dP=P-P1;
  if (dP<0)
    {dP = -dP;}
  if (dP>5)
    {dv = 0.75;}
  if ((dP<=5)&&(dP>2))
    {dv = 0.3;}
   if (dP<=2)
    {dv = 0.2;}
       dV = Vp - Vp1;
      dI  = Ip - Ip1;
      if (dI<0)
      { dI = -dI;}
      if (dI<0.001)
      { dI = 0.001;}
      Rs = dV/dI;
      if (Rs < 0)
        {  Rs = -Rs;
          if (Rs >= 2000)
          {Rs = 2000;}
        }
        Rs = (Rs2 + Rs1 + Rs)/3;
        RL = Vp/Ip;
       if (RL >= 5000)
         {RL = 5000;}
       if (Rs> RL)
      { Vpc = Vp + dv;}
      if (Rs <= RL)
       { Vpc = Vp - dv;}
       if (P<3)
        {Vpc = Vp - 1;}
       if (Vpc>=ymax)
       { Vpc= Vp - 2 * dv;}
        if (Vpc<=ymin)
        { Vpc= Vp + dv;}
       Vp1 = Vp;
       Vpc1 = Vpc;
       Ip1 = Ip;
```

```
        Rs2 = Rs1;
        Rs1 = Rs;
        P1 = P;
      }
y1=Vpc;
y2 = P;
y3 = Rs;
y4 = RL;
```

Experiment Measurement

The experimental devices and teaching aid layout are illustrated as the figure 7.26. DC power supply, PSW 160-7.2, connects to the input terminal J201 of buck converter teaching aid. The output terminal J202 connects to electronic load PEL-2040 and utilizes constant voltage mode. The waveforms of both P-V and I-V of MPPT displayed by Labview are indicated in the figure 7.27.

Figure 7.26

Experiment devices layout

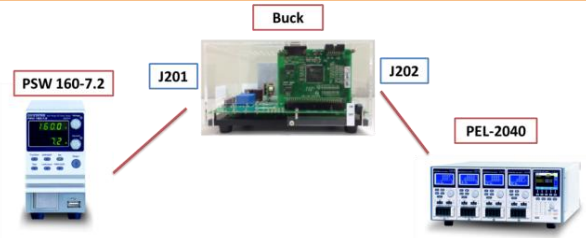
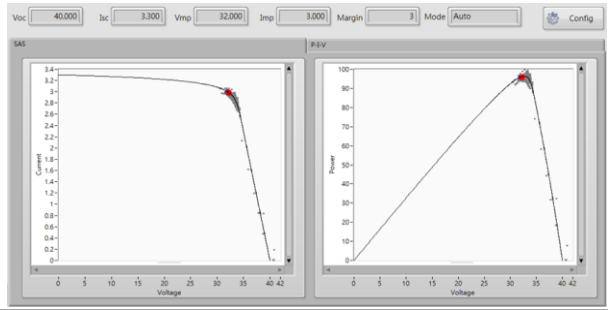


Figure 7.27

P-V and I-V waveforms of MPPT



Experiment 5 – PV Charger

The purpose of experiment

To learn the control method for PV charger including the 3-level charging control method for battery, the hybrid of MPPT control and charging control method, the hardware layout and control program composition, etc.

The principle of experiment

Working mode of PV charger system

The three working modes of PV charging system are shown within the figure 8.1. The MPPT mode, as the figure 8.1(a) displayed, in which when electricity of PV module is insufficient to supply load or charge, the insufficient part will be compensated by battery.

The partial charging mode, as the figure 8.1(b) displayed, in which when electricity of PV module is sufficient to supply load, and the superfluous electricity, however, is not enough to charge battery by the maximum charging current. The above 2 modes are exactly operated in the maximum power point.

The MPPT offset mode, as the figure 8.1 (c) displayed, in which when PV module operates in the maximum power point, the overall output electricity is greater than the requirement of both load and battery. In order to strike a balance of electricity, it requires to lessen the overall output electricity of PV module, and PV module must be away from the maximum power point to reduce electricity produced so that electrical balance can be properly achieved.

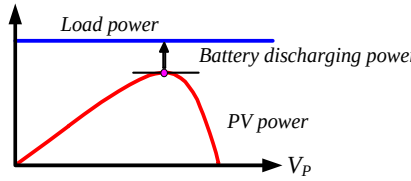
Figure 8.1

PV charging system working mode

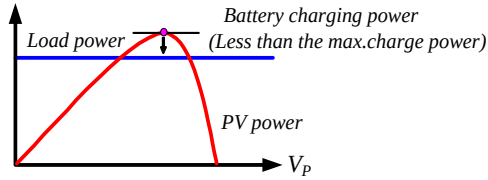
a. MPPT mode

b. Partial charing mode

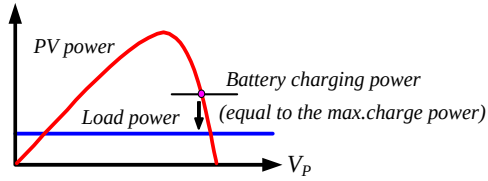
c. MPPT offset mode



(a)



(b)



(c)

Control Architecture

In order to realize the previous working mode, PV charging system, which controls architecture layout as the figure 8.2 shown, utilizes dual-loop control where the outer loop is charge control loop and inner loop includes MPPT control loop and PV voltage control loop. The principle of control is as follows:

Firstly, it samples battery voltage (V_b) and battery maximum voltage command (V_b*) for comparison, and the error can, via PI controller and positive limiter, acquire charging current command (I_b*). When battery voltage not reaches the maximum voltage command yet, the limiter is used to set the maximum charging current. When battery voltage is close to the maximum voltage command, limiter will enter the linear zone so that charging current

command will be reduced and the maximum voltage command level for battery will ultimately met and the charging current will provide power consumption for battery only. By the method above, it helps achieve constant-current charge, constant-voltage charge and floating charge, all of which are 3-level charge with result of battery life extension.

Compare the charging current command (I_b*) produced from PI voltage controller with battery current (I_b). When I_b is greater than I_b*, the error creates, via PI controller and zero-positive limiter, a voltage command (V_L), which will affect the maximum power point by moving it toward the right-side curve. Also, output voltage of PV module will be enhanced and power output by PV module will be the converged requirement of load and battery so that electrical balanced will be met, which occurs in the MPPT offset mode.

On the contrary, when I_b is smaller than I_b*, the error, via PI controller and zero-positive limiter, will become zero. Therefore, charging loop will be not able to influence voltage command (V_P*)) produced by MPPT. That is to say, output voltage command of solar energy is determined by MPPT controller, the MPPT mode and, therefore, the partial charging mode of PV module are operated under the state of maximum power point.

Based on the previous method, the strategic setting of 3-level charging for the experiment, where $I_{ch,max}$ is the maximum charging current set by battery form and capacity, is as the following:

Constant current zone: $V_b \leqq 0.8 V_b$*,

I_b*=$I_{ch,max}$

Constant voltage zone: 0.8 V_b*<$V_b \leqq 0.95 V_b$*,

I_b*= $I_{ch,max}$ ~0.1 $I_{ch,max}$ (depending on linear adjustment of battery voltage

Floating zone: 0.95 V_b*< $V_b \leqq V_b$*,

I_b*= 0.1 $I_{ch,max}$

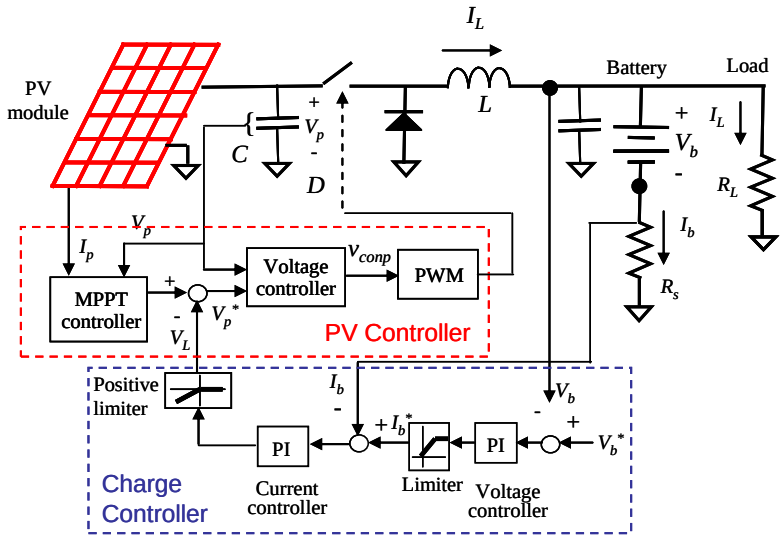
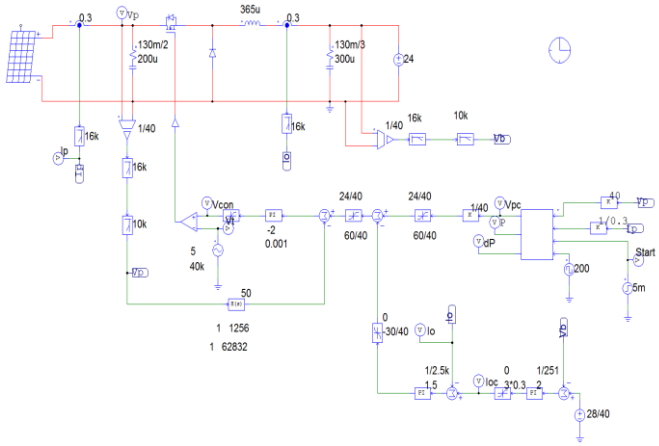


Figure 8.2 PV charging system architecture

Circuit Simulation

The simulating circuit that merges PV controller (MPPT utilizing P&O pertube and observe method) and charging controller is shown as the figure 8.3. The maximum power point of PV module is set as V_{mp}=32V, I_{mp}=3A, P_{mp}=96W. The battery charger setting is V_b*=28V, whilst battery voltage is 24V. When charging current limit (I_b*) is set 5A, the output of system, due to the fact that power output (P_{ch} =24V*5A=120W) is beyond P_{mp} under the setting, will be limited in P_{mp} and PV module will be operated in the maximum power point, which is like the previous MPPT mode (when connecting to load) or partial charging mode. The simulating result is shown as the figure 8.4 where system operates in the MPP point definitely. The battery voltage is 24V; when charging current limit (I_b*) is set 3A, the output of system, due to the fact that power output (P_{ch} =24V*3A=72W) is below Pmp under the setting, will be determined by P_{ch} and MPPT will deviate accordingly. The output of system will be determined by P_{ch} as well. When lifting the output battery voltage to 28V, charging controller will enter CV mode and I_b will be reduced. Thus, MPPT will deviate more seriously and PV module will be close to open-circuit voltage. Refer to the figure 8.6 for the simulating result.



(buck_5_P&O_charge.psimsch)

Figure 8.3 PV charger utilizing P&O MPPT
(buck_5_P&O_charge.psimsch)

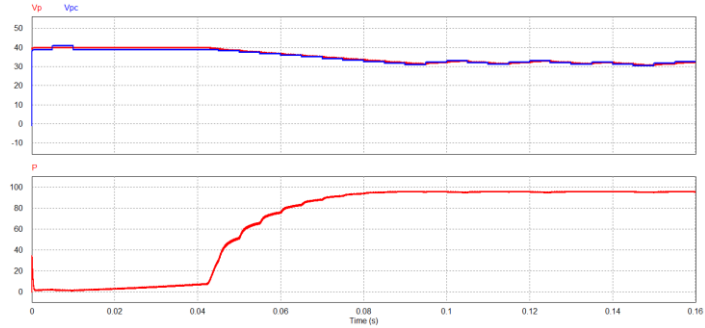


Figure 8.4 The charging controller operating in CC mode with power generation below requirement of CC current setting (MPPT mode or partial charging mode)

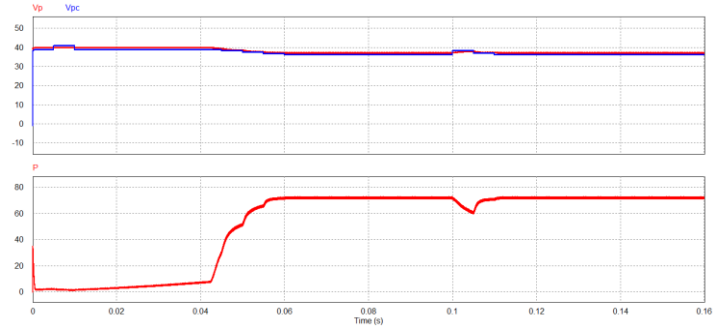


Figure 8.5 The charging controller operating in CC mode with power generation beyond requirement of CC current setting (MPPT offset mode)

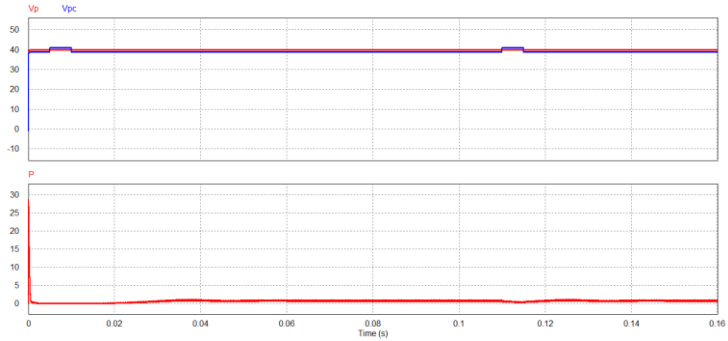
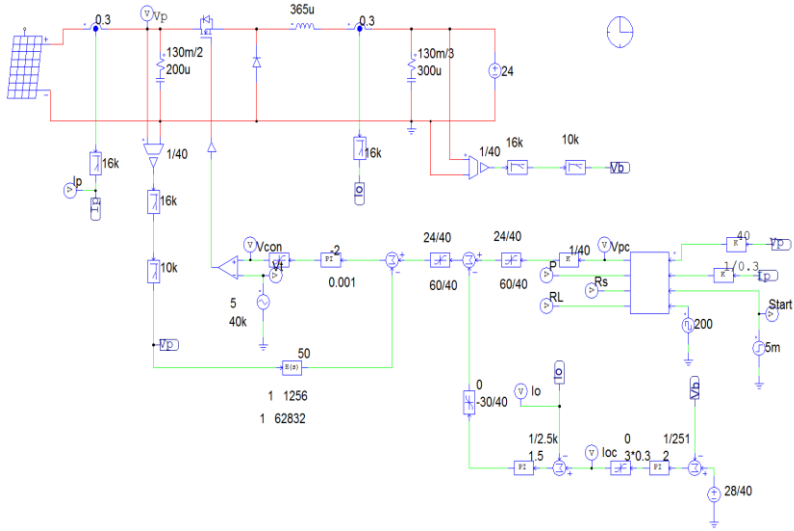


Figure 8.6 The charging controller operating in CV mode with power generation beyond requirement of CV current setting (MPPT offset mode)

As the figure 5.7 shown, MPPT utilizes PV charger simulating circuit of INC method with the simulating result under severally identical testing conditions as the result from P&O method. We will not elaborate further here and please help simulate and validate that on your own.

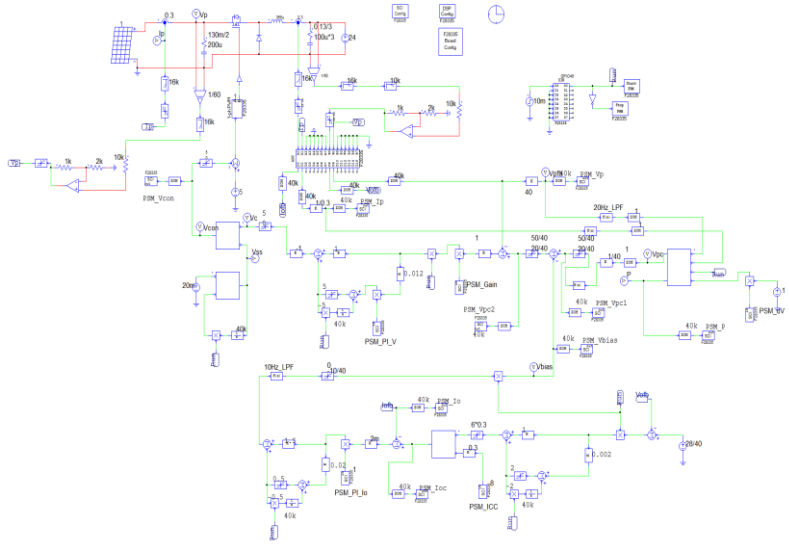


(buck_5_INC_charge.psimsch)

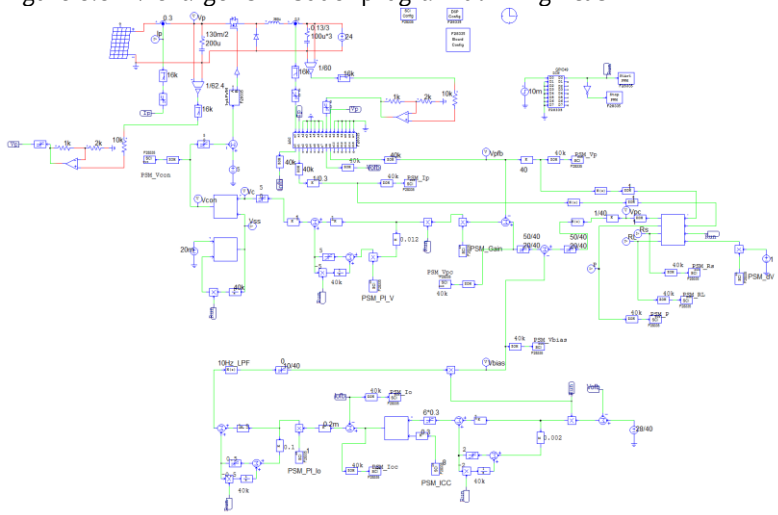
Figure 8.7 PV charger utilizing INC MPPT

(buck_5_INC_charge.psimsch)

SimCoder Program Layout



(Lab5_P&O_charge_R)
Figure 8.8 PV charger SimCoder program utilizing P&O MPPT



(Lab5_INC_charge_R)
Figure 8.9 PV charger SimCoder program utilizing INC MPPT

Experiment Measurement

The experimental devices and teaching aid layout are illustrated as the figure 8.10. DC power supply, PSW 160-7.2, connects to the input terminal J201 of buck teaching aid. The output terminal J202 connects to the DC electrical load, PEL-2040, and utilizes constant voltage mode. MPPT offset mode is displayed in the figure 8.11.

Figure 8.10 Experiment devices layout

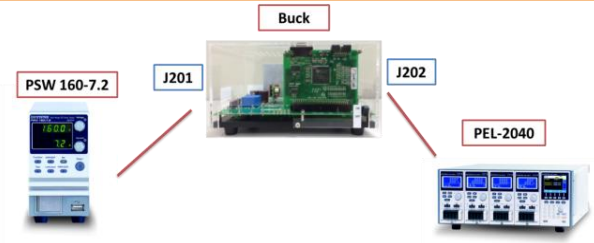


Figure 8.11 MPPT offset mode