# Power Conditioning System Module

PEK-540

## User Manual

**GW INSTEK PART NO. 82EK-11000M01**

ISO-9001 CERTIFIED MANUFACTURER

GW INSTEK

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# Table of Contents

# Introduction

As the figure 0.1 shown, PEK-540, the Power Conditioning System Module, is based on both the first-stage structure of Bi-directional DC-DC Converter and the second-stage structure of Three Phase Four Wire Inverter with fully digital control system. The purpose of this it, as shown in the figure 0.2, is to provide a learning platform for power converter of specifically digital control, having users, via PSIM software, to understand the principle, analysis as well as design of power converter through simulating process. More than that, it helps convert, via SimCoder tool of PSIM, control circuit into digital control and proceed to simulation with the circuit of DSP, eventually burning the control program, through simulating verification, in the DSP chip. Also, it precisely verifies the accuracy of designed circuit and controller via control and communication of DSP.

Figure 0.1

Experiment module of Power Conditioning System

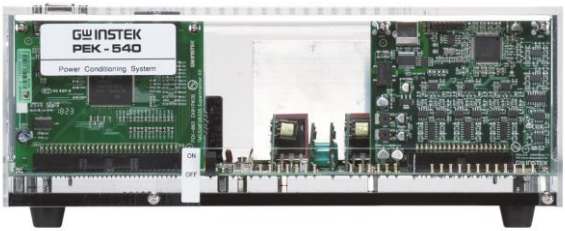
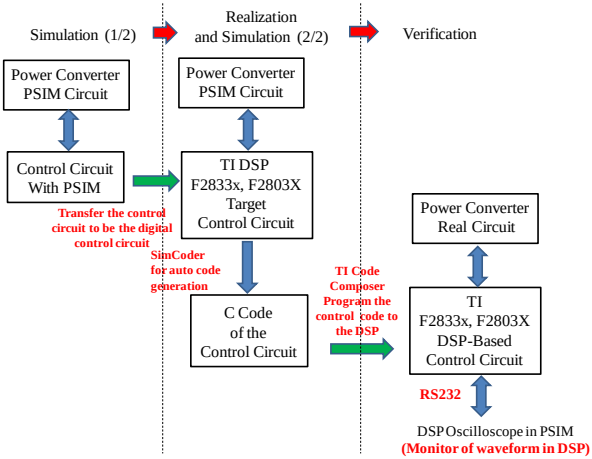


Figure 0.2

The process in details




Thre are 7 experiments can be fulfilled by PEK-540 as follows:

1. Interleaved Buck Converter
2. Interleaved Boost Converter
3. Bi-directional DC-DC Converter
4. Three Phase Four Wire Boost Stand-alone Inverter
5. Three Phase Four Wire PV Grid-connected Inverter
6. Three Phase Four Wire Battery Energy Storage System
7. Three Phase Four Wire Hybrid System

In addition to PEK-540, it is required to utilize PEK-005A auxiliary power module as figure 0.3 shown and PEK-006 JTAG burning module as figure 0.4 shown for experiments. Also, PTS-5000 experiment platform as figure 0.5 shown is necessary for completing the experiments.

Figure 0.3

Auxiliary power module

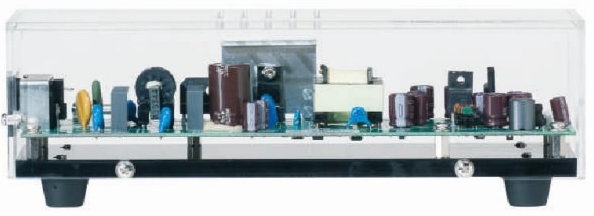


Figure 0.4

JTAG burning module

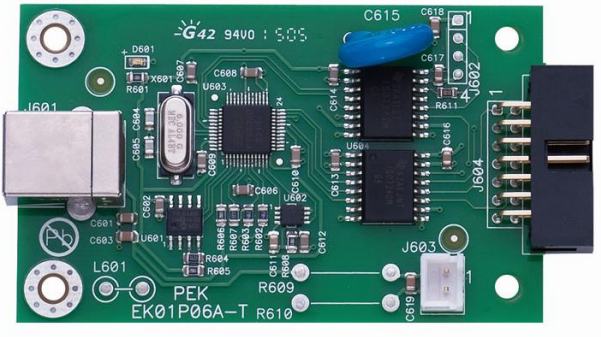


Figure 0.5

PTS-5000 experiment platform

The DSP I/O pin configuration of PEK-510 is shown as the figure 0.6. Refer to the appendix A for the circuit diagrams of PEK-540, which can be divided into power circuit, sensing circuit, drive circuit and protection circuit. The sensing circuit is further divided into 2 sections; one is for test point measurement, and the other one is for feedback DSP control, both of which have varied attenuation amplifications individually as the following table 0-1 and table 0-2 shown.

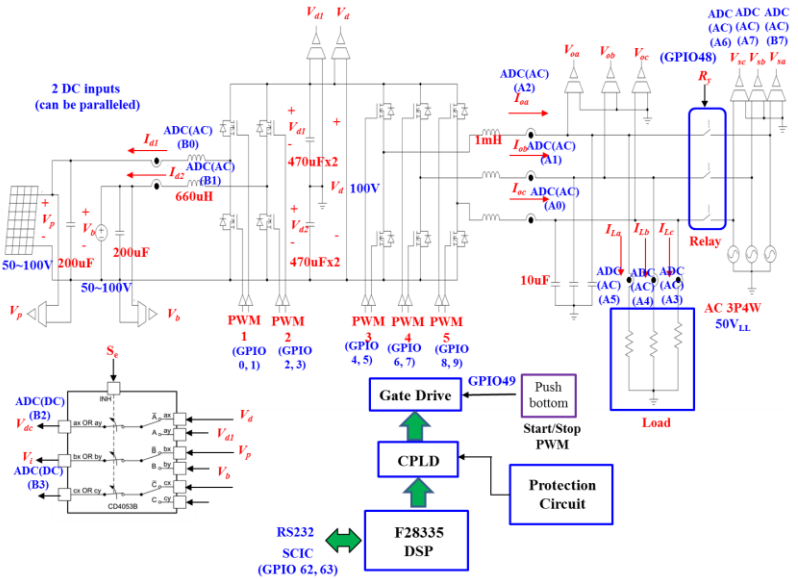



Figure 0.6 I/O configuration

Table 0.1 PEK-540 test point measurement ratio

| | Sensing item | Sensing ratio |
|---|---|---|
| 1 | PV arm inductor current (IP) | 0.4 |
| 2 | Battery arm inductor current (IB) | 0.4 |
| 3 | PV arm input voltage (VP) | 0.0196 |
| 4 | Battery arm input voltage (VB) | 0.0196 |
| 5 | DC link voltage (VD) | 0.0196 |
| 6 | Neutral point ground voltage (Vd1) | 0.0196 |
| 7 | Inverter A phase output current (IO-A) | 0.4768 |
| 8 | Inverter B phase output current (IO-B) | 0.4768 |
| 9 | Inverter C phase output current (IO-C) | 0.4768 |
| 10 | Inverter A phase load current (IL-A) | 0.4768 |
| 11 | Inverter B phase load current (IL-B) | 0.4768 |
| 12 | Inverter C phase load current (IL-C) | 0.4768 |
| 13 | Inverter A phase output voltage (VO-A) | 0.0498 |
| 14 | Inverter B phase output voltage (VO-B) | 0.0498 |
| 15 | Inverter C phase output voltage (VO-C) | 0.0498 |
| 16 | Grid power A phase voltage (VS-A) | 0.0498 |
| 17 | Grid power B phase voltage (VS-B) | 0.0498 |
| 18 | Grid power C phase voltage (VS-C) | 0.0498 |

Table 0.2 PEK-540 DSP feedback ratio

| | Sensing item | Sensing ratio |
|---|---|---|
| 1 | PV arm inductor current (IP) | 0.2410 |
| 2 | Battery arm inductor current (IB) | 0.2410 |
| 3 | PV arm input voltage (VP) | 0.0249 |
| 4 | Battery arm input voltage (VB) | 0.0249 |
| 5 | DC link voltage (VDC) | 0.0249 |
| 6 | Neutral point ground voltage (Vd1) | 0.0249 |
| 7 | Inverter A phase output current (IO-A) | 0.2996 |
| 8 | Inverter B phase output current (IO-B) | 0.2996 |
| 9 | Inverter C phase output current (IO-C) | 0.2996 |
| 10 | Inverter A phase load current (IL-A) | 0.2996 |
| 11 | Inverter B phase load current (IL-B) | 0.2996 |
| 12 | Inverter C phase load current (IL-C) | 0.2996 |
| 13 | Inverter A phase output voltage (VO-A) | 0.0249 |
| 14 | Inverter B phase output voltage (VO-B) | 0.0249 |
| 15 | Inverter C phase output voltage (VO-C) | 0.0249 |
| 16 | Grid power A phase voltage (VS-A) | 0.0249 |
| 17 | Grid power B phase voltage (VS-B) | 0.0249 |
| 18 | Grid power C phase voltage (VS-C) | 0.0249 |

# The Description on Chapters

See the chapter arrangements as follows

| | |
|---|---|
| Brief | Briefly describes the experimental method, experimental items and circuit setup. It also explains the contents of each chapter. |
| Experiment 1 Interleaved Buck Converter | To get to know the main circuit of interleaved buck converter, and learn the voltage and current dual-loop control method. To realize the DSP digital control circuit planning and learn the method of digital control programming via PEK-540 module. To well get familiar with the experiment devices and software manipulation. |
| Experiment 2 Interleaved Boost Converter | To get to know the main circuit of interleaved boost converter, and learn the voltage and current dual-loop control method. To realize the DSP digital control circuit planning and learn the method of digital control programming via PEK-540 module. |
| Experiment 3 Bi-directional DC-DC Converter | To get to know the main circuit of bi-directional DC-DC converter, and learn the control method. To realize the DSP digital control circuit planning and learn the method of digital control programming via PEK-540 module. |
| Experiment 4 Three phase Four Wire Boost Stand-alone Inverter | To get to know the three phase four wire boost stand-alone inverter integrated by the first-stage boost converter with the three-phase inverter, and learn the control method of inverter. |

| | |
|---|---|
| Experiment 5 Three phase Four Wire PV Grid-connected Inverter | To get to know the characteristics of PV module and diversified MPPT method, and learn the SimCoder code programming of Perturb and Observe method. Also, to realize MPPT via the PEK-540 boost converter, further fulfilling the experiment of three phase PV grid-connected inverter through integration with the second-stage three phase grid-connected inverter. |
| Experiment 6 Three phase Four Wire Battery Energy Storage System | To get to know the fundamental with structure of three phase four wire battery energy storage system, and synthesize the bi-directional DC-DC converter with three phase inverter, further proceeding to the code programming via SimCoder, after well planning. |
| Experiment 7 Three phase Four Wire Hybrid System | Synthesize the PV power system with the battery energy storage system to form the hybrid micro-grid system, further proceeding to the code programming via SimCoder, after well mapping out the PEK-540. |

# Experiment 1 – Interleaved Buck Converter

## Circuit Simulation

The circuit parameters of converter are as follows:

Battery Voltage $V_b$ = 50V

DC BUS Voltage $V_d$ = 100V

$F_s$ = 40kHz，$V_{tri}$ = $10V_{pp}$ (PWM)

$C_b$ = 200uF，$L_b$ = 661.5mH，$C_{Bus}$ = 470uF

$K_s$ = 0.24 (AC current sensing factor)

$K_v$ = 1/40 (DC voltage sensing factor)

The analogue circuit diagram based on the parameters above is as the following figure 1.1 shown:

PSIM File: PEK-540_Sim1_ IL_Buck_V11.1.5_V1.1

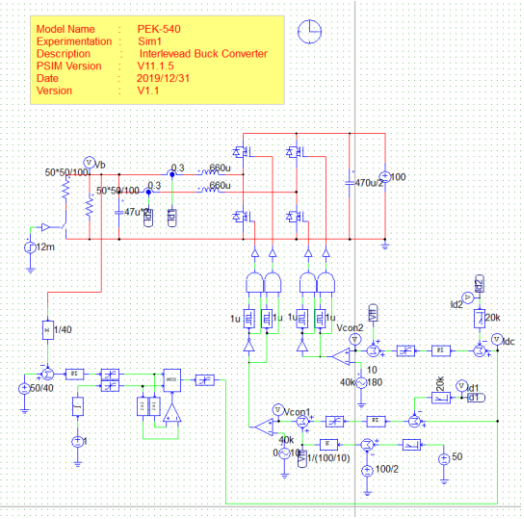



Figure 1.1 Experiment 1 PSIM analogue circuit diagram

The simulation result is shown within the figure 1.2 and 1.3:

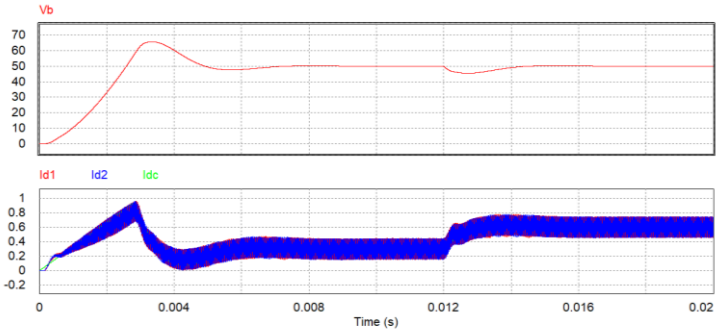



Figure 1.2 Experiment 1 analogue circuit simulation waveforms

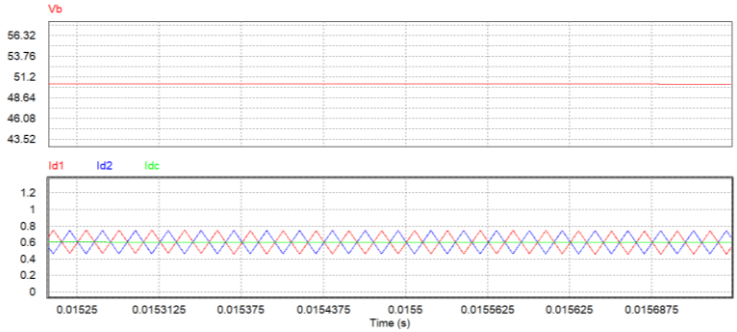



Figure 1.3 Experiment 1 analogue circuit simulation waveforms

The digital circuit diagram based on the analogue circuit is shown as the figure 1.4:
PSIM File: PEK-540_Lab1_ IL_Buck_V11.1.5_V1.1

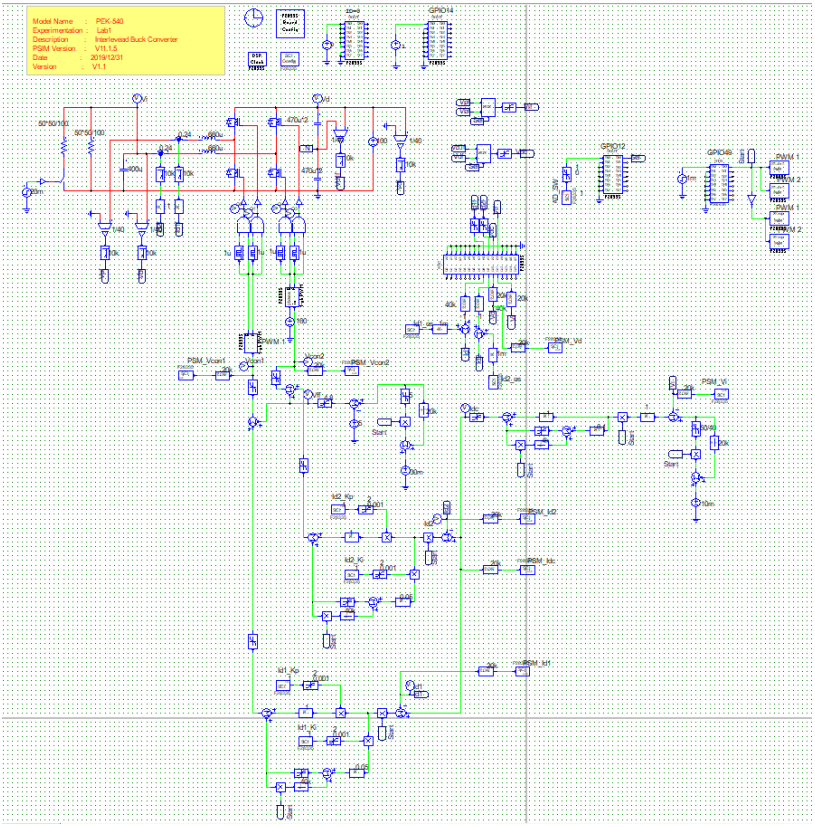



Figure 1.4 Experiment 1 PSIM digital circuit diagram

The simulation result is shown within the figure 1.5:

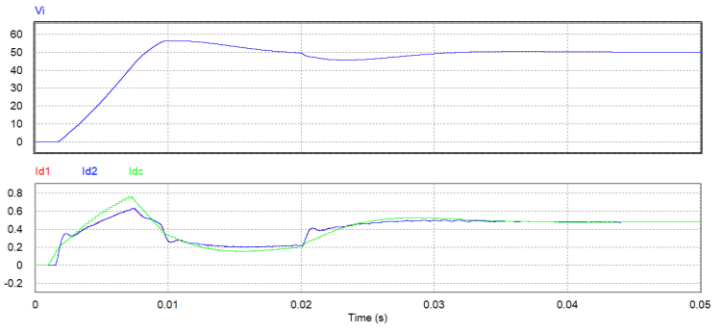



Figure 1.5 Experiment 1 digital circuit simulation waveforms

After confirming simulation, the corresponding C Code will be generated automatically via "Generate Code" of "Simulate".

## Experiment Devices

The required devices for experiment are as follows:

- PEK-540 * 1
- PEK-005A * 1
- PEK-006 * 1
- PTS-5000 * 1 (with GDS-2204E, PSW160-7.2, PEL-3031E)
- PC * 1

# Experiment Procedure

1. The experiment wiring is shown as the figure 1.6. Please follow it to complete wiring.

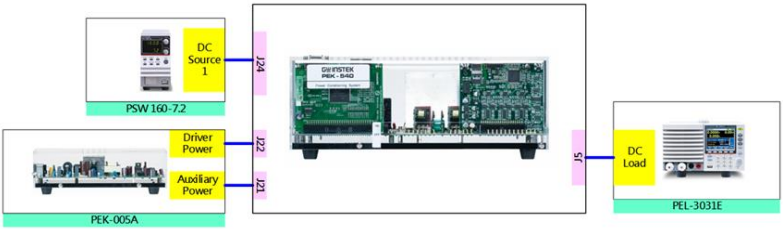



Figure 1.6 Experiment 1 wiring figure

2. After wiring, make sure the PEK-540 switch is OFF followed by turning the PEK-005A switch ON. The DSP red indicator lights on as the figure 1.7 shown, which means the DSP power is steadily normal.


Figure 1.7 DSP normal status with light on

3. Refer to the appendix B for burning procedure.
4. Connect the test leads of oscilloscope to IP, IB and VB, respectively, as the figure 1.8 shown.

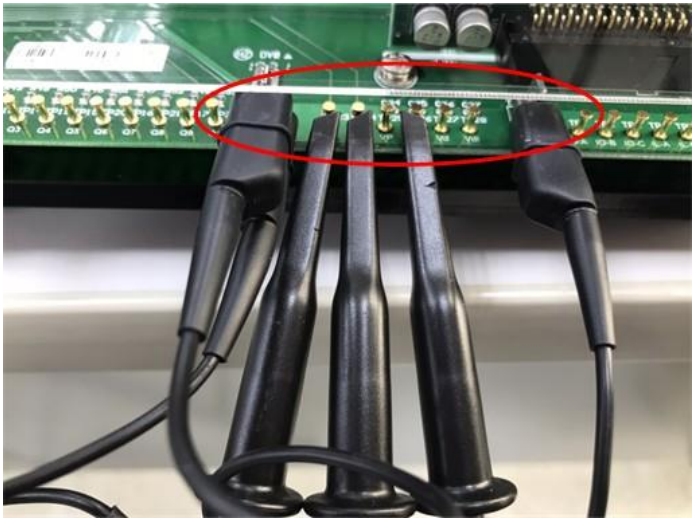


Figure 1.8 Oscilloscope test leads wiring

5. Set voltage 100V and current 3A for PSW 160-7.2 as the figure 1.9 shown.


Figure 1.9 The settings of PSW 160-7.2

6. After powering on PEL-3031E, set CR Mode for Load mode with Low in Range. Further set 26Ω for Channel_A and 13Ω for Channel_B as the figure 1.10 shown.


Figure 1.10 The settings of PEL-3031E load

7. After setting up and turning on PSW power and PEL-3031E load, finally turn on the switch of PEK-540.

# The purpose of experiment

PEK-540 is the Bi-directional DC-DC Converter in terms of the first-stage architecture. Within the Lab2 experiment, we will operate the unit under boost mode to observe, with fluctuations of load condition, if output voltage value is maintained within steady output via closed-loop system.

# The experiment result

Due to the fact that the direction of inductor current is defined as positive under boost mode, the current displayed on oscilloscope will be negative under buck mode.

## Electronic Load 26Ω

The figure 1.11 shows that electronic load is set 26Ω. The figure 1.12 displays that IP output RMS current is 0.447A (1.1175A in actual value), and IB is 0.457A (1.1425A in actual value), and VB output RMS voltage is 0.961V (49.03V in actual value).

Figure 1.11

Electronic load 26Ω setting

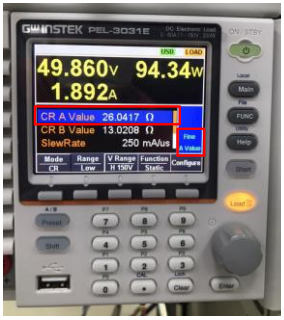


Figure 1.12

Electronic load 26Ω measured waveform


## Electronic Load 13Ω

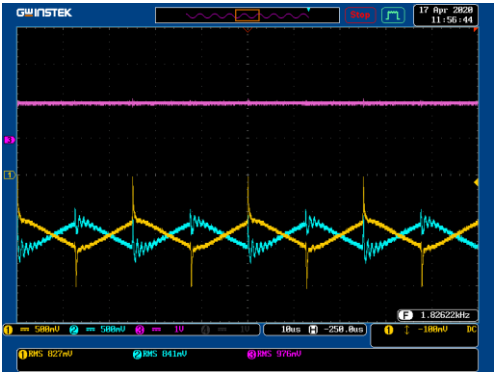
The figure 1.13 shows that electronic load is set 13Ω. The figure 1.14 displays that IP output RMS current is 0.827A (2.0675A in actual value), and IB is 0.841A (2.1025A in actual value), and VB output average RMS is 0.976V (49.795V in actual value).

Figure 1.13

Electronic load 13Ω setting

Figure 1.14

Electronic load 13Ω measured waveform




Per differed load operations, fill in the table 1.1 with the results in order. Refer to the table 0.1 for the sensing ratio.

Table 1.1 Output voltage current measured data in varied load settings

| | IP(Arms) (Measured value) | IP(Arms) (Actual value) | IB(Arms) (Measured value) | IB(Arms) (Actual value) | VB(Vrms) (Measured value) | VB(Vrms) (Actual value) |
|---|---|---|---|---|---|---|
| Half load (26Ω) | 0.447A | 1.1175A | 0.457A | 1.1425A | 0.961V | 49.03V |
| Full load (13Ω) | 0.827A | 2.0675A | 0.841A | 2.1025A | 0.976V | 49.795V |

# The Conclusion

Based on the table 1.1, it is conceivable that output current, in the closed-loop buck converter system with load fluctuations, will increase in accord with load increment with maintaining output voltage unchanged.

# Experiment 2 – Interleaved Boost Converter

## Circuit Simulation

The converter specification is as follows:

Battery Voltage $V_b$ = 50V

DC BUS Voltage $V_d$ = 100V

$F_s$ = 40kHz，$V_{tri}$ = $10V_{pp}$ (PWM)

$C_b$ = 200uF，$L_b$ = 661.5mH，$C_{Bus}$ = 470uF

$K_s$ = 0.24 (AC current sensing factor)

$K_v$ = 1/40 (DC voltage sensing factor)

The analogue circuit diagram based on the parameters above is as the following figure 2.1 shown:
PSIM File: PEK-540_Sim2_ IL_ Boost_V11.1.5_V1.1

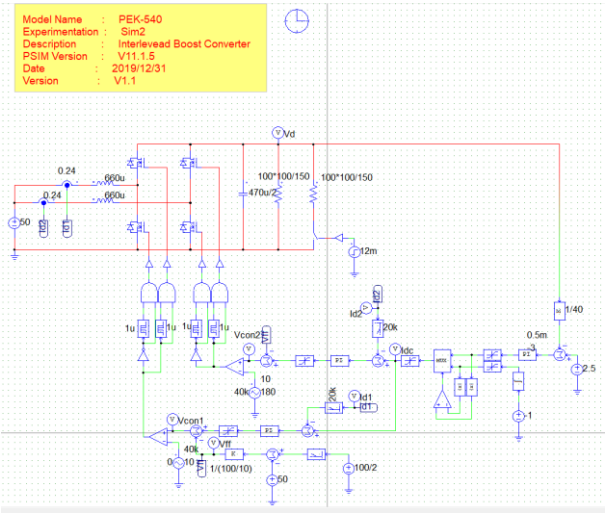



Figure 2.1 Experiment 2 - PSIM analogue circuit diagram

The simulation result is shown within the figure 2.2 and 2.3:

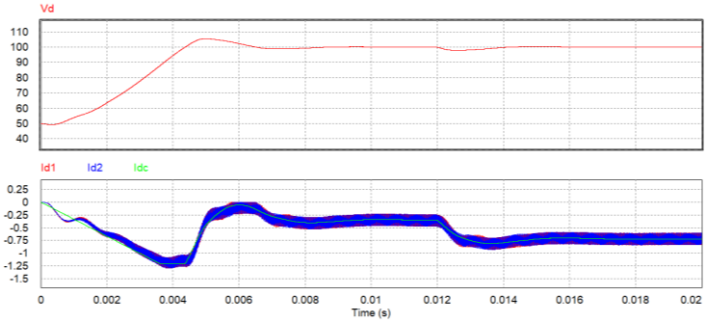



Figure 2.2 Experiment 2 analogue circuit simulation waveforms

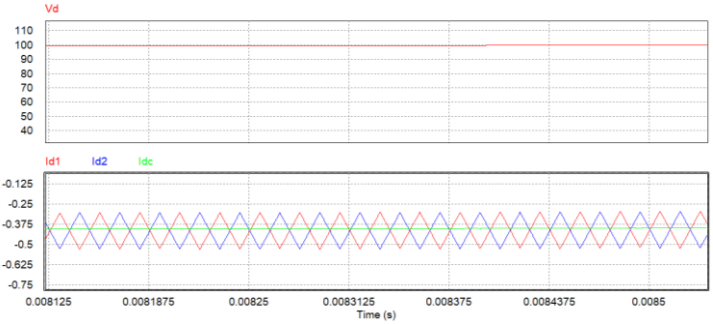



Figure 2.3 Experiment 2 analogue circuit simulation waveforms

The analogue circuit diagram based on the digital circuit is shown as the figure 2.4:
PSIM File: PEK-540_Lab2_ IL_Boost_V11.1.5_V1.1

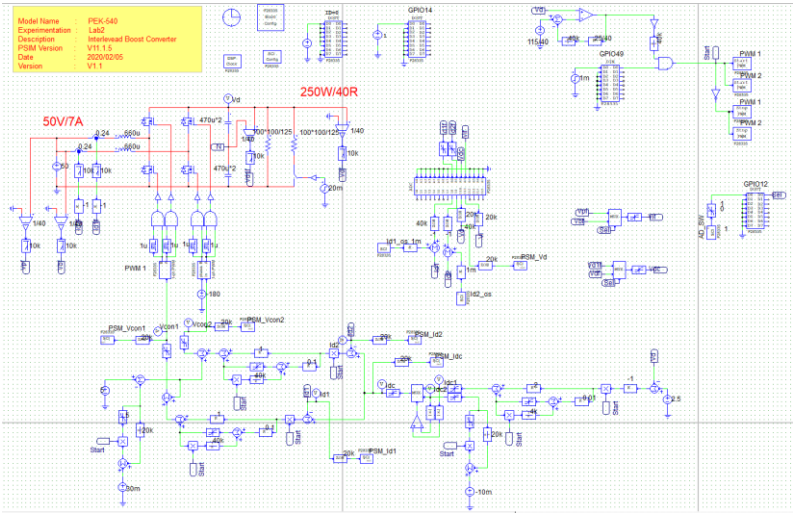



Figure 2.4 Experiment 2 PSIM digital circuit diagram

The simulation result is shown within the figure 2.5:

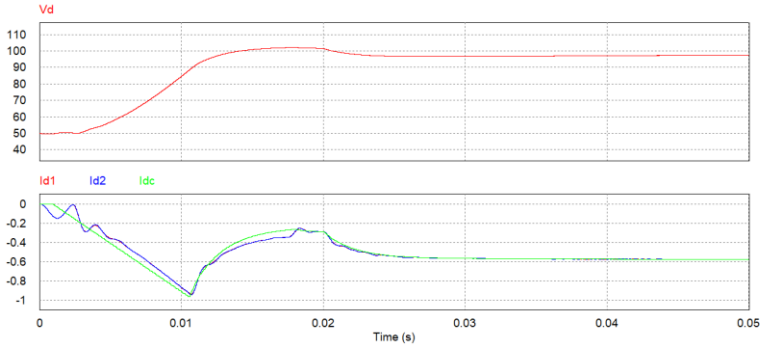



Figure 2.5 Experiment 2 digital circuit simulation waveforms

After confirming simulation, the corresponding C Code will be generated automatically via “Generate Code” of “Simulate”.

# Experiment Devices

The required devices for experiment are as follows:

- PEK-540 * 1
- PEK-005A * 1
- PEK-006 * 1
- PTS-5000 * 1 (with GDS-2204E, PSW160-7.2 and PEL-3031E)
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# Experiment Procedure

1. The experiment wiring is shown as the figure 2.6. Please follow it to complete wiring.

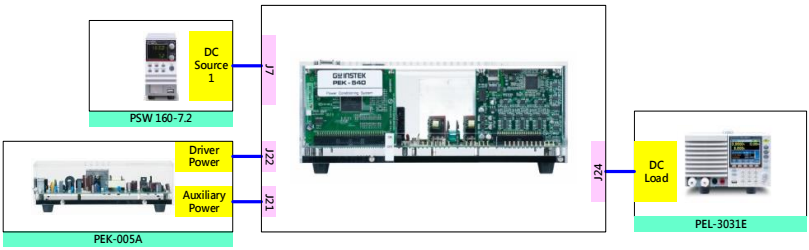



Figure 2.6 Experiment 2 wiring figure

2. After wiring, make sure the PEK-540 switch is OFF followed by turning the PEK-005A switch ON. The DSP red indicator lights on as the figure 2.7 shown, which means the DSP power is steadily normal.


Figure 2.7 DSP normal status with light on

3. Refer to the appendix B for burning procedure.
4. Connect the test leads of oscilloscope to IP, IB and Vd, respectively, as the figure 2.8 shown.

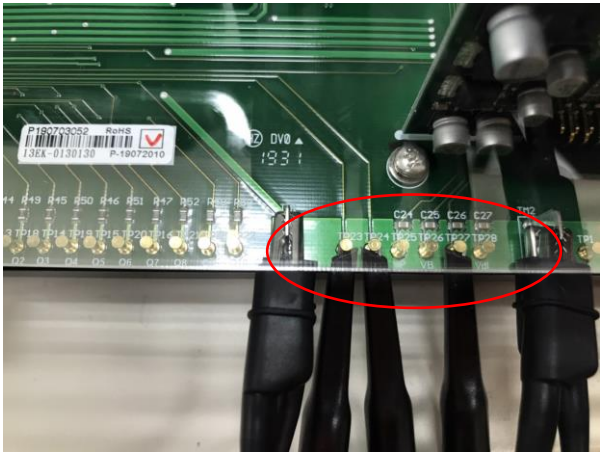


Figure 2.8 Oscilloscope test leads wiring

5. Set voltage 50V and current 7A for PSW 160-7.2 as the figure 2.9 shown.


Figure 2.9 The settings of PSW 160-7.2

6. After powering on PEL-3031E, set CR Mode for Load mode with Low in Range. Further set 100Ω for Channel_A and 50Ω for Channel_B as the figure 2.10 shown.


Figure 2.10 The settings of PEL-3031E load

7. After setting up and turning on PSW power and PEL-3031E load, finally turn on the switch of PEK-540.

# The purpose of experiment

PEK-540 is the Bi-directional DC-DC Converter in terms of the first-stage architecture. Within the Lab2 experiment, we will operate the unit under boost mode to observe, with fluctuations of load condition, if output voltage value is maintained within steady output via closed-loop system.

# The experiment result

Due to the fact that the direction of inductor current is defined as positive under boost mode, the current displayed on oscilloscope will be positive.

## Electronic Load 100Ω

The figure 2.11 shows that electronic load is set 100Ω. The figure 2.12 displays that IP output RMS current is 0.411A (1.0275A in actual value), and IB is 0.396A (0.99A in actual value), and Vd output RMS voltage is 1.93V (98.469V in actual value).

Figure 2.11

Electronic load 100Ω setting

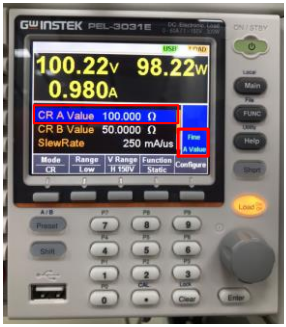
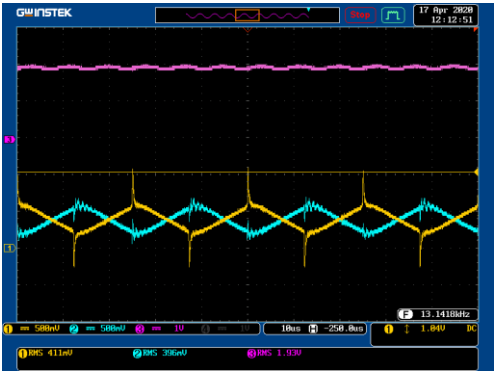


Figure 2.12
Load 100Ω measured waveform




## Electronic Load 50Ω

The figure 2.13 shows that electronic load is set 50Ω. The figure 2.14 displays that IP output RMS current is 0.827A (2.0675A in actual value), and IB is 0.811A (2.0275A in actual value), and Vd output average RMS is 1.92V (97.959V in actual value).

Figure 2.13
Electronic load 50Ω setting

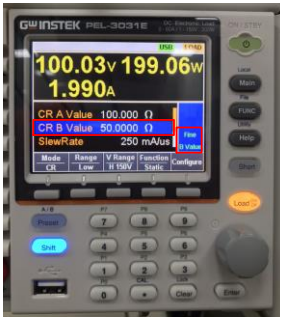
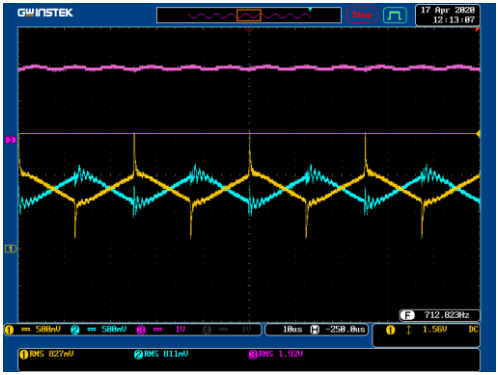


Figure 2.14
Load 50Ω measured waveform




Per differed load operations, fill in the table 2.1 with the results in order. Refer to the table 0.1 for the sensing ratio.

Table 2.1 Output voltage current measured data in varied load settings.

| | IP(Arms) (Measured value) | IP(Arms) (Measured value) | IB(Arms) (Measured value)) | IB(Arms) (Measured value) | Vd(Vrms) (Measured value) | Vd(Vrms) (Measured value)) |
|---|---|---|---|---|---|---|
| Half load (100Ω) | 0.411A | 1.0275A | 0.396A | 0.99A | 1.93V | 98.469V |
| Full load (50Ω) | 0.827A | 2.0675A | 0.811A | 2.0275A | 1.92V | 97.959V |

# The Conclusion

Based on the table 2.1, it is conceivable that output current, in the closed-loop boost converter system with load fluctuations, will increase in accord with load increment with maintaining output voltage unchanged.

# Experiment 3 – Bi-directional DC-DC Converter

## Circuit Simulation

The circuit parameters of converter are as follows:

Battery Voltage $V_b$ = 50V

DC BUS Voltage $V_d$ = 100V

$F_s$ = 40kHz，$V_{tri}$ = $10V_{pp}$ (PWM)

$C_b$ = 200uF，$L_b$ = 661.5mH，$C_{Bus}$ = 470uF

$K_s$ = 0.24 (AC current sensing factor)

$K_v$ = 1/40 (DC voltage sensing factor)

The analogue circuit diagram based on the parameters above is as the following figure 3.1 shown:

PSIM File: PEK-540_Sim3_BD_DC-DC_V11.1.5_V1.1

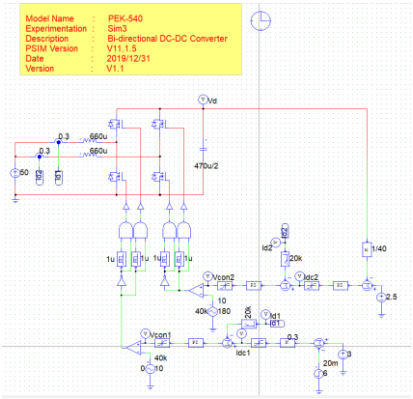



Figure 3.1 Experiment 3 PSIM analogue circuit diagram

The simulation result is shown within the figure 3.2 and 3.3:

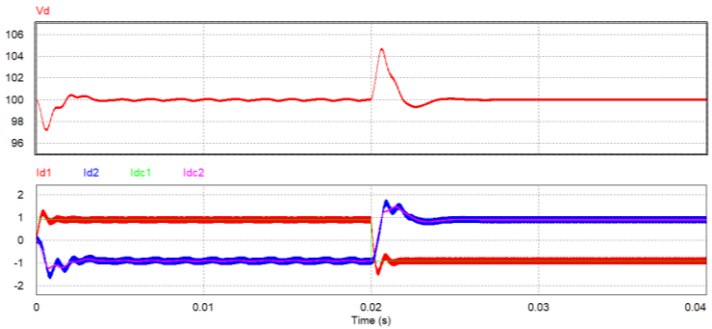



Figure 3.2 Experiment 3 analogue circuit simulation waveforms

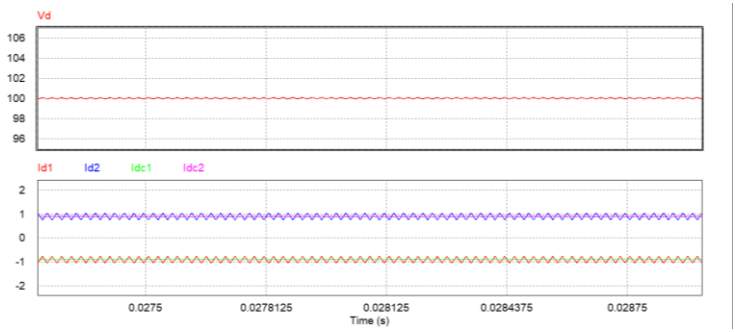



Figure 3.3 Experiment 3 analogue circuit simulation waveforms

The digital circuit diagram based on the analogue circuit is shown as the figure 3.4:
PSIM File: PEK-540_Lab3_BD_DC-DC_V11.1.5_V1.2

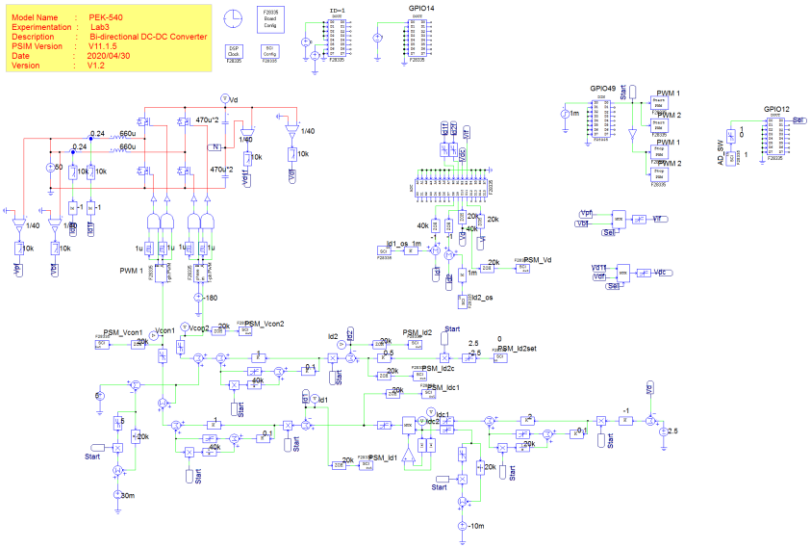



Figure 3.4 Experiment 3 PSIM digital circuit diagram

The simulation result is shown within the figure 3.5:

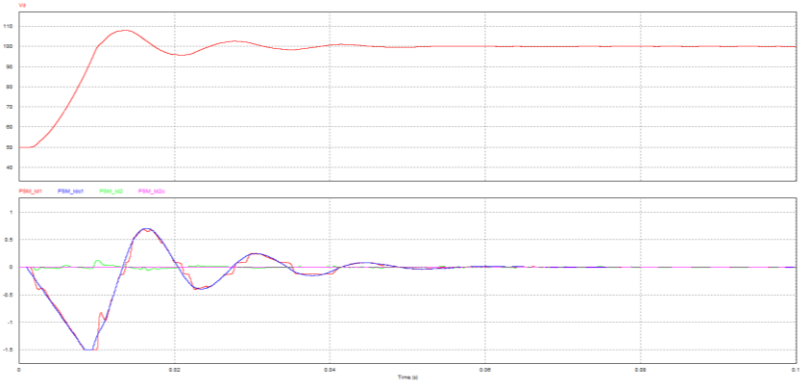


Figure 3.5 Experiment 3 digital circuit simulation waveforms

After confirming simulation, the corresponding C Code will be generated automatically via “Generate Code” of “Simulate”.

# Experiment Devices

The required devices for experiment are as follows:

- PEK-540 * 1
- PEK-005A * 1
- PEK-006 * 1
- PTS-5000 * 1 (with GDS-2204E and PSW160-7.2)
- PC * 1

# Experiment Procedure

1. The experiment wiring is shown as the figure 3.6. Please follow it to complete wiring.

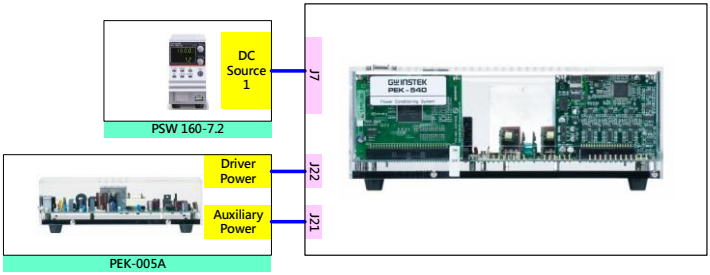



Figure 3.6 Experiment 3 wiring figure

2. After wiring, make sure the PEK-540 switch is OFF followed by turning the PEK-005A switch ON. The DSP red indicator lights on as the figure 3.7 shown, which means the DSP power is steadily normal.


Figure 3.7 DSP normal status with light on

3. Refer to the appendix B for burning procedure.
4. Connect the test leads of oscilloscope to IP, IB and Vd, respectively, as the figure 3.8 shown.

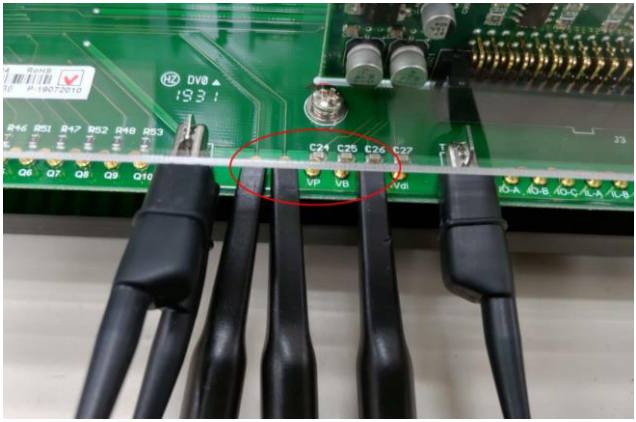



Figure 3.8 Oscilloscope test leads wiring

5. Set voltage 50V and current 1A for PSW 160-7.2 as the figure 3.9 shown.


Figure 3.9 The settings of PSW 160-7.2

6. Proceed to connection step in accordance with the appendix C.
7. After setting up and turning on PSW power output, finally turn on the switch of PEK-540.

# The purpose of experiment

Lab3 is the Bi-directional DC-DC Converter. When powering on the circuit, change the operation mode of converter (Boost or Buck) via different current settings to observe the fluctuations of inductor current.

# The experiment result

Due to the fact that the direction of inductor current is defined as positive under boost mode, the current displayed on oscilloscope will be negative under buck mode. And the Id1 and Id2 displayed on DSP oscilloscope are IP current and IB current, respectively.

## PSM_Id2set = 0

As the figure 3.10 shown, through the observation on waveforms from DSP oscilloscope, Id1 and Id2 currents are in the proximity of zero on the condition of the command value PSM_ID2SET = 0. As the figure 3.11 shown, it can be clearly seen that IP output RMS current is 0.145A (0.362A in actual value), and IB is 0.116A (0.290A in actual value), and Vd is 1.98V (101.02V in actual value).

Figure 3.10
PSM_Id2set = 0

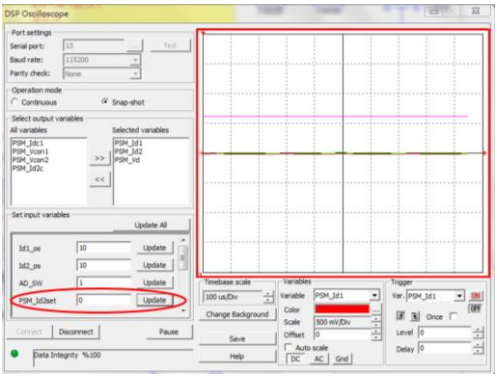
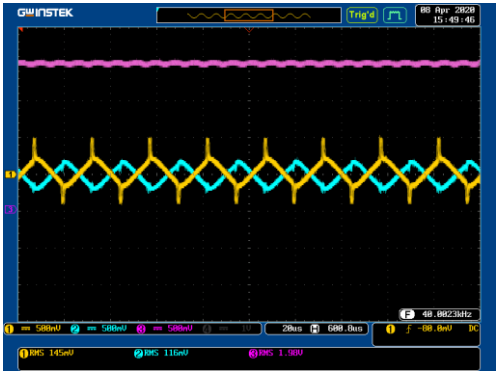


Figure 3.11
PSM_Id2set = 0 measured waveform



## PSM_Id2set = -1

As the figure 3.12 shown, through the observation on waveforms from DSP oscilloscope, Id1 is under the Boost mode with positive current direction, whereas Id2 is under the Buck mode with negative current direction on the condition of the command value PSM_ID2SET = -1. As the figure 3.13 shown, it can be clearly seen that IP output RMS current is 0.765A (1.912A in actual value), and IB is 0.829A (2.072A in actual value), and Vd is 1.98V (101.02V in actual value).

Figure 3.12
PSM_Id2set = -1

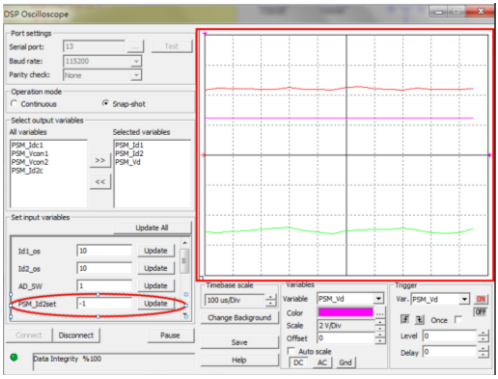


Figure 3.13 PSM_ID2SET = -1 measured waveform


## PSM_Id2set = 1

As the figure 3.14 shown, through the observation on waveforms from DSP oscilloscope, Id2 is under the Boost mode with positive current direction, whereas Id1 is under the Buck mode with negative current direction on the condition of the command value PSM_ID2SET = 1. As the figure 3.15 shown, it can be clearly seen that IP output RMS current is 0.939A (2.347A in actual value), and IB is 0.860A (2.150A in actual value), and Vd is 1.98V (101.02V in actual value).

Figure 3.12 PSM_Id2set= 1

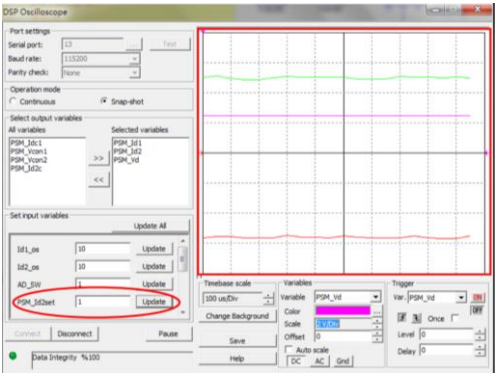


Figure 3.12

PSM_ Id2set= 1 measured waveform


Per the setting of PSM_ID2SET, fill in the table 3.1 with the measured IP, IB and Vd RMS values in order. Refer to the table 0.1 for the ratios of the measured values against the actual values and fill in the table 3.1 with the actual values.

Table 3.1 Output voltage current measured data in varied settings of PSM_ID2SET

| | IP(Arms) (Measured value) | IP(Arms) (Measured value) | IB(Arms) (Measured value) | IB(Arms) (Measured value) | Vd(Vrms) (Measured value) | Vd(Vrms) (Measured value) |
|---|---|---|---|---|---|---|
| PSM_Id2set =0 | 0.145A | 0.362A | 0.116A | 0.290A | 1.98V | 101.02V |
| PSM_Id2set =-1 | 0.765A | 1.912A | 0.829A | 2.072A | 1.98V | 101.02V |
| PSM_Id2set =1 | 0.939A | 2.347A | 0.860A | 2.150A | 1.98V | 101.02V |

From the table 3.1 shown, it has seen that the 2 sets of inductor current have differences due to the circuit loss, though the ideal situation is identically same for 2 sets of inductor current.

# The Conclusion

Within the Lab3 experiment, the first converter is in charge of voltage output, whist the PSM_ID2SET command of the second converter determines current direction. When PSM_ID2SET is positive, the second converter operates under Boost mode and the first converter operates under Buck mode. In contrast, when PSM_ID2SET is negative, the second converter operates under Buck mode and the first converter operates under Boost mode.

# Experiment 4 – Three Phase Four Wire Boost Stand-alone Inverter

## Circuit Simulation

The system specification is as follows:

Battery Voltage Vb = 50V
DC BUS Voltage Vd = 100V
Fs = 40kHz, Vtri = 10Vpp (DC-DC PWM)
Fs = 20kHz, Vtri = 10Vpp (Inverter PWM)
$C_b$ = 200uF, $L_b$ = 661.5uH, $C_{Bus}$= 470uF
L = 1.02mH, C = 10uF
Ks = 0.24 (DC current sensing factor)
Ks = 0.3 (AC current sensing factor)
Kv = 1/40 (DC voltage sensing factor)
Kv = 1/40 (AC voltage sensing factor)

The analogue circuit diagram based on the parameters above is as the following figure 4.1 shown:
PSIM File: PEK-540_Sim4_3P4W_Boost_SA_Inv(50Hz)_V11.1.5_V1.1

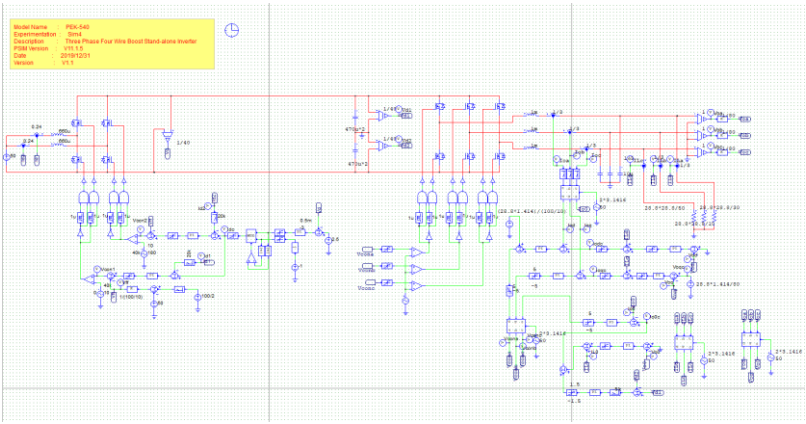


Figure 4.1 Experiment 4 PSIM analogue circuit diagram

The simulation result is shown within the figure 4.2 and 4.3:

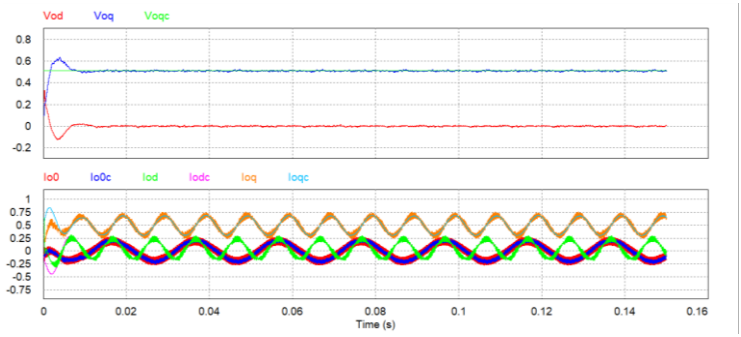



Figure 4.2 Experiment 4 analogue circuit simulation waveforms

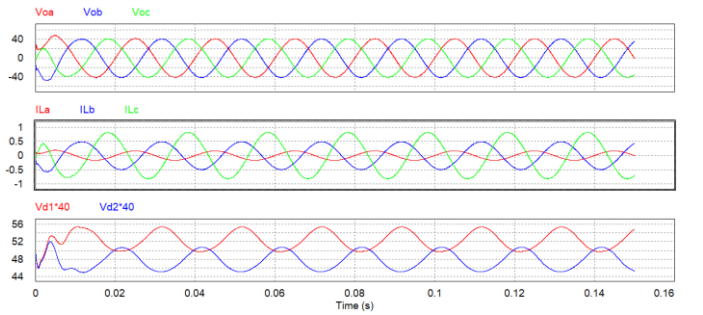



Figure 4.3 Experiment 4 analogue circuit simulation waveforms

The digital circuit diagram based on the analogue circuit is shown as the figure 4.4:

PSIM File: PEK-540_Lab4_3P4W_Boost_SA_Inv(50Hz)_V11.1.5_V1.1

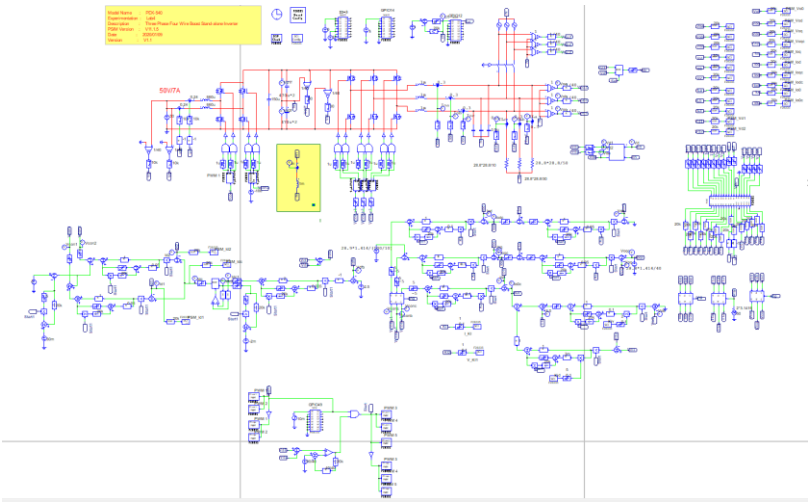


Figure 4.4 Experiment 4 PSIM digital circuit diagram

The simulation result is shown within the figure 4.5 and 4.6:

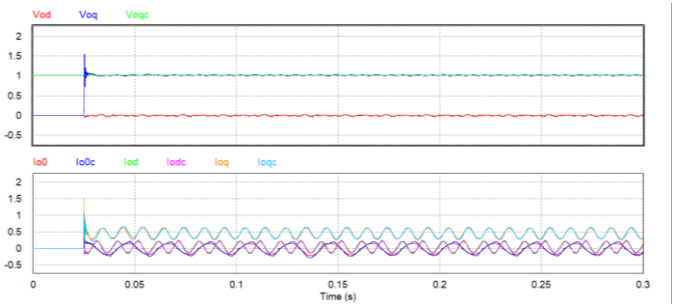



Figure 4.5 Experiment 4 digital circuit simulation waveforms

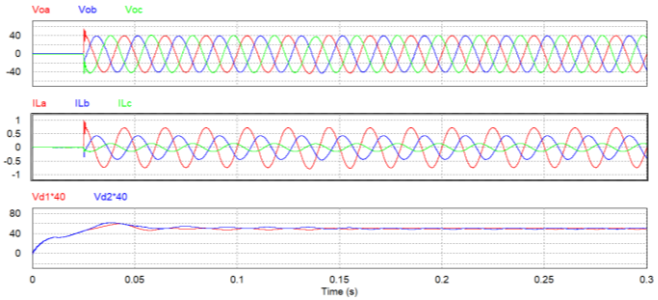



Figure 4.6 Experiment 4 digital circuit simulation waveforms

After confirming simulation, the corresponding C Code will be generated automatically via “Generate Code” of “Simulate”.

## Experiment Devices

The required devices for experiment are as follows:

- PEK-540 * 1
- PEK-005A * 1
- PEK-006 * 1
- PTS-5000 * 1 (with GDS-2204E, PSW160-7.2 and GPL-500)
- PC * 1

## Experiment Procedure

1. The experiment wiring is shown as the figure 4.7. Please follow it to complete wiring.

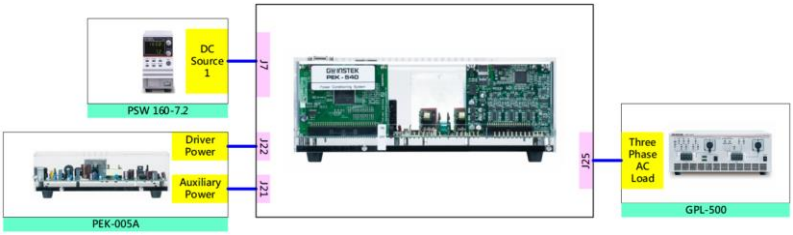



Figure 4.7 Experiment wiring figure

2. After wiring, make sure the PEK-540 switch is OFF followed by turning the PEK-005A switch ON. The DSP red indicator lights on as the figure 4.8 shown, which means the DSP power is steadily normal.


Figure 4.8 DSP normal status with light on

3. Refer to the appendix B for burning procedure.
4. Connect the test leads of oscilloscope to VOA, VOB, VOC and IOA, respectively, as the figure 4.9 shown.

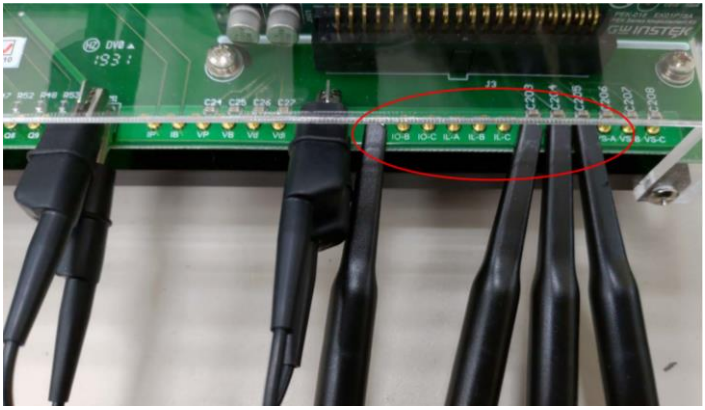


Figure 4.9 Oscilloscope test leads wiring

5. Set voltage 50V and current 7.56A for PSW 160-7.2 as the figure 4.10 shown.

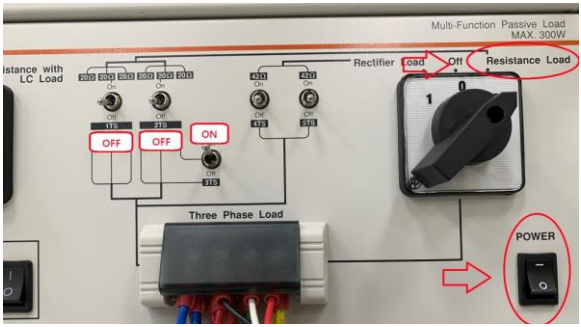
Figure 4.10

The settings of PSW


6. As the figure 4.11 shown, follow the steps below for GPL-500 operation. Power on GPL-500 → Rotate the Three Phase Lord knob to 2 (Resistance Load) → Set 1TS and 2TS as OFF, and 3TS as ON, which indicates no-load mode.

Figure 4.11

The no-load setting of GPL-500




7. Proceed to connection step in accordance with the appendix C.
8. After setting up and turning on PSW power output, finally turn on the switch of PEK-540.

# The purpose of experiment

This experiment is the load fluctuation test of independent inverter. It discusses output voltage and output current fluctuating waveforms when operating in no-load, half-load and full-load modes. Also, it discusses if output voltage is remained balanced when operating in out of balanced.

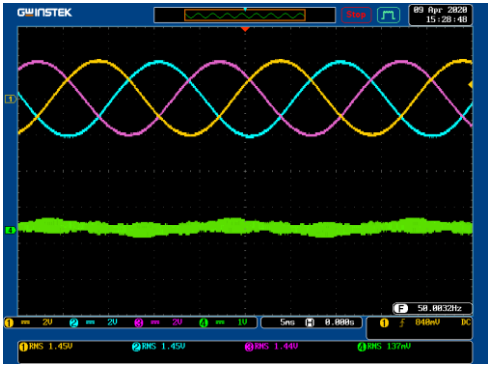
# The experiment result

## GPL-500 in no-load mode

The figure 4.12 shows that when GPL-500 is set as no-load mode, VOA output RMS voltage is 1.45V (29.11V in actual value), and VOB output RMS voltage is 1.45V (29.11V in actual value), and VOC output RMS voltage is 1.44V (28.91V in actual value), and IOA output RMS current is 0.137A (0.287A in actual value).

Figure 4.12

No-load measured waveform

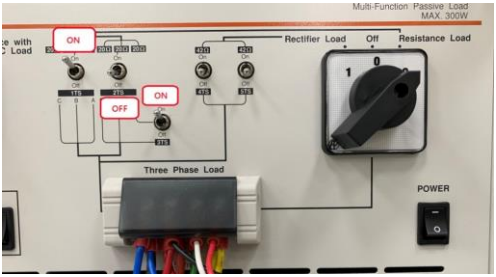



## GPL-500 in half-load mode (20Ω)

As the figure 4.13 shown, both 1TS and 3TS are set ON, and 2TS is OFF, which indicates the half-load mode.

Figure 4.13

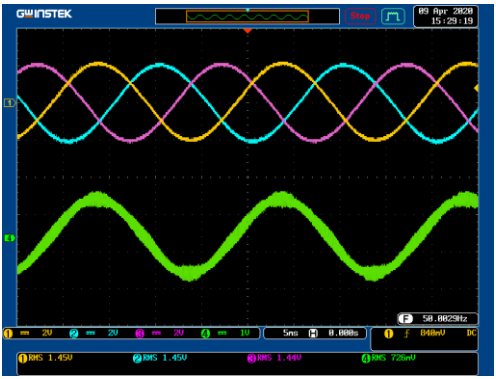
GPL-500 half-load setting




The figure 4.14 shows that when GPL-500 is set half-load mode setting, the VOA output RMS voltage is 1.45V (29.11V in actual value), and VOB output RMS voltage is 1.45V (29.11V in actual value), and VOC output RMS voltage is 1.44V (28.91V in actual value) and IOA output RMS current is 0.726A (1.522A in actual value).

Figure 4.14

Half-load measured waveform




## GPL-500 in full-load mode (10Ω)

The figure 4.15 shows that when 1TS, 2TS and 3TS are set ON, it turns out full-load mode. The figure 4.16 shows that when GPL-500 is set full-load mode setting, the VOA output RMS voltage is 1.45V (29.11V in actual value), and VOB output RMS voltage is 1.45V (29.11V in actual value), and VOC output RMS voltage is 1.44V (28.91V in actual value) and IOA output RMS current is 1.380A (2.893A in actual value).

Figure 4.15
GPL-500 full-load setting

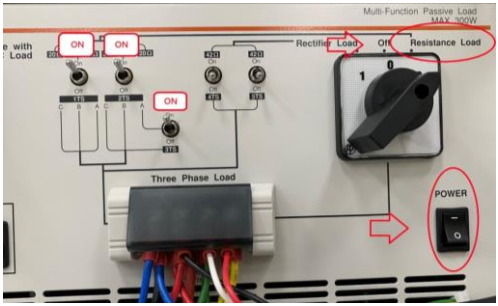
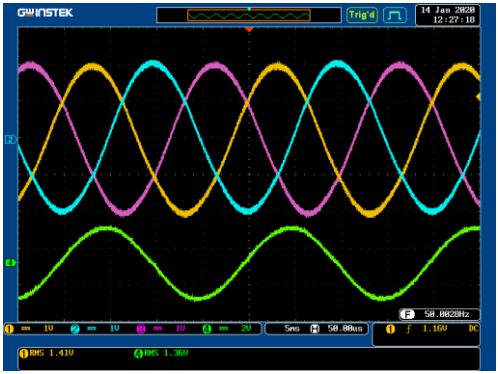



Figure 4.16
Full-load measured waveform




## GPL-500 in out-of-balanced load mode (Ra/Rb/Rc = 20/10/10Ω)

The figure 4.17 shows that when 1TS and 2TS are set ON, and 3TS is set OFF, it turns out out-of-balanced load mode.

[1]. The figure 4.18 shows that when GPL-500 is set out-of-balanced load mode setting, the VOA output RMS voltage is 1.47V (29.51V in actual value), and VOB output RMS voltage is 1.45V (29.51V in actual value), and VOC output RMS voltage is 1.40V (28.11V in actual value). The output voltage is balanced state currently.

[2]. The figure 4.19 shows that when GPL-500 is set out-of-balanced load mode setting, the IOA output RMS current is 0.747A (1.566A in actual value), and IOB output RMS current is 1.41A (2.955A in actual value), and IOC output RMS current is 1.35A (2.830A in actual value). The output current is out-of-balanced state currently.

Figure 4.17

GPL-500 out-of-balanced load setting

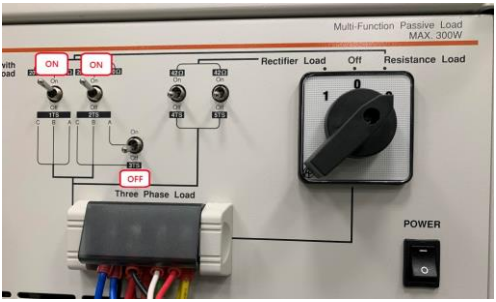



Figure 4.18

Out-of-balanced load output voltage waveform

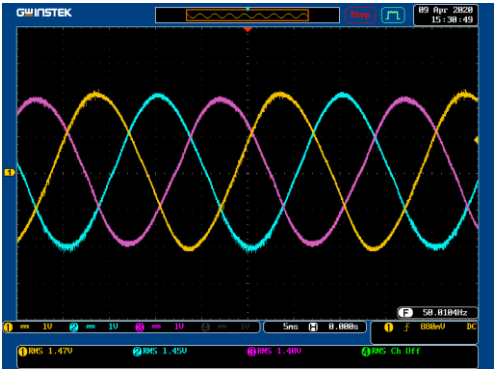
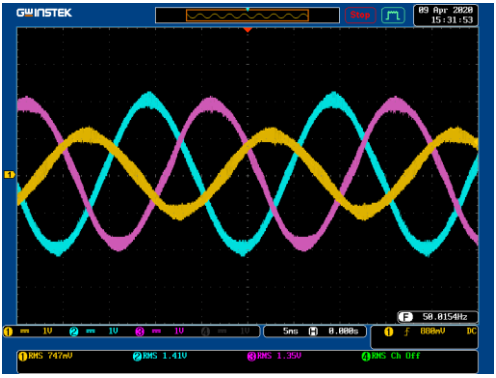



Figure 4.19

Out-of-balanced load output current waveform



Per no-load, half-load and full-load settings of GPL-500, fill in the table 4.1 with the measured values of VOA, VOB, VOC and IOA, respectively. Refer to the table 0.1 for the sensing ratio followed by filling in the actual values.

Table 4.1 Output voltage current measured data in varied load settings of GPL-500

| GPL-500 | $V_{OA}$($V_{rms}$) (Measured value) | $V_{OA}$($V_{rms}$) (Measured value) | $V_{OB}$($V_{rms}$) ((Measured value) | $V_{OB}$($V_{rms}$) (Measured value) | $V_{OC}$($V_{rms}$) (Measured value) | $V_{OC}$($V_{rms}$) (Measured value) |
|---|---|---|---|---|---|---|
| No Load | 1.45V | 29.11V | 1.45V | 29.11V | 1.44V | 28.91V |
| Half load | 1.45V | 29.11V | 1.45V | 29.11V | 1.44V | 28.91V |
| Full load | 1.45V | 29.11V | 1.45V | 29.11V | 1.44V | 28.91V |

| GPL-500 | $I_{OA}$($I_{rms}$) (Measured value) | $I_{OA}$($I_{rms}$) (Measured value) |
|---|---|---|
| No Load | 0.137A | 0.287A |
| Half load | 0.726A | 1.522A |
| Full load | 1.380A | 2.893A |

As the figure 4.1 shown, when GPL-500 changes from no-load to full-load setting, the output current IOA increases gradually and the output voltage VOA, VOB, VOC remain unchanged.

Per out-of-balanced load setting of GPL-500, fill in the table 4.2 with the measured values of VOA, VOB, VOC, IOA, IOB and IOC, respectively. Refer to the table 0.1 for the sensing ratio followed by filling in the actual values.

Table 4.2 Output voltage current measured data in varied load settings of GPL-500

| GPL-500 | $V_{OA}(V_{rms})$ (Measured value) | $V_{OA}(V_{rms})$ (Measured value) | $V_{OB}(V_{rms})$ (Measured value) | $V_{OB}(V_{rms})$ (Measured value) | $V_{OC}(V_{rms})$ (Measured value) | $V_{OC}(V_{rms})$ ((Measured value) |
|---|---|---|---|---|---|---|
| Out-of-balanced load | 1.47V | 29.51V | 1.45V | 29.11V | 1.40V | 28.11V |
| GPL-500 | $I_{OA}(I_{rms})$ (Measured value) | $I_{OA}(I_{rms})$ (Measured value) | $I_{OB}(I_{rms})$ (Measured value) | $I_{OB}(I_{rms})$ (Measured value) | $I_{OC}(I_{rms})$ (Measured value) | $I_{OC}(I_{rms})$ (Measured value) |
| Out-of-balanced load | 0.747A | 1.566A | 1.410A | 2.955A | 1.350A | 2.830A |

As the figure 4.2 shown, when load is out-of-balanced, output voltage remains balanced state. When, however, output current IOA is the half value (1/2) of IOB and IOC current value, output current is out-of-balanced state.

# The Conclusion

Within the Lab4 practical test of independent inverter, output current of inverter increases gradually, during the process from no-load adjusting to full-load state, and output voltage remains unchanged. However, while operating in out-of-balanced load, output current is out-of-balanced state but output voltage remains balanced state.

# Experiment 5 – Three Phase Four Wire PV Grid-connected Inverter

## Circuit Simulation

The circuit parameters of system are as follows:

Battery Voltage Vb = 50V
DC BUS Voltage Vd = 100V
AC Source Voltage $V_{LL}$ = 50Vrms
Fs = 40kHz, Vtri = 10Vpp (DC-DC PWM)
Fs = 20kHz, Vtri = 10Vpp (Inverter PWM)
$C_b$ = 200uF, $L_b$ = 661.5uH, $C_{Bus}$= 470uF
L = 1.02mH, C = 10uF
Ks = 0.24 (DC current sensing factor)
Ks = 0.3 (AC current sensing factor)
Kv = 1/40 (DC voltage sensing factor)
Kv = 1/40 (AC voltage sensing factor)

The analogue circuit diagram based on the parameters above is as the following figure 5.1 shown:
PSIM File: PEK-540_Sim5_3P4W_PV_GC_Inv(50Hz)_V11.1.5_V1.1

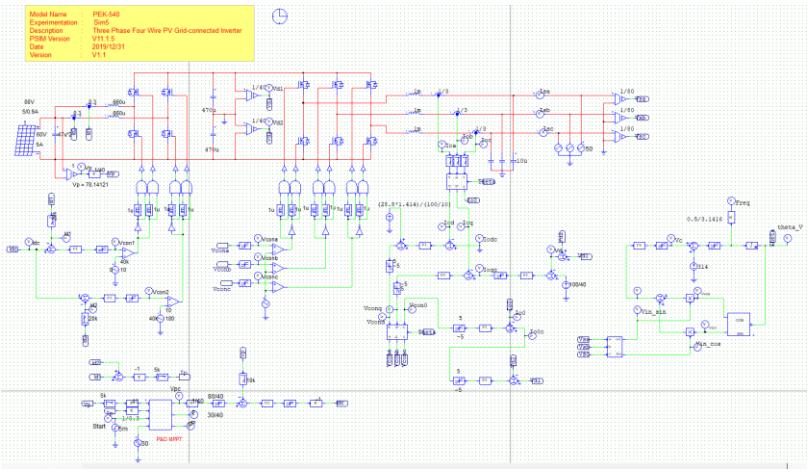



Figure 5.1 Experiment 5 PSIM analogue circuit diagram

The simulation result is shown within the figure 5.2:

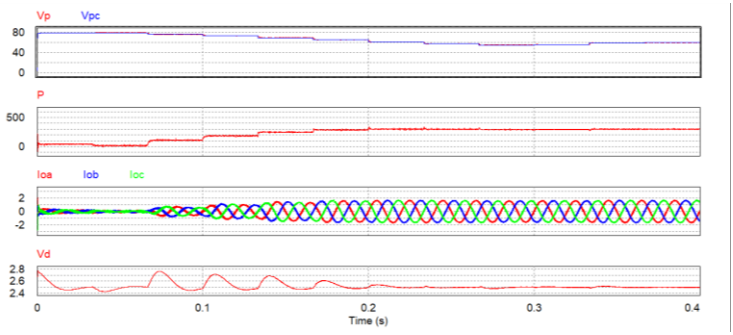



Figure 5.2 Experiment 5 analogue circuit simulation waveforms

The digital circuit diagram based on the analogue circuit is shown as the figure 5.3:
PSIM File: PEK-540_Lab5_3P4W_PV_GC_Inv(50Hz)_V11.1.5_V1.1

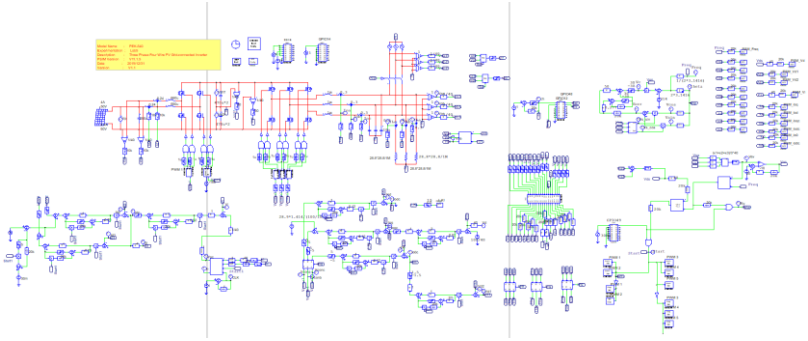


Figure 5.3 Experiment 5 PSIM digital circuit diagram

Due to the fact that to simulate the file, which is the Code circuit with the adjusted frequency of MPPT 1Hz, is time-consuming, we adopt the other file, which is the digital circuit named with "PEK-540_Sim5-1_3P4W_PV_GC_Inv(50Hz)_V11.1.5_V1.1" with the adjusted frequency of MPPT 100Hz, for simulation that results in the prompt result within short time period. See the figure 5.4 for the simulation result.

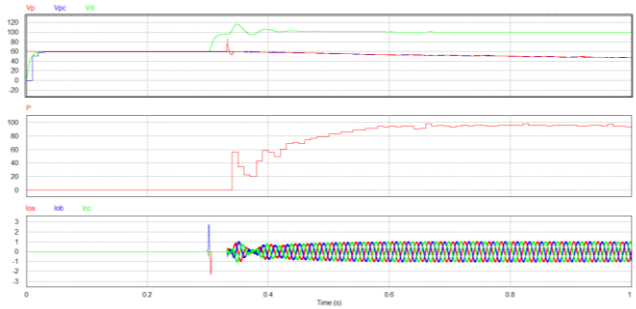


Figure 5.4 Experiment 5 – digital circuit simulation waveforms

After confirming simulation, the corresponding C Code will be generated automatically via "Generate Code" of "Simulate".

# Experiment Devices

The required devices for experiment are as follows:

- PEK-540 * 1
- PEK-005A * 1
- PEK-006 * 1
- PTS-5000 * 1 (with GDS-2204E, PSW160-7.2, APS-300 and GPL-500)
- PC * 1

# Experiment Procedure

1. The experiment wiring is shown as the figure 5.5. Please follow it to complete wiring.

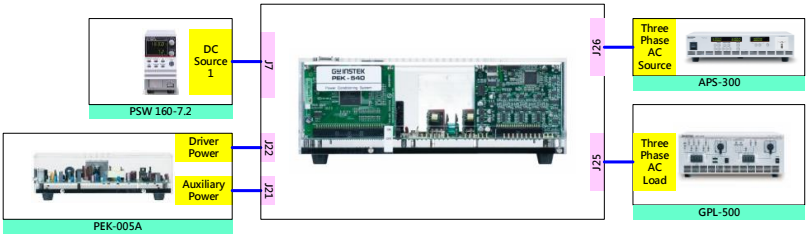



Figure 5.5 Experiment 5 wiring figure

2. After wiring, make sure the PEK-540 switch is OFF followed by turning the PEK-005A switch ON. The DSP red indicator lights on as the figure 5.6 shown, which means the DSP power is steadily normal.


Figure 5.6 DSP normal status with light on

3. Refer to the appendix B for burning procedure.
4. Connect the test leads of oscilloscope to IOA, IOB and IOC respectively, as the figure 5.7 shown.

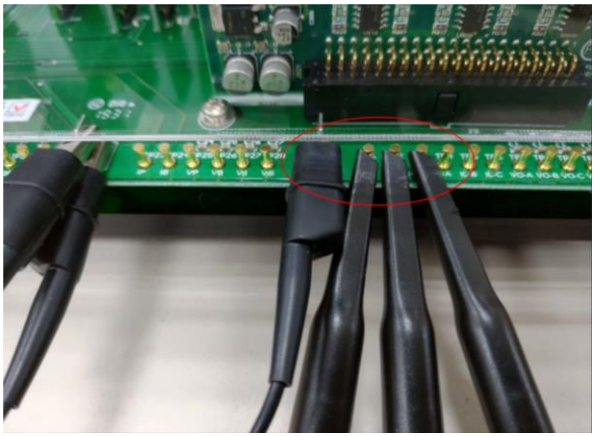


Figure 5.7 Oscilloscope test leads wiring

5. Refer to the appendix D – SAS software operation manual for PV system setting process in simulation. As the figure 5.8 shown, the open circuit voltage of first curve is 60V, and the short circuit current is 4.4A with the MPP voltage 50V along with the MPP current 4A. As the figure 5.9 shown, the value of second curve is set 90% of the first MPP. The open circuit voltage of the second MPP, therefore, is 54V, and the short circuit current is 3.96A with the MPP voltage 45V along with the MPP current 3.6A.

Figure 5.8
The 1st curve setting value

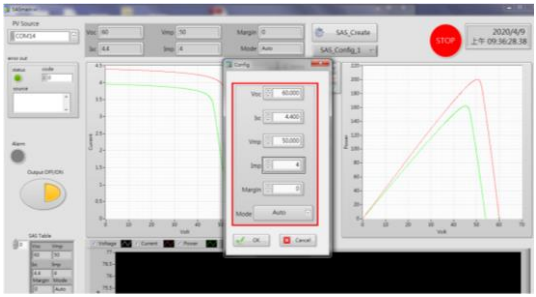
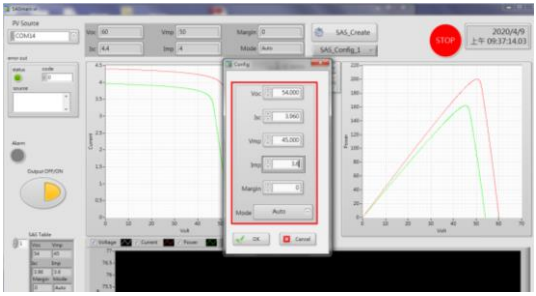
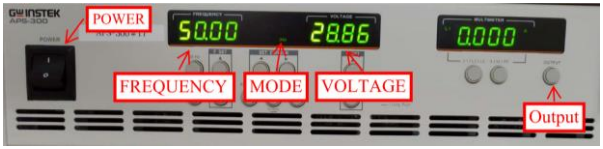


Figure 5.9
The 2nd curve setting value



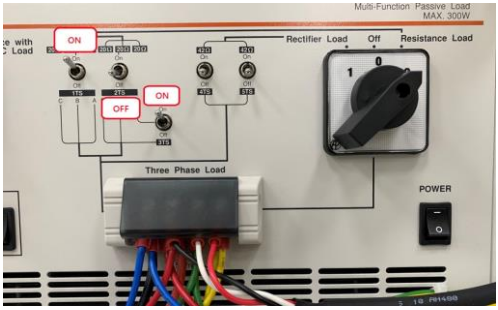
6. The operation process of APS-300 is shown as the figure 5.10. Power on APS-300 → Set 50Hz for APS-300 frequency → Set operation mode as 3P4W → Set output voltage as 28.86V.

Figure 5.10
APS-300 Settings



7. As the figure 5.11 shown, follow the steps below for GPL-500 operation. Power on GPL-500 → Rotate the Three Phase Lord knob to 2 (Resistance Load) → Set 1TS and 3TS as ON, and 2TS as OFF, which indicates half-load mode.

Figure 5.11
GPL-500 half-load Setting




8. After setting up, turn on PSW output via SAS program and open APS-300 output followed by powering on PEK-540 for test.

## The purpose of experiment

This experiment, which is the Grid power system, simulates the pattern of PV panel via PSW 160-7.2, and simulates grid power via APS-300. Observe the power fluctuations between inverter and grid power when this system is under operation.

## The experiment result

1. In the early phase of PSW operation, it is evident that supply to load power is insufficient; therefore, APS-300 output supplements the required power for load. As the figure 5.12 & 5.13 shown, the power provided by PSW is 28.26W, whilst the single phase power provided by APS-300 is 34.8W.

Figure 5.12
Default PSW output power


Figure 5.13
Default APS-300 output power


2. As the figure 5.14 & 5.15 shown, after a period of time of PSW operation, it has seen that load power rises to 105.7W and the single phase power provided by APS-300 lowers down to 12.9W.

Figure 5.14 PSW output power


Figure 5.15 APS-300 output power


3. As the figure 5.16 & 5.17 shown, when the MPP reaches, the PSW output power is 200W and the required power by load is 125W; therefore, APS-300 absorbs the additional output power.

Figure 5.16 MPP PSW output power


Figure 5.17 MPP APS-300 output power

Owning to the fact that the power-voltage curve of PV panel constantly fluctuates in accordance with the environmental and external factors, we have managed to make sure inverter remains the maximum power output in any given environmental conditions, via 2 curves alternation, to meet the highest utilization rate. As the figure 5.18 & 5.19 shown, it is clear that the output power of arbitrary curves alternation is approaching the maximum power output point and remains steadily.

Figure 5.18

SAS lies in the maximum power point of the 1st curve

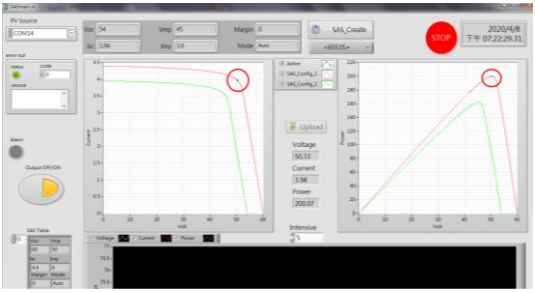
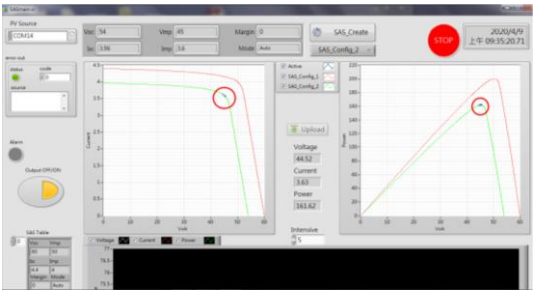


Figure 5.19

SAS lies in the maximum power point of the 2nd curve



# The Conclusion

This experiment is executed on the basis of operations of PV inverter and power grid in parallel, jointly providing power and passing to load. When the power provided by PV inverter is insufficient, power grid supplements the required power for load. Also, when power of PV inverter is sufficient to supply load, the redundant electrical energy can be sent to power grid.

# Experiment 6 – Three Phase Four Wire Battery Energy Storage System

## Circuit Simulation

The circuit parameters of system are as follows:

Battery Voltage Vb = 50V
DC BUS Voltage Vd = 100V
AC Source Voltage $V_{LL}$ = 50Vrms
Fs = 40kHz, Vtri = 10Vpp (DC-DC PWM)
Fs = 20kHz, Vtri = 10Vpp (Inverter PWM)
$C_b$ = 200uF, $L_b$ = 661.5uH, $C_{Bus}$= 470uF
L = 1.02mH, C = 10uF
Ks = 0.24 (DC current sensing factor)
Ks = 0.3 (AC current sensing factor)
Kv = 1/40 (DC voltage sensing factor)
Kv = 1/40 (AC voltage sensing factor)

The analogue circuit diagram based on the parameters above is as the following figures 6.1, 6.3 & 6.5 shown:
PSIM File: PEK-540_Sim6-1_3P4W_BESS_EXT(50Hz)_V11.1.5_V1.1

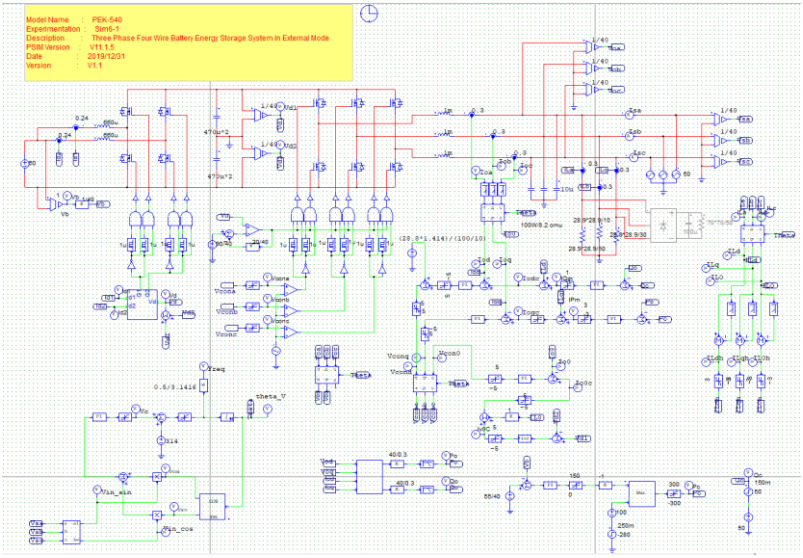



Figure 6.1 Experiment 6 PSIM analogue circuit diagram

The simulation result is shown within the figure 6.2:

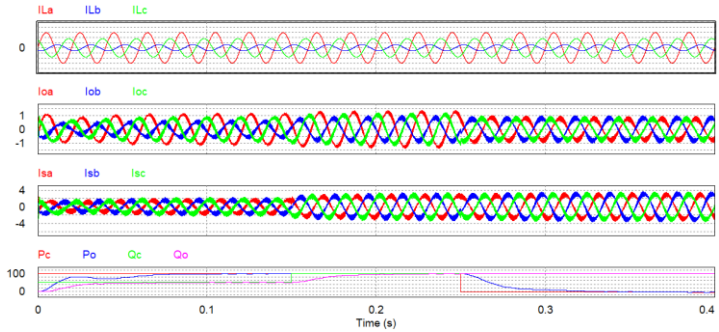



Figure 6.2 Experiment 6 analogue circuit simulation waveforms

PSIM File: PEK-540_Sim6-2_3P4W_BESS_PQ(50Hz)_V11.1.5_V1.1

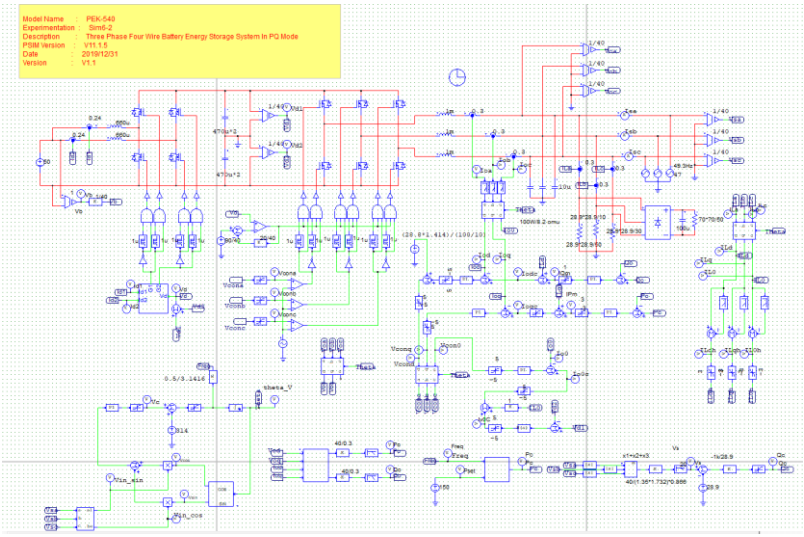



Figure 6.3 Experiment 6 PSIM analogue circuit diagram

The simulation result is shown within the figure 6.4:

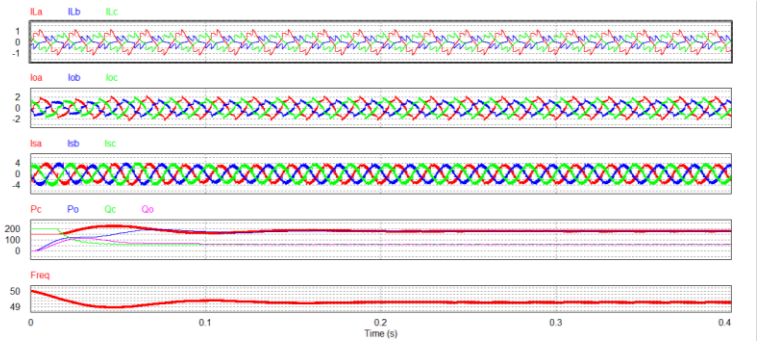



Figure 6.4 Experiment 6 analogue circuit simulation waveforms

PSIM File: PEK-540_Sim6-3_3P4W_BESS_SA(50Hz)_V11.1.5_V1.1

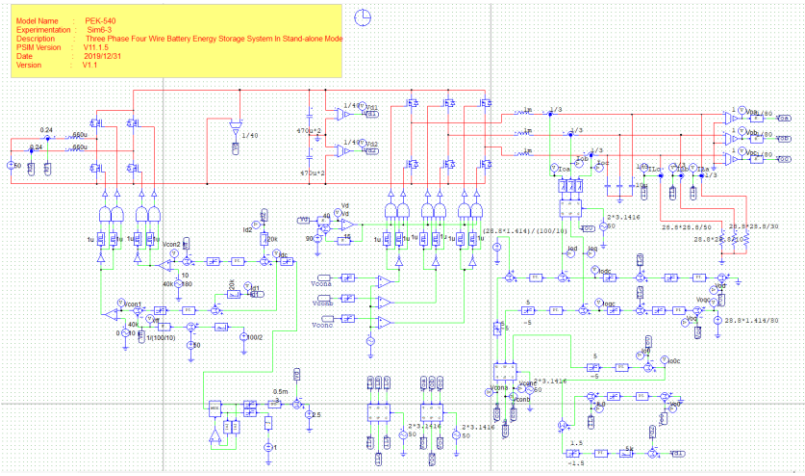



Figure 6.5 Experiment 6 PSIM analogue circuit diagram

The simulation result is shown within the figure 6.6:

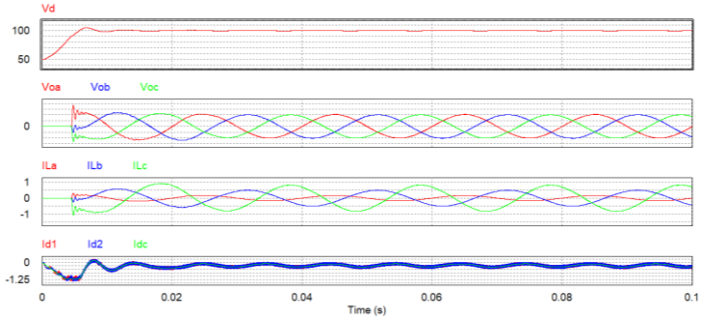



Figure 6.6 Experiment 6 analogue circuit simulation waveforms

The digital circuit diagram based on the analogue circuit is shown as the figure 6.7:
PSIM File: PEK-540_Lab6_3P4W_BESS(50Hz)_V11.1.5_V1.1

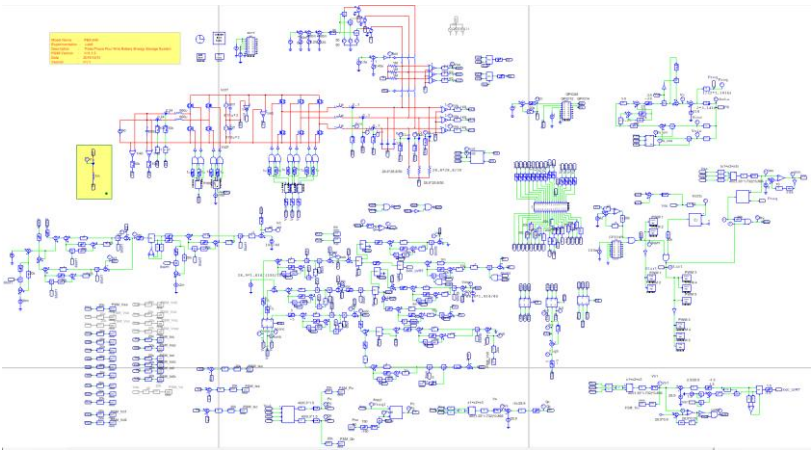


Figure 6.7 Experiment 6 PSIM digital circuit diagram

The simulation result is shown within the figure 6.8:

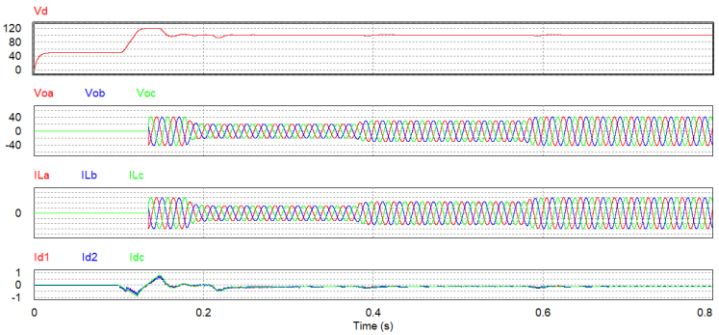



Figure 6.8 Experiment 6 digital circuit simulation waveforms

After confirming simulation, the corresponding C Code will be generated automatically via “Generate Code” of “Simulate”.

# Experiment Devices

The required devices for experiment are as follows:

- PEK-540 * 1
- PEK-005A * 1
- PEK-006 * 1
- PTS-5000 * 1 (with GDS-2204E, PSW160-7.2, APS-300, PEL-3031E and GPL-500)
- PC * 1

# Experiment Procedure

1. The experiment wiring is shown as the figure 6.9. Please follow it to complete wiring.

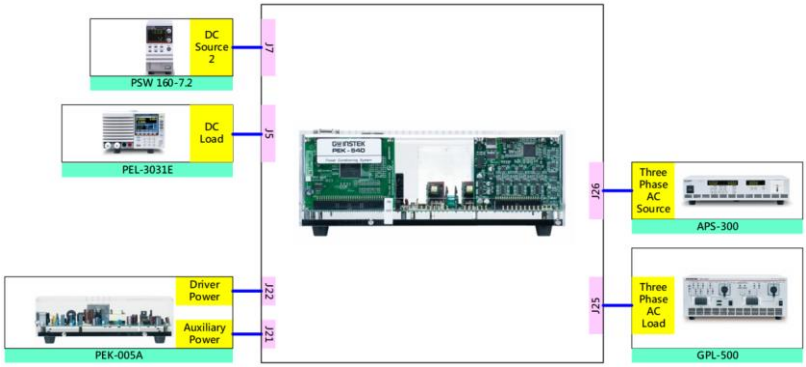



Figure 6.9 Experiment 6 wiring figure

2. After wiring, make sure the PEK-540 switch is OFF followed by turning the PEK-005A switch ON. The DSP red indicator lights on as the figure 6.10 shown, which means the DSP power is steadily normal.


Figure 6.10 DSP normal status with light on

3. Refer to the appendix B for burning procedure.
4. Connect the test leads of oscilloscope to VOA, VOB, VOC and IOA, respectively, as the figure 6.11 shown.

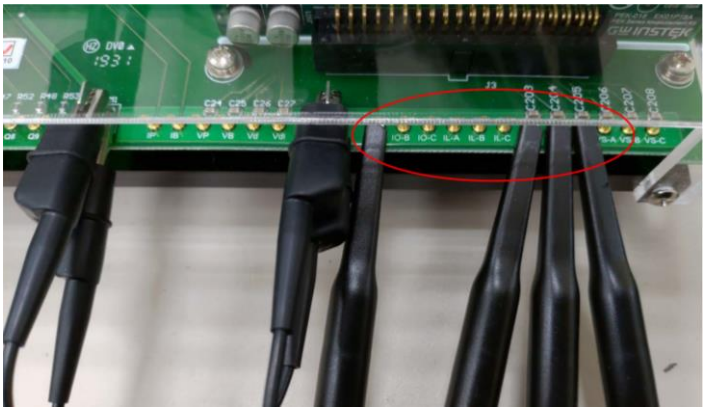
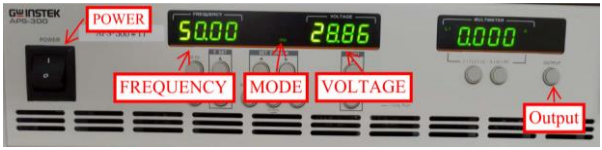


Figure 6.11 Oscilloscope test leads wiring

5. The operation process of APS-300 is shown as the figure 6.12. Power on APS-300 → Set 50Hz for APS-300 frequency → Set operation mode as 3P4W → Set output voltage as 28.86V → Activate APS-300 Output after everything is confirmed.

Figure 6.12

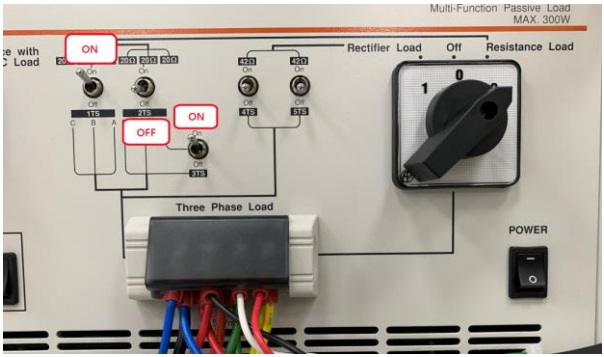
The setting of APS-300




6. As the figure 6.13 shown, follow the steps below for GPL-500 operation. Power on GPL-500 → Rotate the Three Phase Lord knob to 2 (Resistance Load) → Set 2TS as OFF, and 1TS and 3TS as ON, which indicates half-load mode.

Figure 6.13

GPL-500 half-load setting

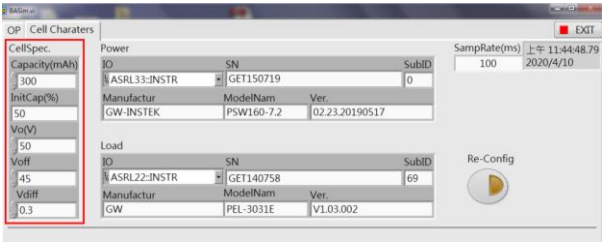



7. Proceed to connection step in accordance with the appendix C – RS232 Connection.

8. Refer to the appendix E – BATSim operation manual for detailed setting. As the figure 6.14 shown, set 300mAh for battery capacity, which is 50% by default capacity. The voltage in full charge is 50V, whilst it is 45V for full discharge. The voltage difference of internal charge and discharge is 0.5V.

Figure 6.14

Batter simulation parameter setting




9. After setting up the instrument with confirmation, activate both PSW and PEL power output via BATSim followed by powering on APS-300 output. Lastly, turn On PEK-540 .

# The purpose of experiment

This experiment, which is the battery power storage system, simulates battery via PSW 160-7.2 and PEL-3031E, and simulates grid power via APS-300. Observe both power and waveform fluctuations between inverter and grid power when this system is under operation.

# The experiment result

## Battery Discharge Mode

As the figure 6.15 shown, the default setting of inverter output power Poc is 50 with the DSP oscilloscope displaying waveforms of output voltage and current of inverter. The figure 6.16 displays that while inverter output voltage VOA and output current IOA are in-phase state, VOA output RMS voltage is 1.43V (28.71V in actual value), and VOB output RMS voltage is 1.43V (28.71V in actual value), and VOC output RMS voltage is 1.41V (28.31V in actual value),and IOA output RMS current is 0.331A (0.693A in actual value).Through the status of battery we can realize the battery power is passed to grid power and load via inverter, which is the so-called discharge mode.

Figure 6.15

Command parameters Poc set in 50

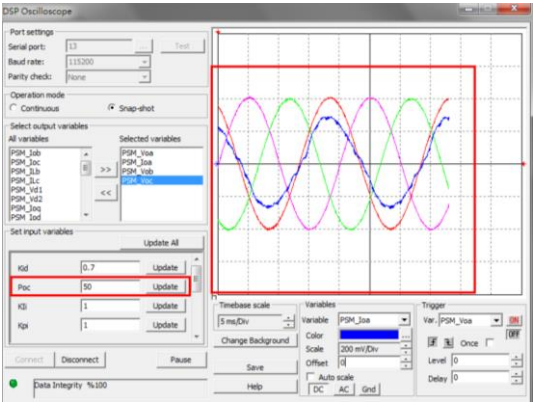


Figure 6.16

Measured waveform of command parameters Poc set in 50

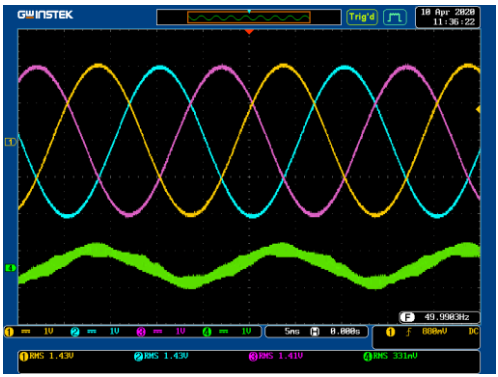


Figure 6.17

Battery status of command parameters Poc set in 50


## Battery Charge Mode

As the figure 6.18 shown, the inverter output power command parameter Poc is set in -50 with the DSP oscilloscope displaying waveforms of output voltage and current of inverter. The figure 6.19 displays that while inverter output voltage VOA and output current IOA are anti-phase state, VOA output RMS voltage is 1.43V (28.71V in actual value), and VOB output RMS voltage is 1.42V (28.51V in actual value), and VOC output RMS voltage is 1.42V (28.51V in actual value), and IOA output RMS current is 0.280A (0.587A in actual value).As the figure 6.20 shown, through the status of battery we can realize that grid power offers the power to both battery and load, which is the so-called charge mode.

Figure 6.18

Command parameters Poc set in -50

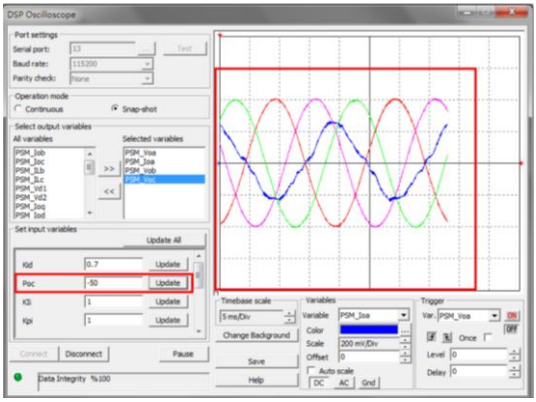



Figure 6.19

Measured waveform of command parameters Poc set in -50

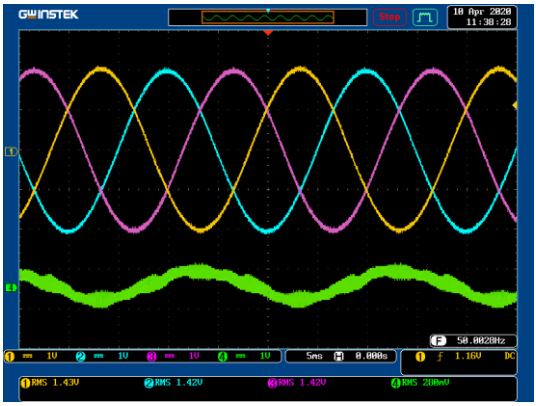



Figure 6.20

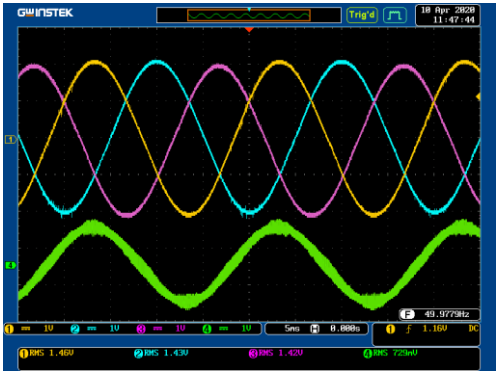
Battery status of command parameters Poc set in -50

## Inverter Independent Mode (balanced half-load)

Adjust Poc setting back to 50 followed by powering off APS-300 and the inverter under independent mode is powered by battery. The figure 6.21 shows that VOA output RMS voltage is 1.46V (29.31V in actual value), and VOB output RMS voltage is 1.43V (28.71V in actual value), and VOC output RMS voltage is 1.42V (28.51V in actual value), and IOA output RMS current is 0.729A (1.528A in actual value).

Figure 6.21

Measured waveform of inverter independent mode

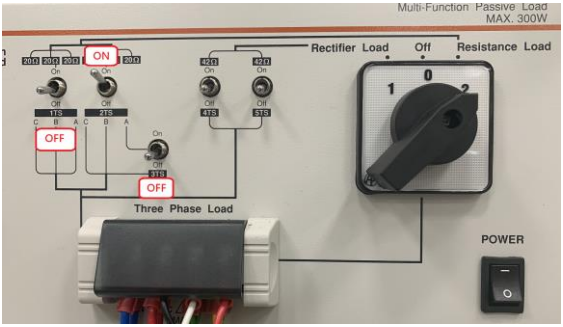



## Inverter independent mode (out-of-balanced mode Ra/Rb/Rc = ∞/20/20Ω)

As the figure 6.22 shown, adjust GPL-500 to out-of-balanced mode and rotate the knob to Resistance Load followed by setting 2TS as ON and 1TS with 3TS as OFF.

Figure 6.22

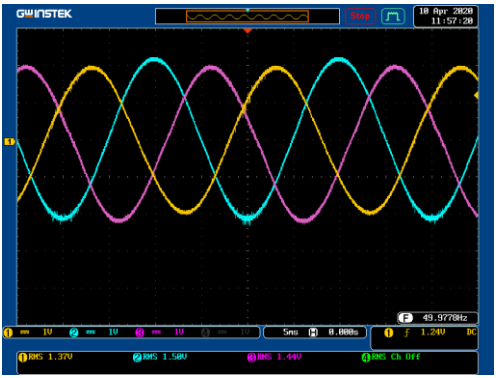
GPL-500 out-of-balanced mode setting




As the figure 6.23 shown, when load is out-of-balanced, output voltage of inverter is still balanced.

Figure 6.23

Measured voltage output waveform of load out-of-balanced mode



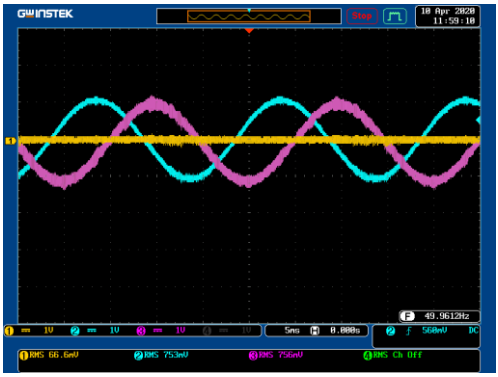
As the figure 6.24 shown, connect the test leads to the load current ILA, ILB and ILC. Also, the figure 6.25 shows that ILA is zero and therefore three phase current is in out-of-balanced state.

Figure 6.24

Oscilloscope test leads wiring (out-of-balanced ILA, ILB, ILC)

Figure 6.25

Measured current output waveform of load out-of-balanced mode




## Active power filter

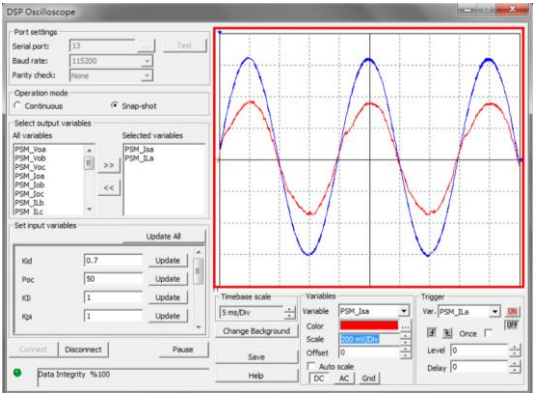
Select PSM_ISA (grid power) and PSM_ILA (load) for

DSP oscilloscope waveform.

As the figure 6.13 shown, adjust GPL-500 to resistive half-load and turn on APS-300. The figure 6.26 shows that both grid power and load current are sine waves.

Figure 6.26

Grid power and load current of resistive load




As the figure 6.27 shown, adjust GPL-500 to Rectifier Load and set 4TS as ON and 5TS as OFF, which indicates the non-linear load. As the figure 6.28 shown, though load current is the non-linear current, the grid power current can be rectified to be nearly sine wave via the active power rectification of inverter.

Figure 6.27

GPL-500 non-linear load setting

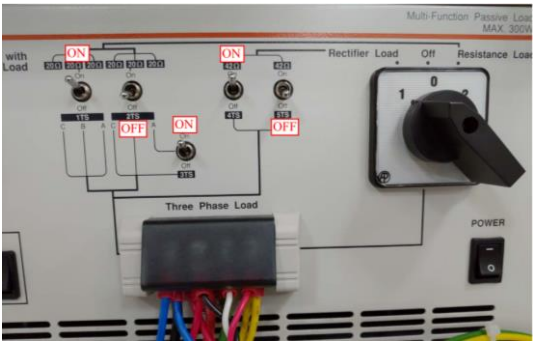
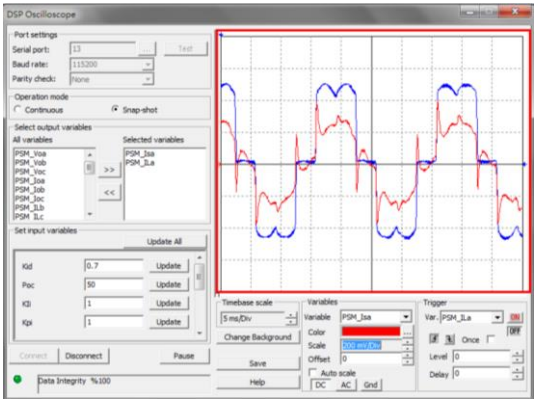


Figure 6.28

Non-linear grid power and load current




Under the condition of half-load of independent mode, fill in the table 6.1 with the measured VOA, VOB, VOC and IOA RMS values in order. Refer to the table 0.1 for the sensing ratio.

Table 6.1 Three phase output voltage current measured data under the condition of half-load of independent mode

| GPL-500 | VOA(Vrms) (Measured value) | VOA(Vrms) (Measured value) | VOB(Vrms) (Measured value) | VOB(Vrms) (Measured value) | VOC(Vrms) (Measured value) | VOC(Vrms) (Measured value) |
|---|---|---|---|---|---|---|
| Half Load | 1.46V | 29.31V | 1.43V | 28.71V | 1.42V | 28.51V |

| GPL-500 | IOA(Irms) (Measured value) | IOA(Irms) (Measured value) |
|---|---|---|
| Half Load | 0.729A | 1.528A |

Under the condition of out-of-balanced of independent mode, fill in the table 6.2 with the measured VOA, VOB, VOC, ILA, ILB and IC RMS values in order. Refer to the table 0.1 for the sensing ratio.

Table 6.2 Three phase output voltage current measured data under the condition of out-of-balanced of independent mode

| GPL-500 | VOA(Vrms) (Measured value) | VOA(Vrms) (Measured value)) | VOB(Vrms) (Measured value) | VOB(Vrms) (Measured value) | VOC(Vrms) (Measured value) | VOC(Vrms) (Measured value) |
|---|---|---|---|---|---|---|
| Out-of-balanced Load | 1.37V | 27.51V | 1.50V | 30.12V | 1.44V | 28.91V |

| GPL-500 | $I_{LA}$(Irms) (Measured value) | $I_{LA}$(Irms) (Measured value) | $I_{LB}$(Irms) (Measured value) | $I_{LB}$(Irms) (Measured value) | $I_{LC}$(Irms) (Measured value) | $I_{LC}$(Irms) (Measured value) |
|---|---|---|---|---|---|---|
| Out-of-balanced Load | 0A | 0A | 0.753A | 1.578A | 0.756A | 1.584A |

From the table 6-1 & 6-2, it is clear that in the independent mode, whether load is balanced or out-of-balanced, three phase output voltage is still approaching balanced state.

## The conclusion

A. This experiment, which is equipped with battery charge/discharge mode, passes battery power to load when battery is in discharge mode. However, when battery is in charge mode, grid power will be responsible for passing power to load and, in the meantime, charging to battery.

B. When grid power is cut off, the system switches to independent mode in which the battery passes power to load. If any change occurs in load, inverter can maintain balance of output voltage.

C. When it is under grid-connected mode and load is non-linear, the grid power current waveform, via the active power filter of inverter, will be compensated to nearly sine wave.

# Experiment 7 – Three Phase Four Wire Hybrid System

## Circuit Simulation

The converter specification is as follows:

Battery Voltage Vb = 50V
PV Voltage Vp = 50V
DC BUS Voltage Vd = 100V
AC Source Voltage $V_{LL}$ = 50Vrms
Fs = 40kHz, Vtri = 10Vpp (DC-DC PWM)
Fs = 20kHz, Vtri = 10Vpp (Inverter PWM)
$C_b$ = 200uF, $L_b$ = 661.5uH, $C_{Bus}$= 470uF
L = 1.02mH, C = 10uF
Ks = 0.24 (DC current sensing factor)
Ks = 0.3 (AC current sensing factor)
Kv = 1/40 (DC voltage sensing factor)
Kv = 1/40 (AC voltage sensing factor)

The analogue circuit diagram based on the parameters above is as the following figure 7.1 shown:
PSIM File: PEK-540_Sim7_3P4W_Hybrid(50Hz)_V11.1.5_V1.1

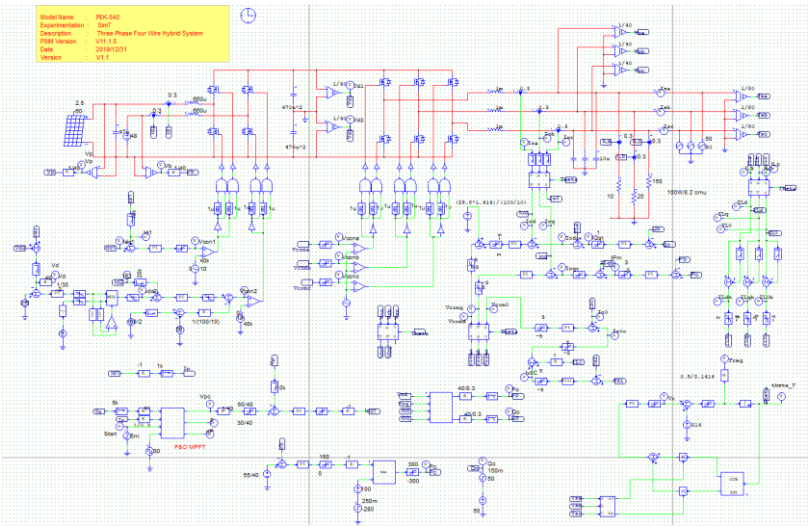


Figure 7.1 Experiment 7 - PSIM analogue circuit diagram

The simulation result is shown within the figure 7.2 and 7.3:

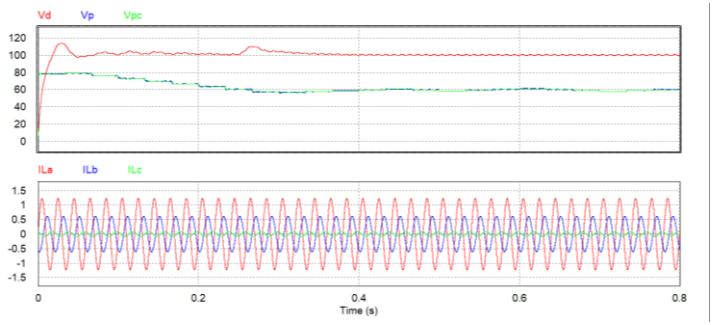



Figure 7.2 Experiment 7 analogue circuit simulation waveforms

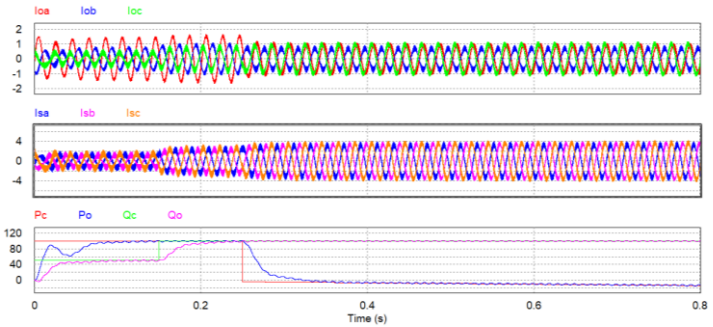



Figure 7.3 Experiment 7 analogue circuit simulation waveforms

The digital circuit diagram based on the analogue circuit is shown as the figure 7.4:
PSIM File: PEK-540_Lab7_3P4W_Hybrid(50Hz)_V11.1.5_V1.2

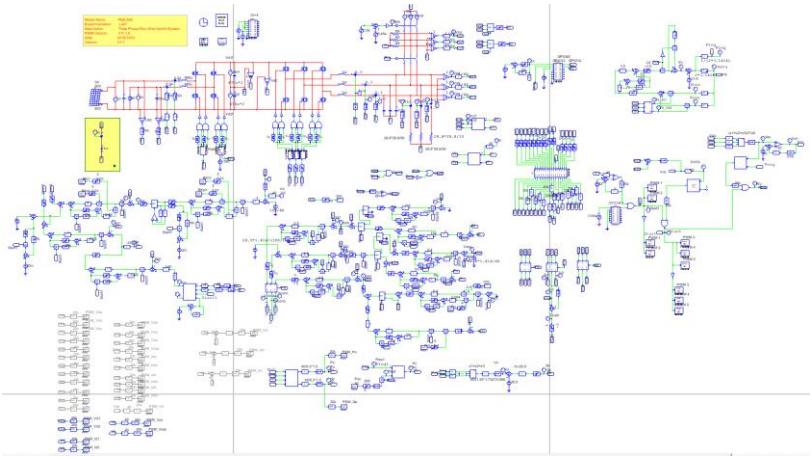


Figure 7.4 Experiment 7 PSIM digital circuit diagram

Because the generated Code circuit with MPPT adjusted frequency 1Hz consumes much longer time for simulation, we instead provide the other digital circuit, "PEK-540_Sim7D_3P4W_Hybrid(50Hz)_V11.1.5_V1.1", with adjusted MPPT frequency 100Hz for simulation that consumes less time for practical result. Refer to the figure 7.5 & 7.6 for the simulation result.

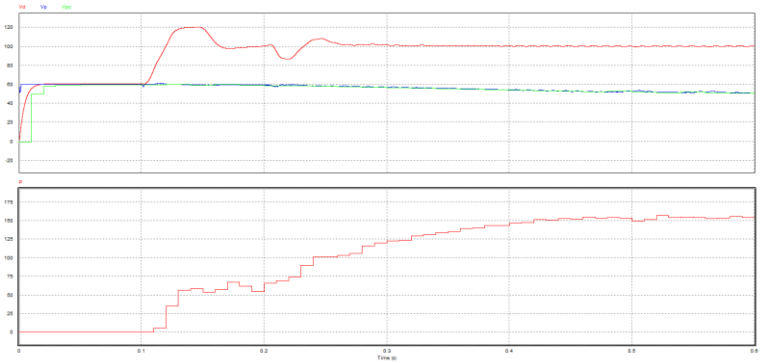


Figure 7.5 Experiment 7 digital circuit simulation waveforms

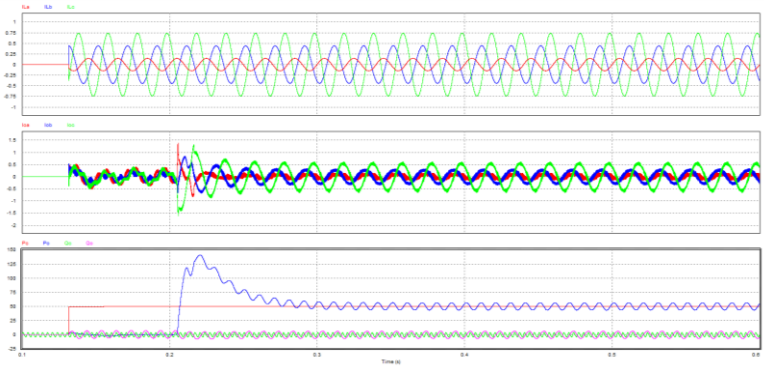


Figure 7.6 Experiment 7 digital circuit simulation waveforms

After confirming simulation, the corresponding C Code will be generated automatically via “Generate Code” of “Simulate”.

# Experiment Devices

The required devices for experiment are as follows:

- PEK-540 * 1
- PEK-005A * 1
- PEK-006 * 1
- PTS-5000 * 1 (with GDS-2204E, PSW160-7.2*2, PEL-3031E, APS-300 and GPL-500)
- PC * 1

# Experiment Procedure

1. The experiment wiring is shown as the figure 7.7. Please follow it to complete wiring.

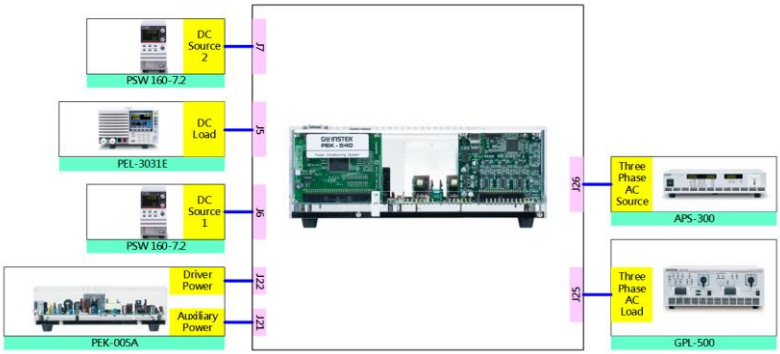



Figure 7.7 Experiment wiring figure

2. After wiring, make sure the PEK-540 switch is OFF followed by turning the PEK-005A switch ON. The DSP red indicator lights on as the figure 7.8 shown, which means the DSP power is steadily normal.


Figure 7.8 DSP normal status with light on

3. Refer to the appendix B for burning procedure.
4. Connect the test leads of oscilloscope to VOA, VOB, VOC and IOA, respectively, as the figure 7.9 shown.

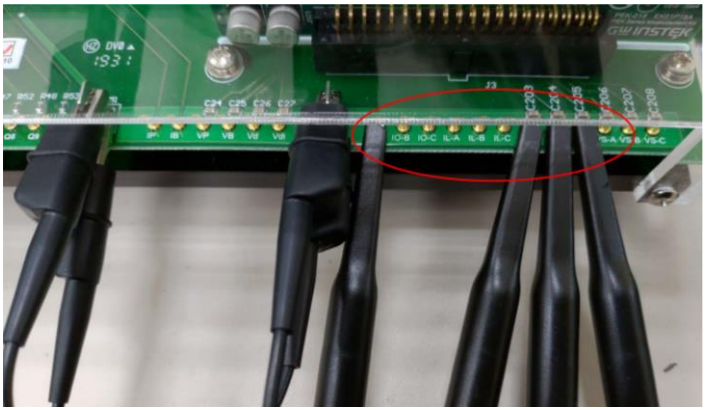


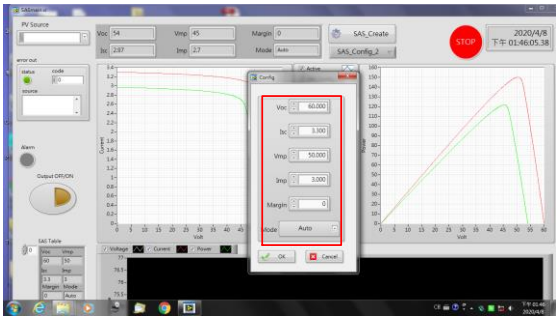
Figure 7.9 Oscilloscope test leads wiring

5. Refer to the appendix D – SAS software operation manual for the setting process of simulation PV panel. As the figure 7.10 shown, the open circuit voltage of the 1st curve is 60V, and the short circuit current is 3.3A, and the maximum power point voltage is 50V, and the maximum power point current is 3A. On the other

hand, the 2nd curve setting is 90% of that of the 1st curve.

Figure 7.10

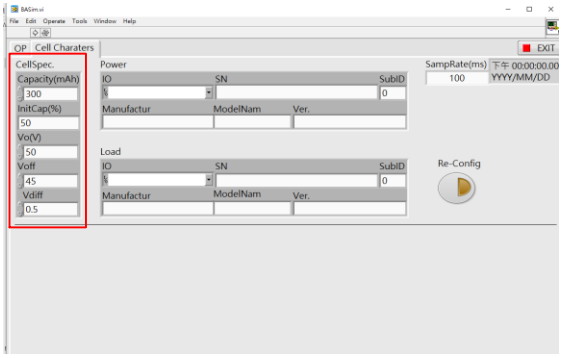
The 1st curve setting



6. Refer to the appendix E – BATSim software operation manual for the setting process of simulation battery. As the figure 7.11 shown, set 300mAh for battery capacity, which is 50% by default capacity. The voltage in full charge is 50V, whilst it is 45V for full discharge. The voltage difference of internal charge and discharge is 0.5V.

Figure 7.11

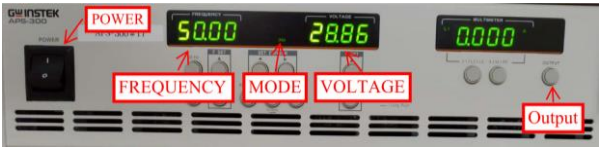
Battery simulation parameter setting




7. As the figure 7.12 shown, power on APS-300 and set 50Hz for frequency, 3P4W for mode, 28.86V for output voltage.

Figure 7.12

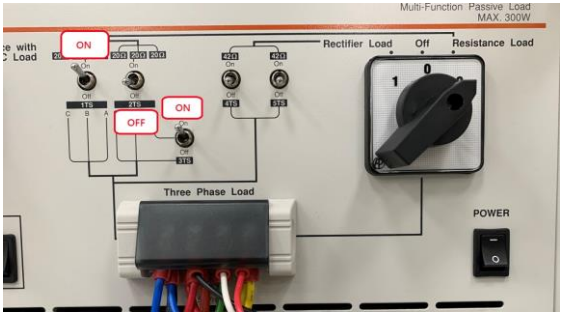
The setting of APS-300



8. As the figure 7.13 shown, power on GPL-500 and rotate the Three Phase Lord knob to 2 (Resistance Load). Set 1TS and 3TS as ON, and 2TS as OFF, which indicates the half-load mode. Please note that this experiment can only be executed when load is under half-load mode.

Figure 7.13

GPL-500 half-load setting




9. After setting up, turn on PSW and PEL output via SAS and BATSim programs and also open APS-300 output followed by powering on PEK-540 for test.

# The purpose of experiment

This experiment, which is the hybrid inverter system of PV and battery, further describes the modes of PV and battery in the inverter system.

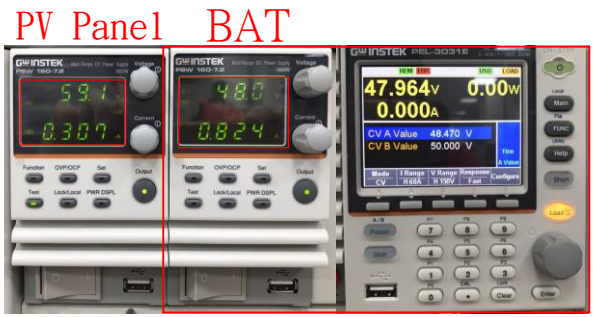
# The experiment result

## Battery Discharge Mode

As the figure 7.14 shown, when powering on, due to the fact that the PV panel is Not able to provide load with enough power, the battery and grid power will supply the insufficient power instead, which is the so-called discharge mode.

Figure 7.14

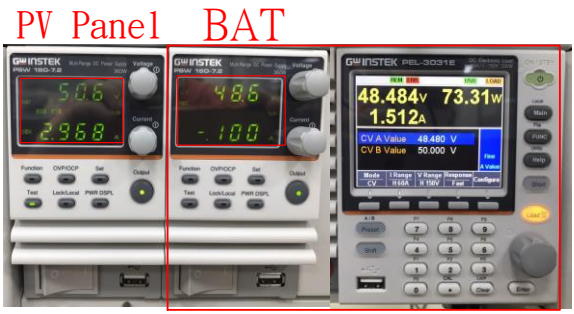
BAT in discharge state



## Battery Charge Mode

As the figure 7.15 shown, when PV panel is the maximum power point output, due to the fact that the power is able to provide load with sufficient power, the redundant power will be recharged back to battery storage, which is the so-called charge mode.

Figure 7.15
BAT in charge state




As the figure 7.16 & 7.17 shown, during the experiment process, we simulate different curves by varied sun exposures from the 2 differed PV curves by default. The 2 curves can switch at any time and head toward the maximum power point in the end, individually.

Figure 7.16

SAS in the maximum power point of the 1st curve

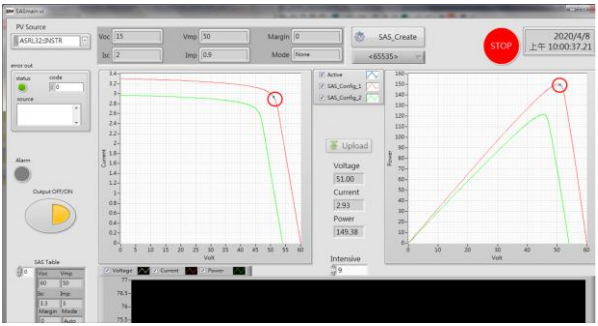
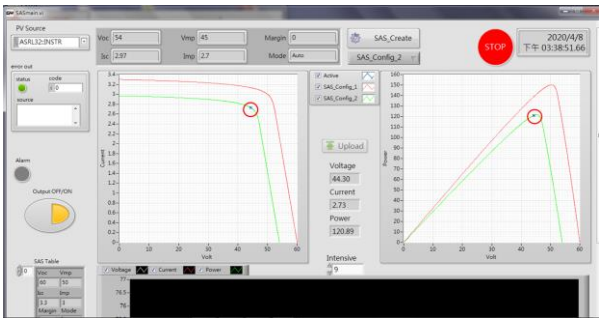


Figure 7.17

SAS in the maximum power point of the 2nd curve

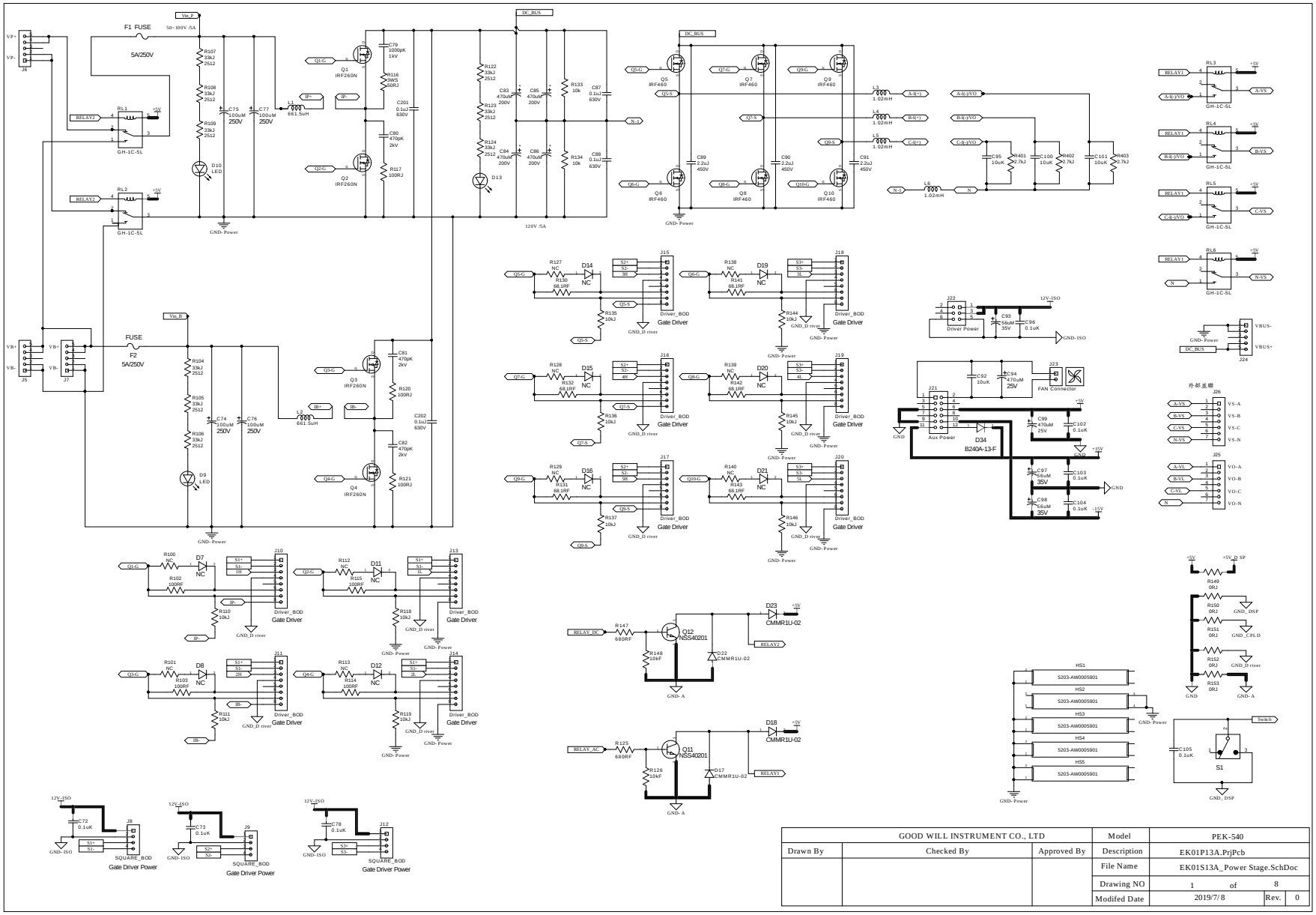


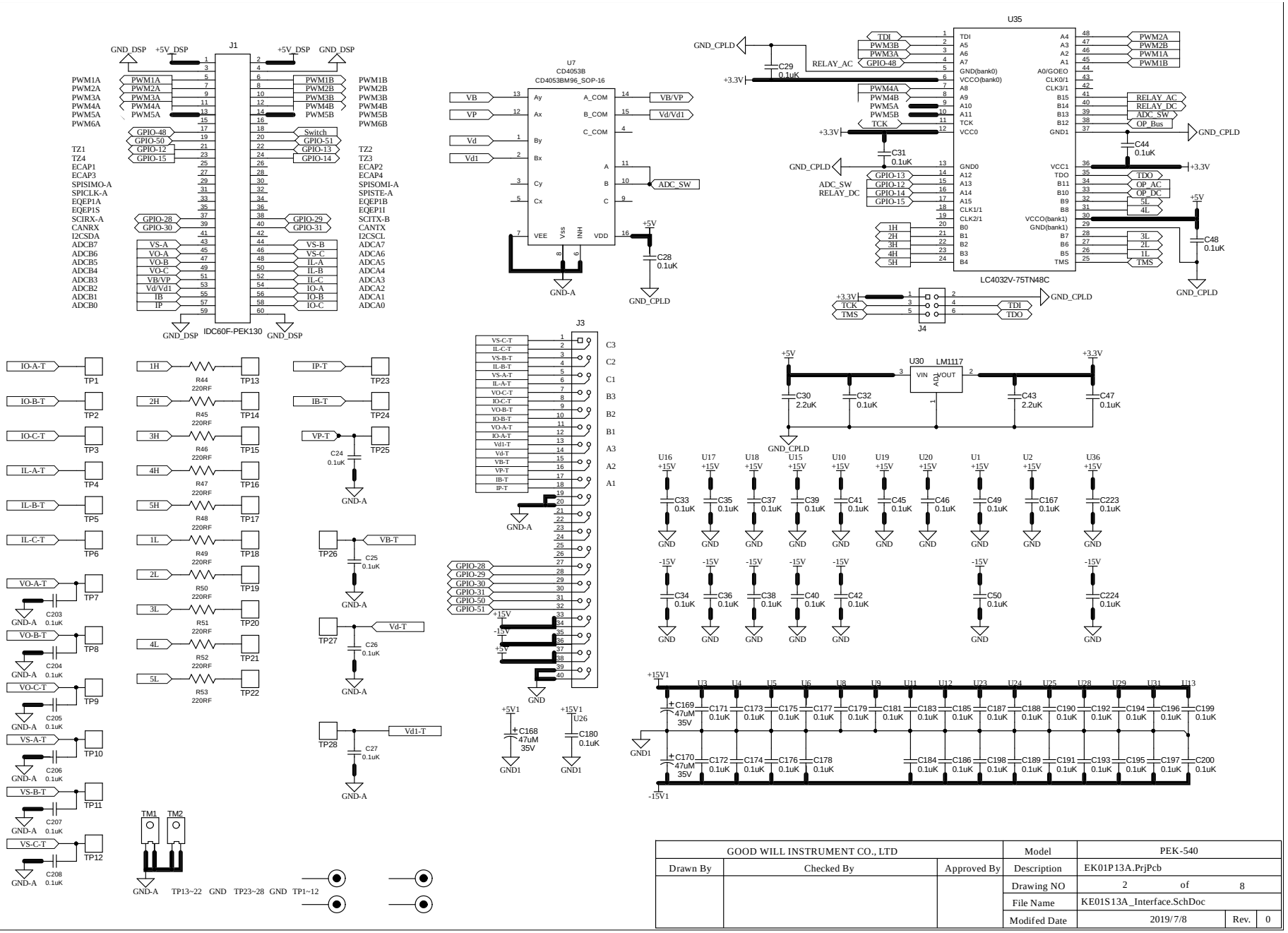

# The Conclusion

We can clearly understand that, though the experiment, the power provided by PV panel is determined by the external factors. When the power provided to load is insufficient, battery will adapt into discharge state, which compensates the insufficient power required by load. While, on the other hand, the power provided by PV panel is way excessive, battery will adapt into charge state, which practically stores the redundant power.

# Appendix A – PEK-540 Circuit Diagram

# Power Conditioning System



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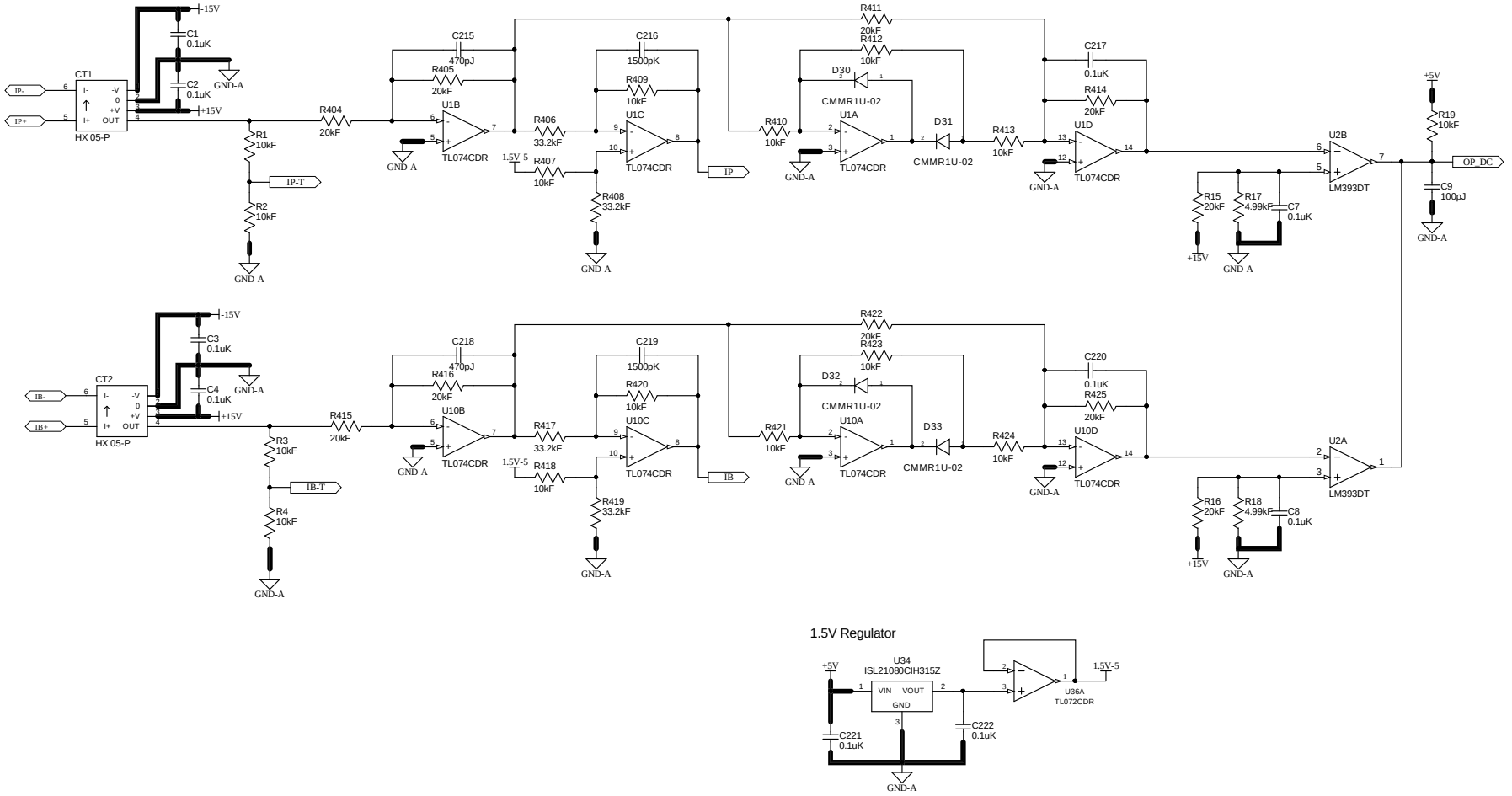
| | | | Modifed Date | 2019/7/8 Rev. 0 |

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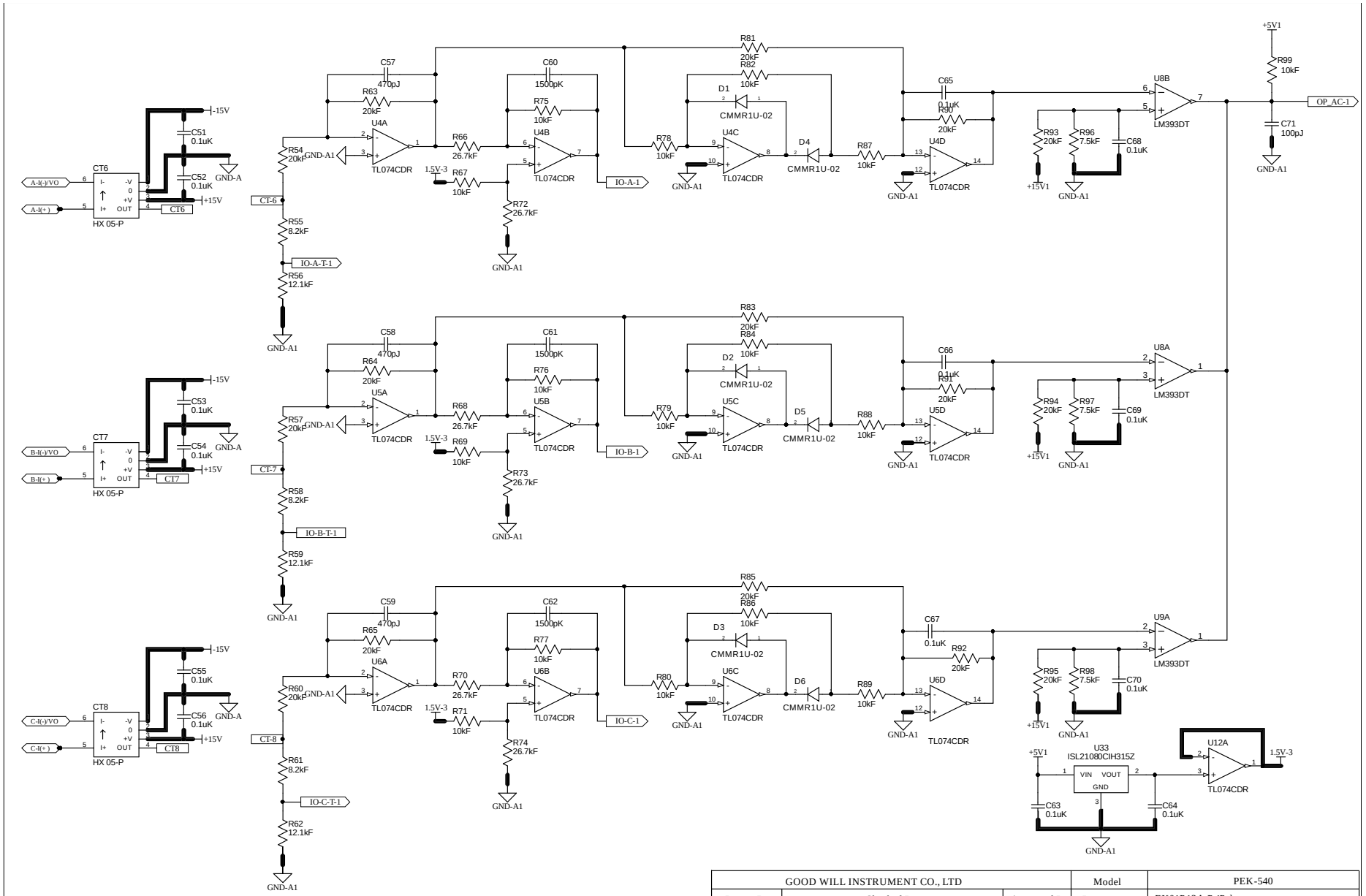


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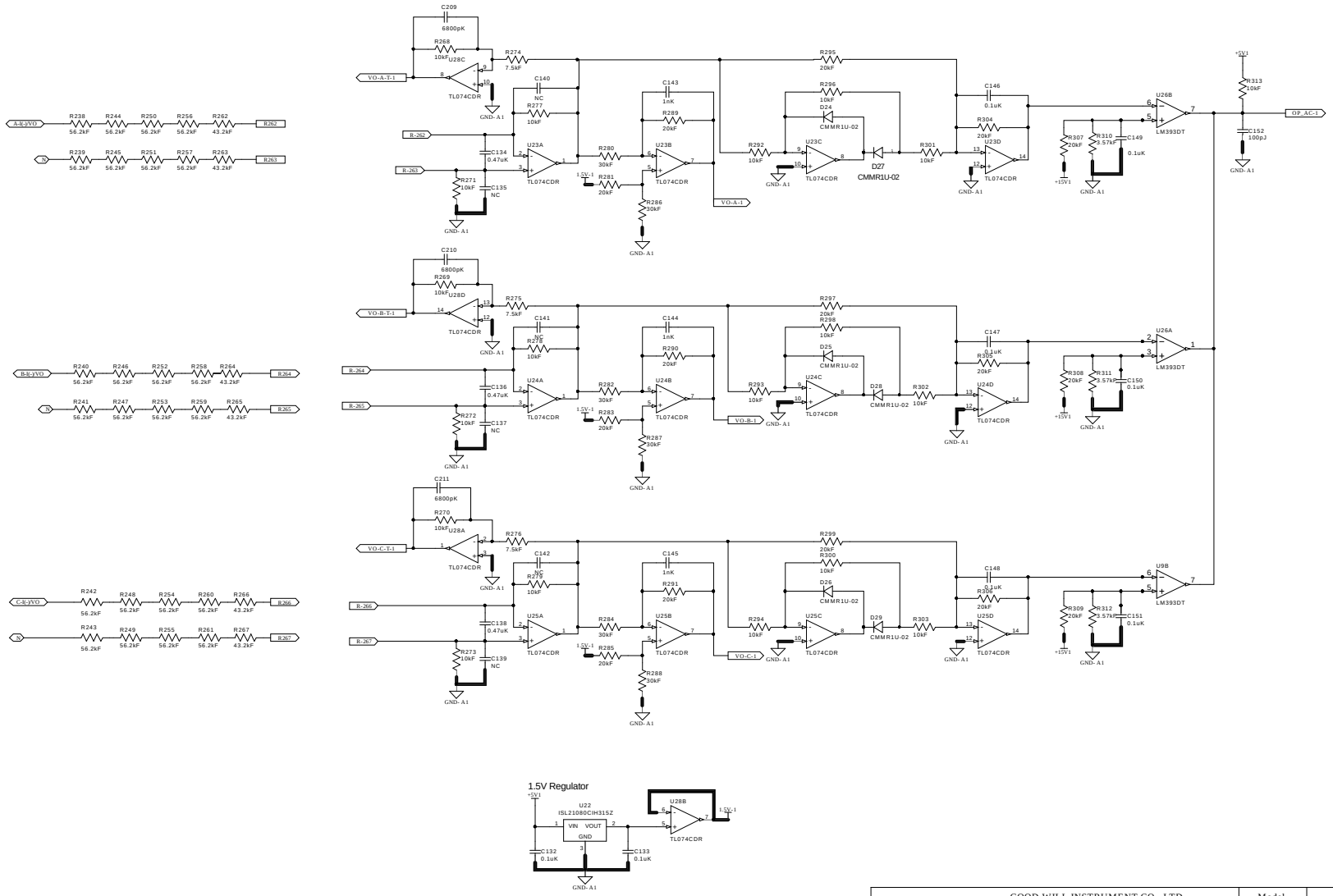


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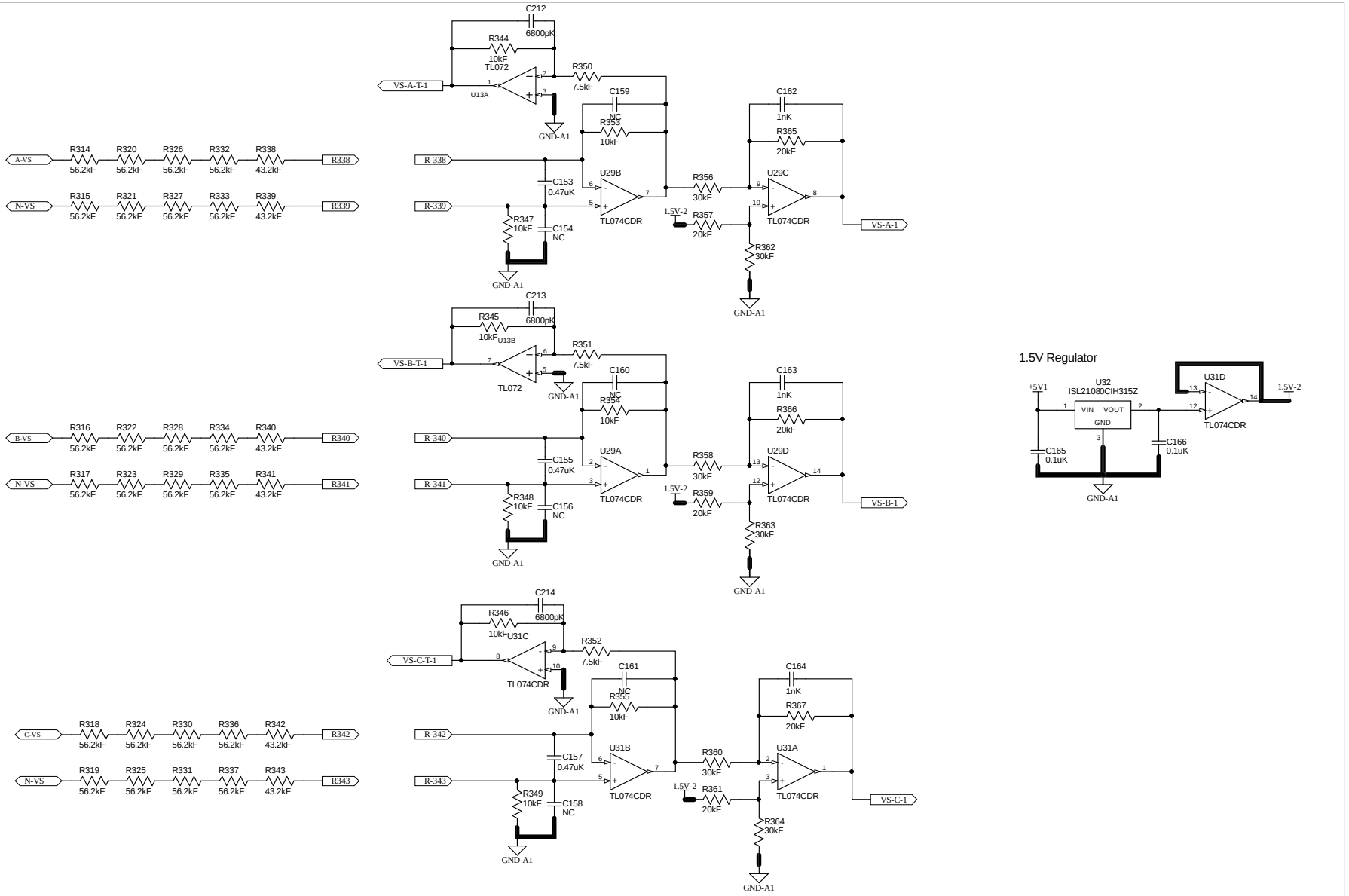


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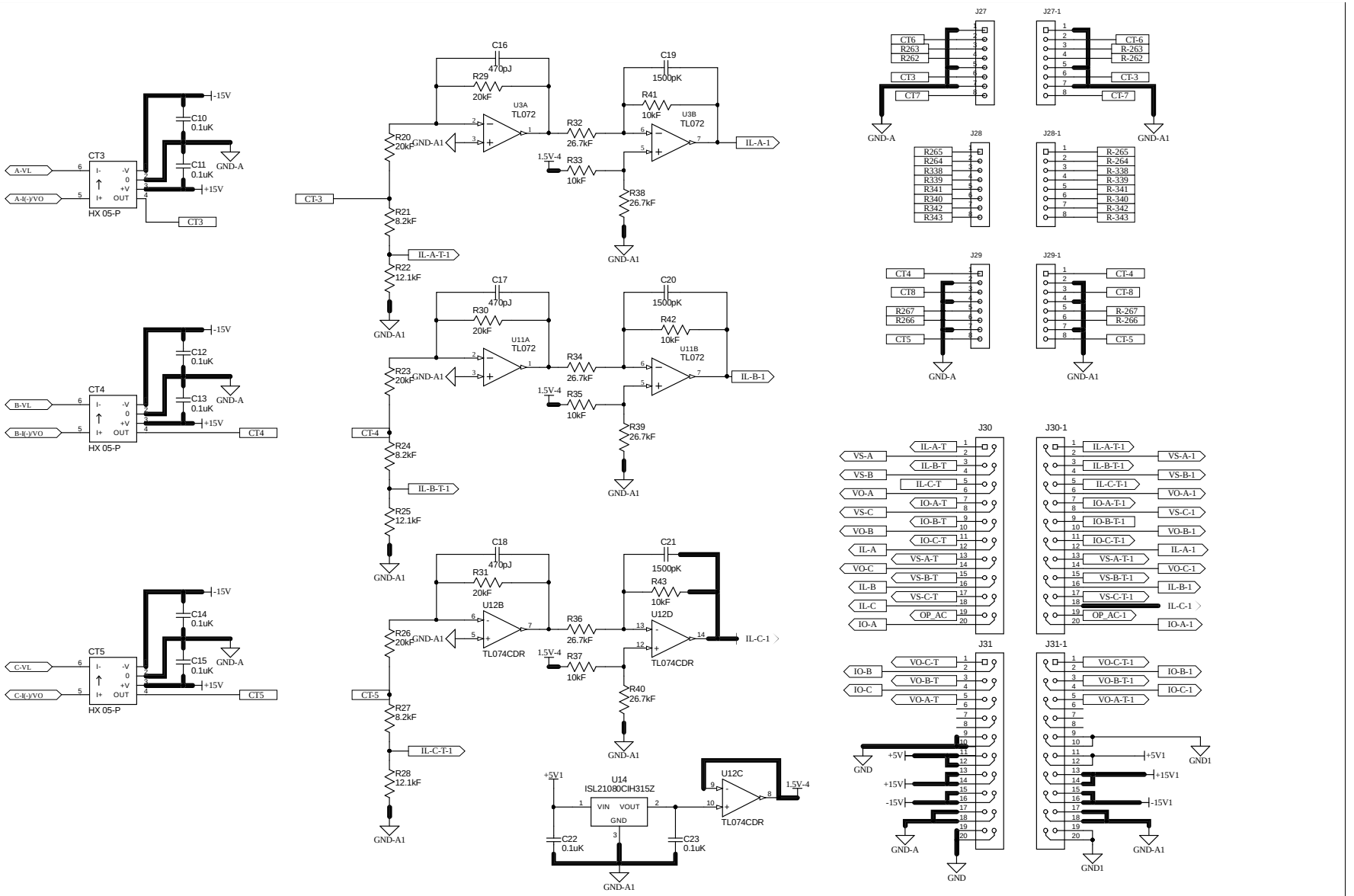


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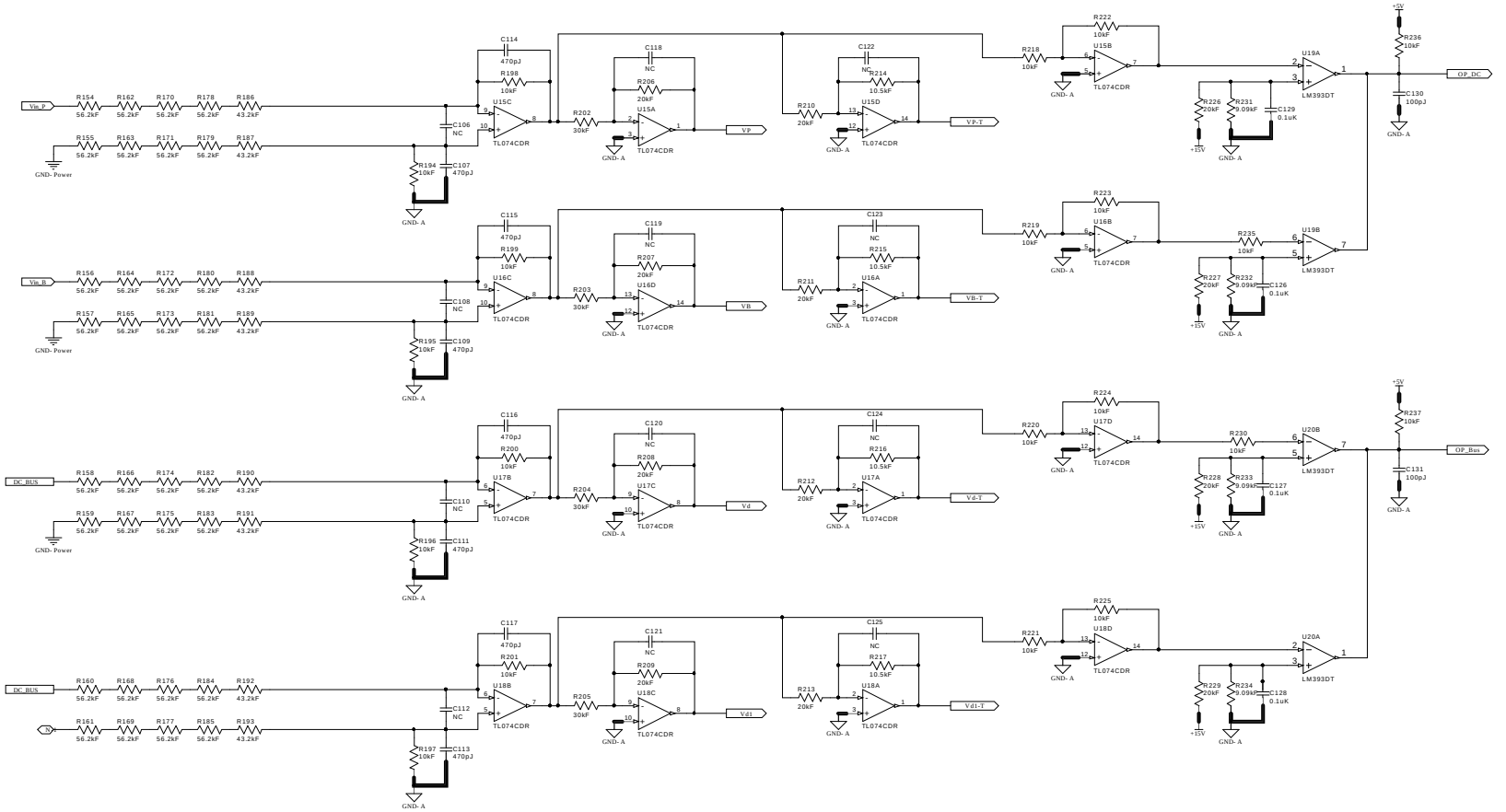


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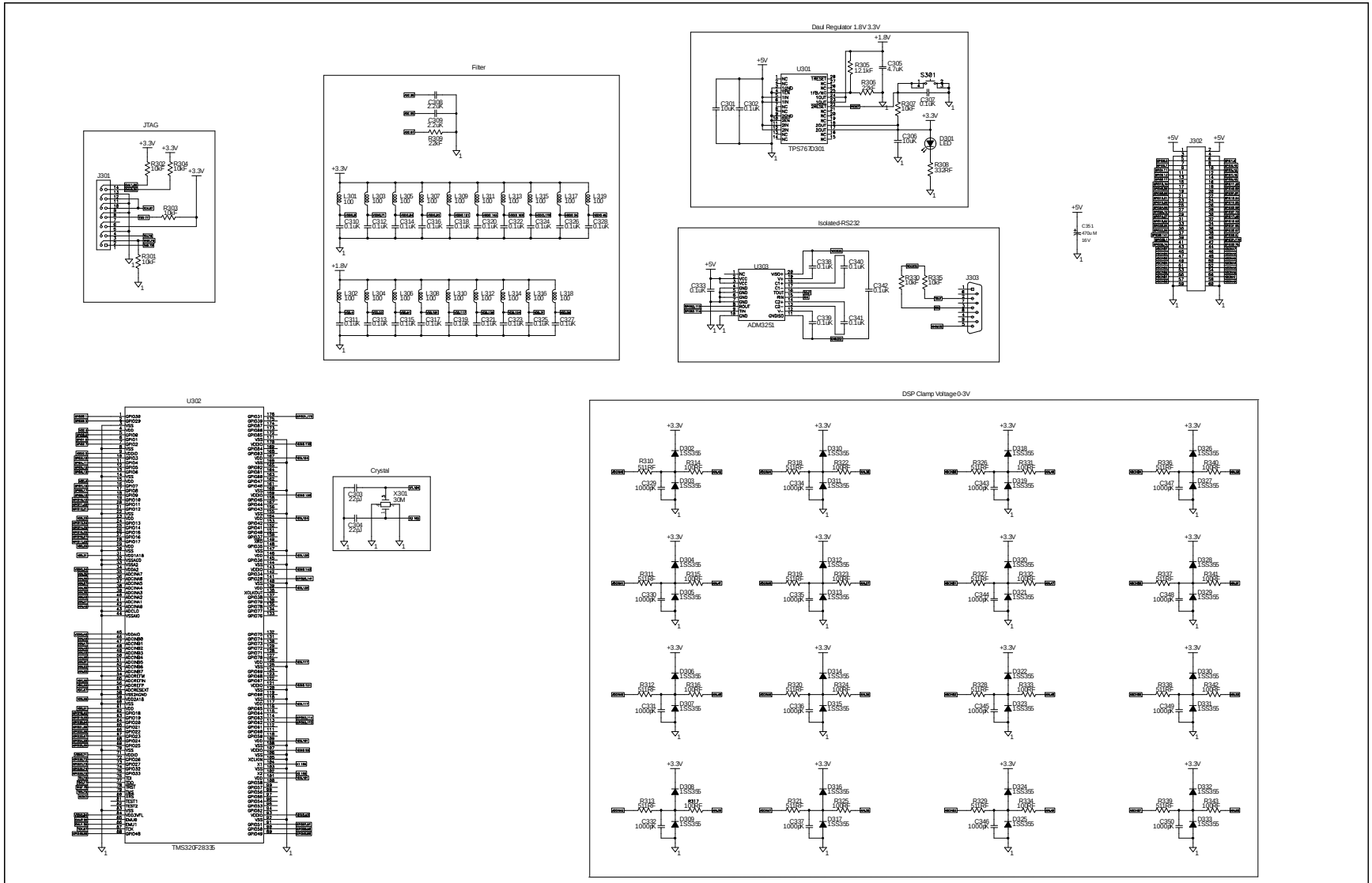
# F28335 Delfino control CARD

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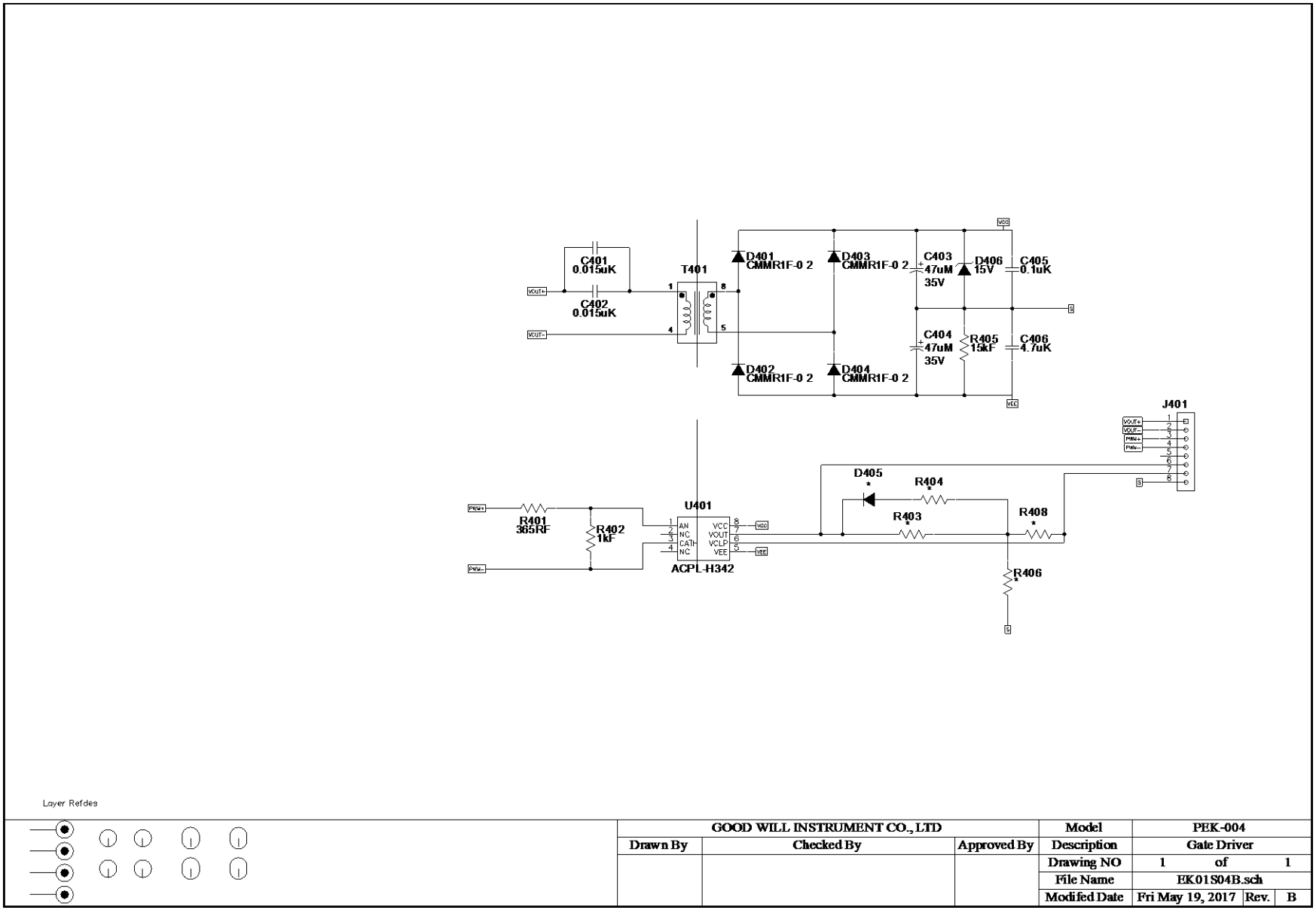
| | | | File Name | EK01S03B.sch | |
| | | | Modifed Date | Tue May 23, 2017 | Rev. B |

# Gate Driver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C402
0.015uK
T401
D401
CMMR1F-0 2
D402
CMMR1F-0 2
D403
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D404
CMMR1F-0 2
C403
47uM
35V
C404
47uM
35V
D406
15V
C405
0.1uK
R405
15kF
C406
4.7uK
J401
D405
R404
R403
R408
R406
R401
365RF
R402
1kF
U401
ACPL-H342
Layer Refdes
GOOD WILL INSTRUMENT CO., LTD
Drawn By
Checked By
Approved By
Model
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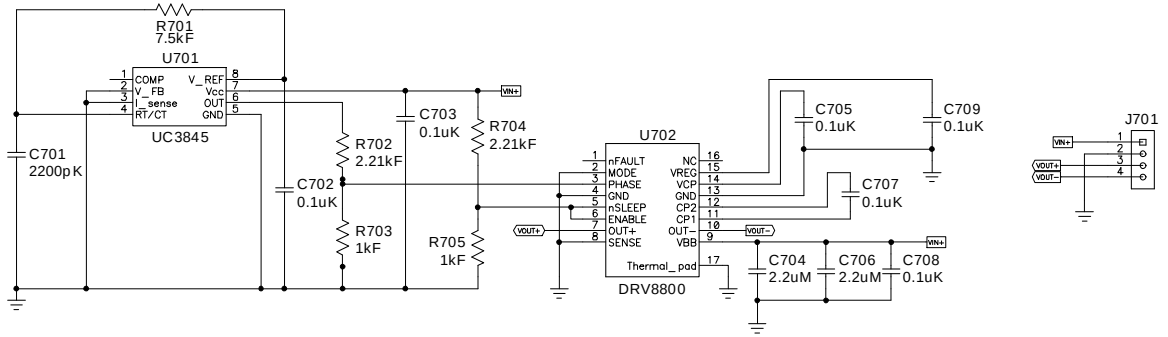
Drawing NO
1 of 1
File Name
EK01S04B.sch
Modifed Date
Fri May 19, 2017
Rev.
B

# Gate Driver Power




Layer Refdes

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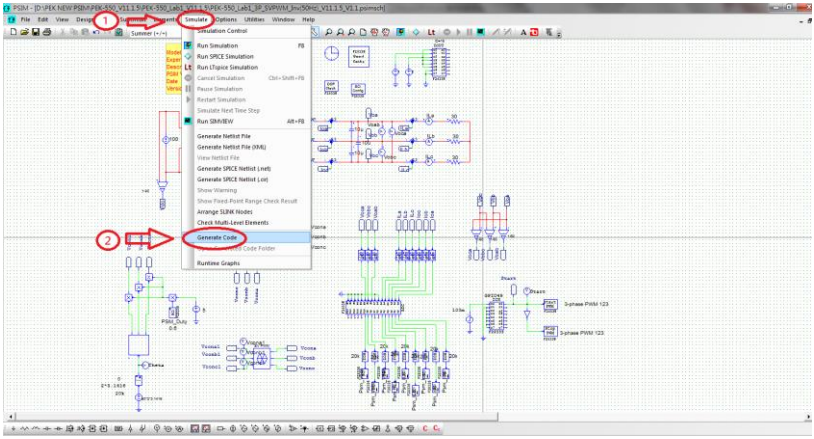
| | | | Drawing NO | 1 of 1 | |
| | | | File Name | EK01S07A.sch | |
| | | | Modifed Date | Mon Mar 09, 2015 | Rev. A |

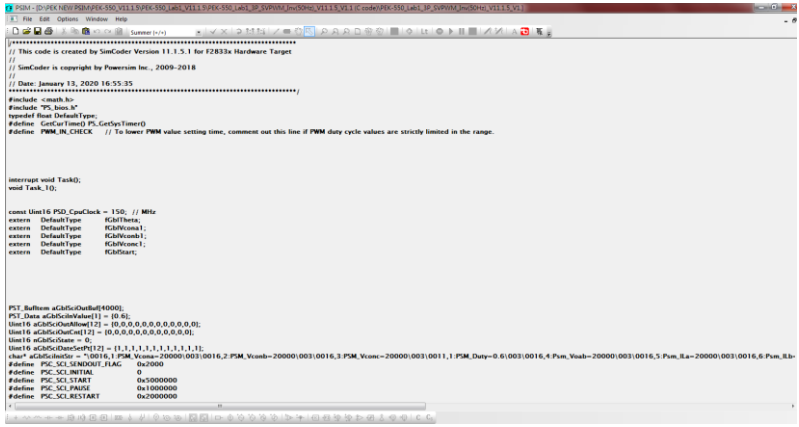
# Appendix B – C Code Burning Procedure

This appendix takes “PEK-550_Lab1_3P_SVPWM_Inv(50Hz)_V11.1.5_V1.1” as an example for the instruction. See the detailed steps below.

Operating steps

1. Open the digital circuit file “PEK-550_Lab1_3P_SVPWM_Inv(50Hz)_V11.1.5_V1.1” within the PSIM program followed by clicking “Generate Code” from “Simulate” tab. The PSIM will generate C Code automatically as shown below.

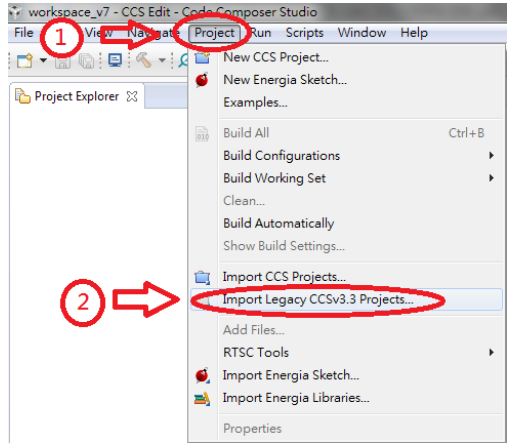




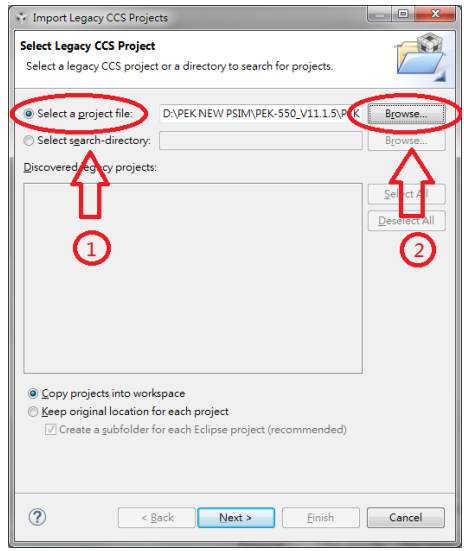
2. A folder of identical name with the PSIM circuit file in which the required files for burning and C Code are well saved will be generated in the location of PSIM circuit file by system.

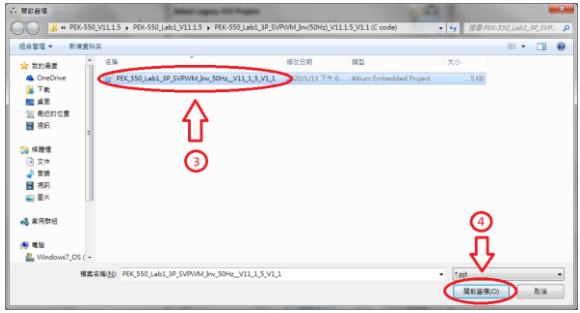


3. Open CCS and select “Project” tab followed by clicking ”Import Legacy CCSv3.3 Projects” as the figure below.

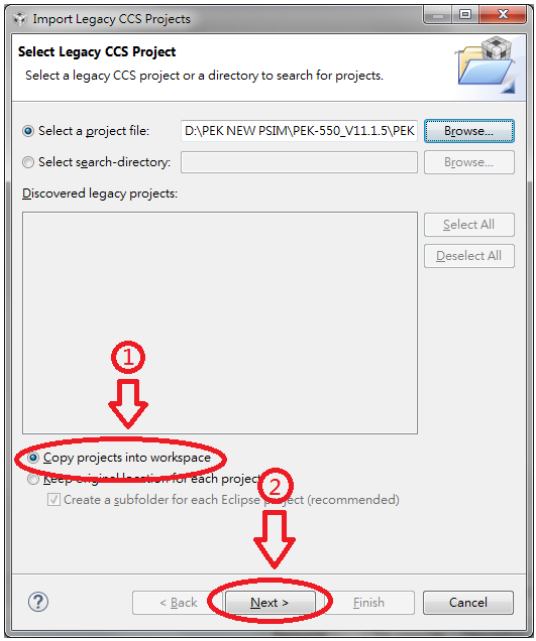


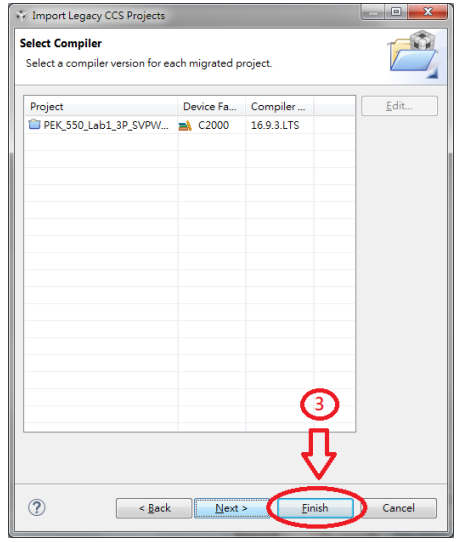

4. Go to "Select a project file" and click "Browser" followed by searching the folder where C Code is located and selecting the file with name extension ".pjt" as the following figure shown.

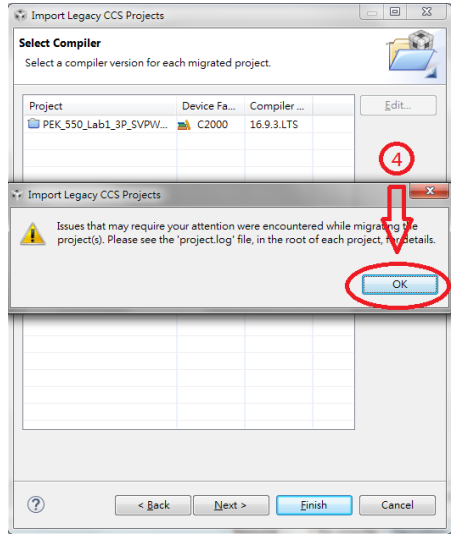





5. Select " Copy projects into workspace " followed by clicking "Next" and then "Finish" to import C Code into CCS program. See the figure below.




Import Legacy CCS Projects
Select Compiler
Select a compiler version for each migrated project.
Project
Device Fa...
Compiler ...
PEK_550_Lab1_3P_SVPW...
C2000
16.9.3.LTS
Edit...
3
< Back
Next >
Finish
Cancel


Import Legacy CCS Projects
Select Compiler
Select a compiler version for each migrated project.
Project
Device Fa...
Compiler ...
PEK_550_Lab1_3P_SVPW...
C2000
16.9.3.LTS
Edit...
4
Import Legacy CCS Projects
Issues that may require your attention were encountered while migrating the project(s). Please see the 'project.log' file, in the root of each project, for details.
OK
< Back
Next >
Finish
Cancel

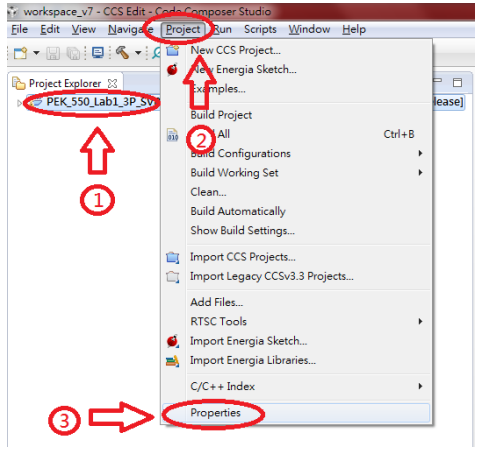
6. Select C Code file and choose "Properties" from "Project" tab. The setting steps are as follows.

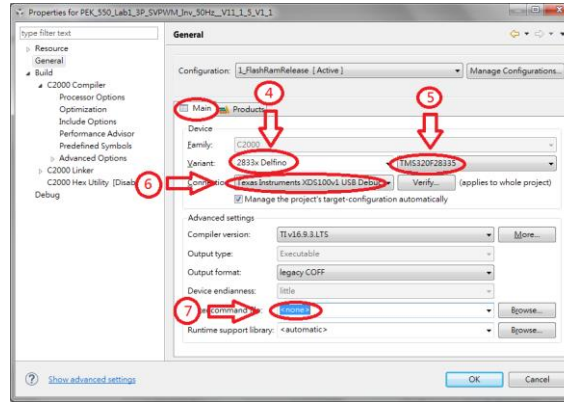
   1) Select "TMS320F28335" of "2833X Delfino" from Variant under Main tab.

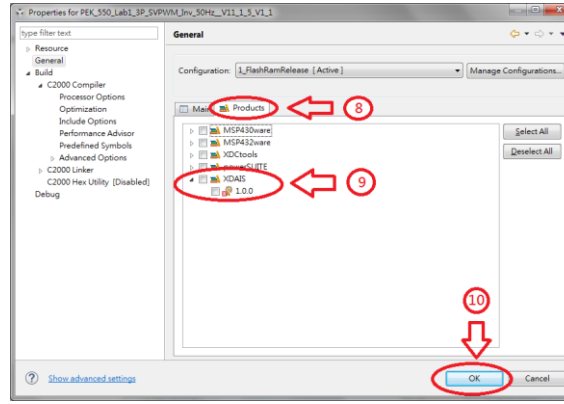
   2) Select "Texas Instruments XDS100v1 USB Debug Probe" from Connection under Main tab.

   3) Select "none" from Linker command file under Main tab.

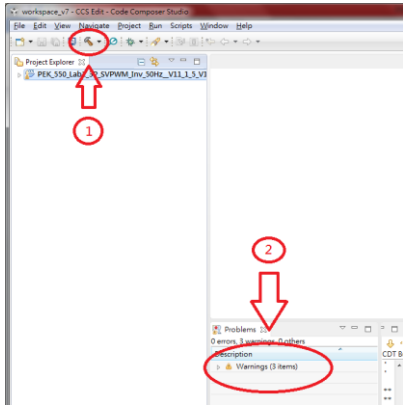
   4) Deselect "XDAIS" under Project tab. (Ignore this step if your CCS version doesn't provide this option.



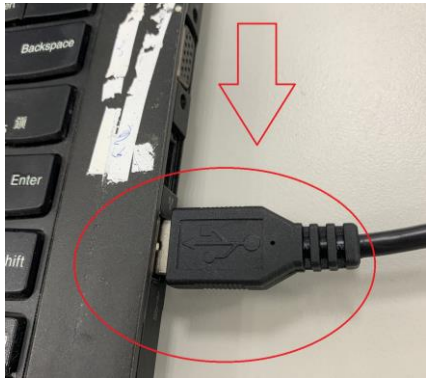


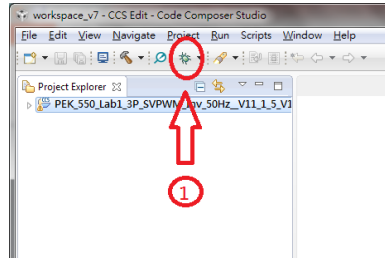




7. After the setting, click "Build" for compilation. If no errors occur after compiling, the program is eligible for burning. Simply ignore the warnings, which have no impact on burning process.

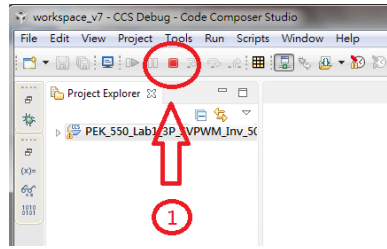



8. Connect PEK-006 to PC and PEK module respectively followed by clicking "Debug" to proceed to burning process.

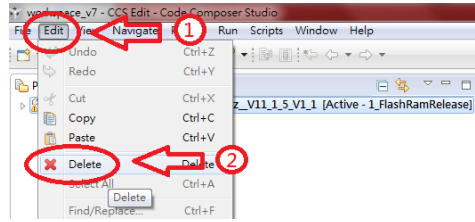



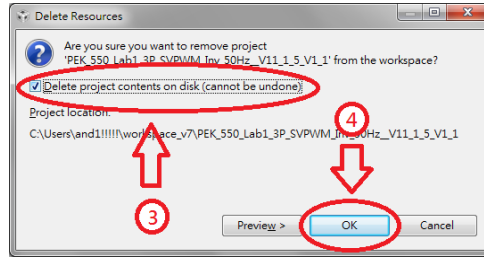



9. After the burning process, click "Terminate" and remove "PEK-006" to finish the entire procedure.




10. If it needs to delete file, select C Code file followed by selecting "Delete" under "Edit" tab and checking "Delete project contents on disk". Finally, click "OK" to complete the action.



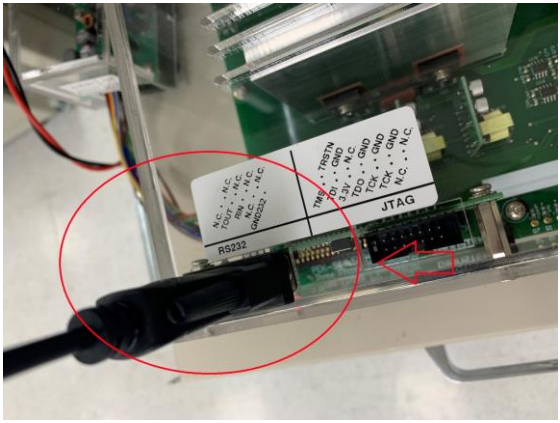



# Appendix C – RS232 Connection

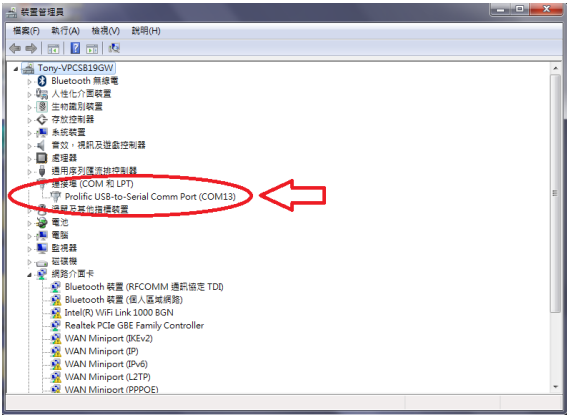
Operating steps

1. Connect PEK-005A to PEK module and make sure DSP is working normally.

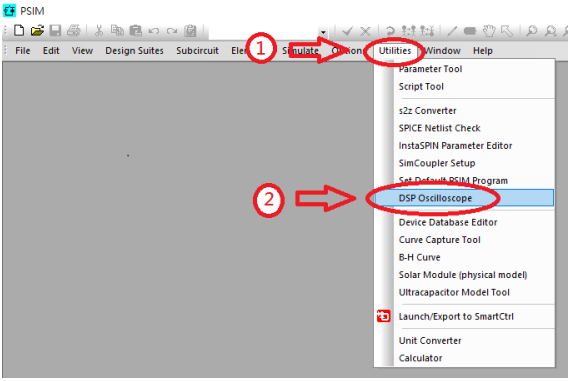

2. Connect one end of RS232 cable to PC, and the other end to the RS232 connector of PEK module.




3. Open Device Manger from PC and identify the COM port number being utilized by RS232 cable.




4. Open PSIM program and select "DSP Oscilloscope" under "Utilities" tab.

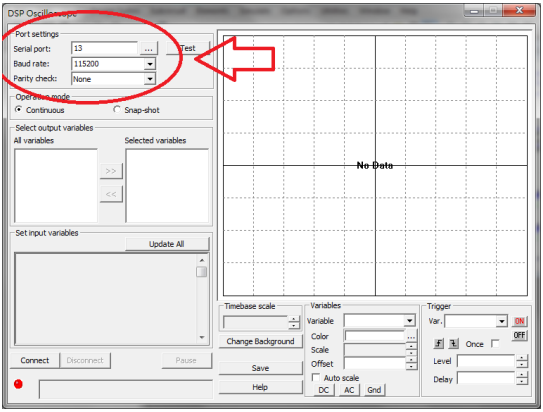



5. The Port settings are as follows.

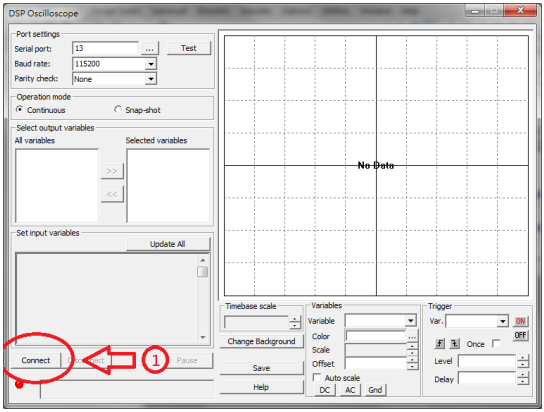
   1) Select the COM port being used by RS232.

   2) Set 115200 for Baud rate.

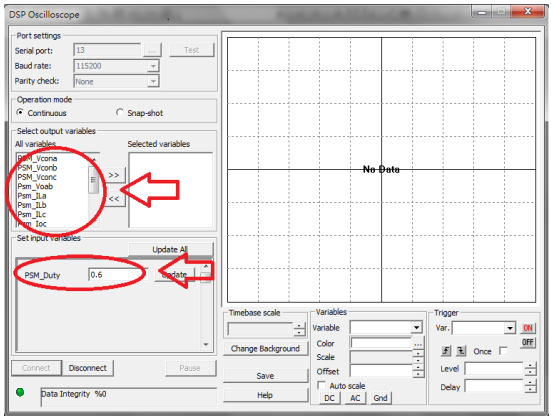
   3) Set None for Parity check.




6. After the settings, click "Connect" to proceed to RS232 connection.




7. Both the output and input variables schemed within PSIM circuit can be clearly observed when connection is properly established.



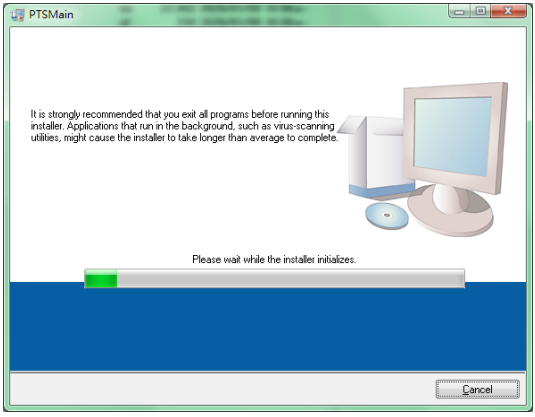
# Appendix D – SAS Operation Procedure

We thoroughly introduce the PTS software covering SAS signal tracking, BAT simulation and real-time signal measurement subsystem. Through the system auto-detection function, each device can be well applied to the corresponding functions.

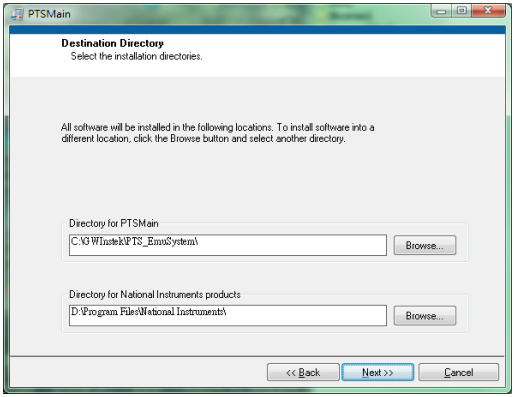
## Installation and Startup

Operating steps

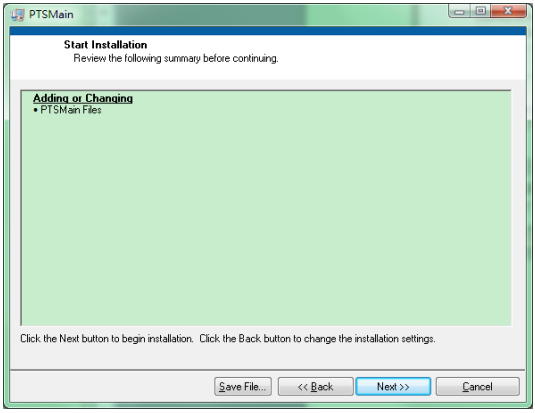
1. Install the complete PTS software: download the PTS5 installer and decompress it to the location c:\PTS installer followed by entering the Volume and executing the Setup.exe as follows.



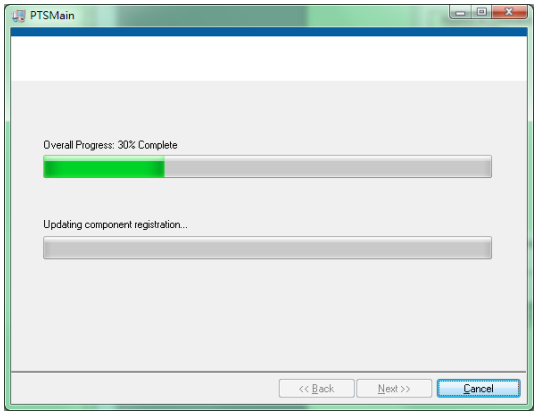
2. The system will search if the required component has been installed. If the required component is not installed yet or the installed one is with old version, the required component will be in the waiting list for installation. In contrast, if the installed one is with higher version than the required one, the installation process will be skipped.



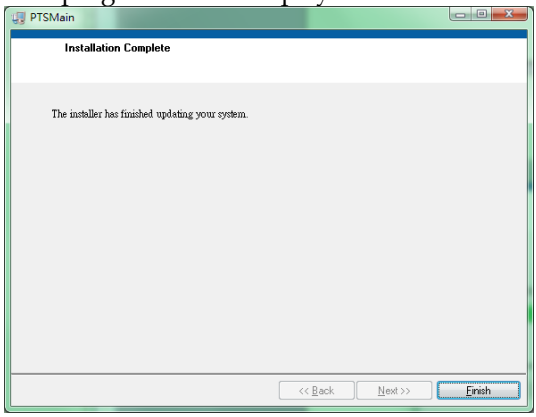

Use the default location and press the "Next" to finish installation. Then, the installed software and the software waiting to be installed including the required executing component will be listed.



3. Press "Next" to proceed to the following installation.

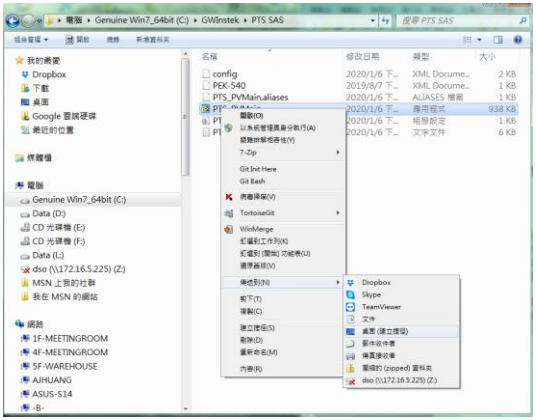



The overall installation progress along with each item progress will be displayed.




4. Download the PTS SAS package software and decompress it to the previous location for installation. A new directory will be added under the location c:\gwinstek\.

5. Switch to the directory and it is available to create a shortcut on the desktop for convenient execution. See the following screenshot shown.




Right click on the PTS_PVMain file followed by selecting "Sent to" -> "Desktop (create shortcut)" to create a shortcut, which allows you to promptly execute the software from the desktop directly with ease.

6. Locate the shortcut from desktop and execute it promptly when necessary later.

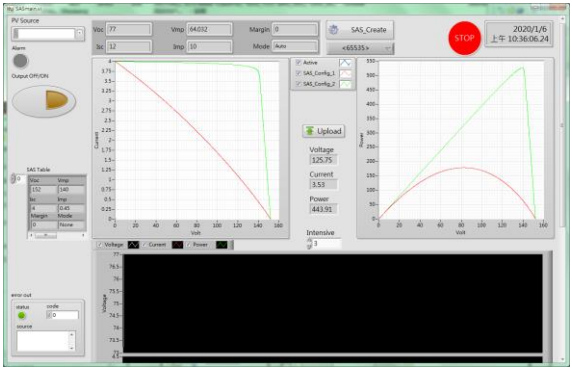
Uninstall

7. In the Control Panel, click the "Programs and Features" item followed by locating the PTSMain one for uninstall.

# Interface Introduction

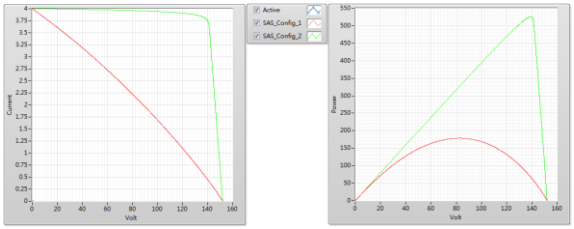
## Program Running Interface

Diagram 1
System Running Interface




The PV trajectory curve of the configured system

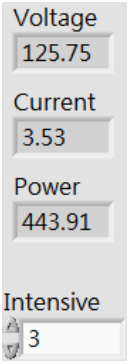
Diagram 2



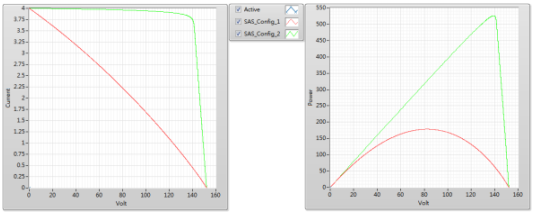

V1 display in left and PV display in right. Active indicates the one after startup. The real IV measurements, via Intensive setting, allow user to check the relevant trajectories.

## Real-time readings monitor

Diagram 3



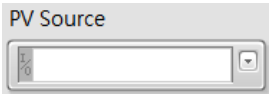

Both Voltage and Current are indicated in the left side of the IV curve chart from the diagram 2, whereas both Voltage and Power are indicated in the right side of the PV curve chart from the figure 2. Intensive indicates the remaining data points on screen, which tracks the real IVP fluctuating trajectory.



# Operation

## Device connection setup

Diagram 4
Device selection



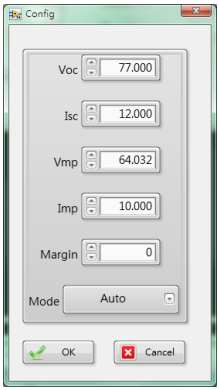

Establish system connection, via the drop-down menu, to designate the applicable device.

## Establish PV reference curve

Diagram 5
Trajectory parameters of previous setup


SAS_Create: Establish a new curve as the following screenshot shown:

Diagram 6
SAS trajectory parameter setting

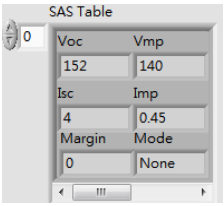



When a new curve is established, the relevant curve will be displayed in the VI and PV charts. And it is available to add parameters for the curve into the SAS table.

- Voc: Open circuit voltage
- Isc: Short circuit current
- Vmp: Max power point voltage
- Imp: Max power point current
- Margin: Output will not be updated within the ample area (%)

- Mode: Select Auto mode when utilizing
- OK: Confirm parameter setting and import into SAS Table
- Cancel: Discard the modification setting

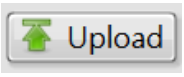
Diagram 7 Trajectory parameter table




- SAS Table: The curve ready to be written into device. Right click to open the operational functions: Import Table, Export Table
- Import Table: Load the previously established curve and parameter in the auto-saving file.
- Export Table: Export the current curve and parameter. Point the cursor to the SAS Table, through the delete button, to delete the current setting (trajectory curve).

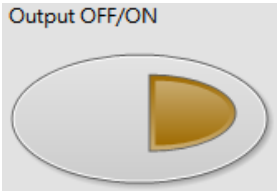
## Upload / Load PV trajectory curve parameter

Diagram 8




Write the set trajectory curve parameter from the SAS Table into the device and wait for execution. In the meantime, PSW enters the SAS running mode.

Diagram 9




Start / Stop PSW output
In the SAS mode, PSW output reacts in accord with the selected curve. In the normal mode, PSW acts as a standard function.

## Select Trajectory Parameter

Diagram 10

Refer to trajectory parameter selection


## Stop and End

Diagram 11

Once the upload action is executed, the device enters the SAS mode and all the Output ON/OFF control determine if PSW proceeds to tracking operation.


If PSW requires to returning back to the normal operation mode, it must select stop software and restart it.

# Appendix Description

## A: PSW Tracking Mode

After SAS software startup, PSW will, by uploading trajectory curve software, initiate tracking mode. User then is able to switch freely among the established trajectory software. In order to exit from the tracking mode, press the "STOP" to make the device return back to the default operation mode.

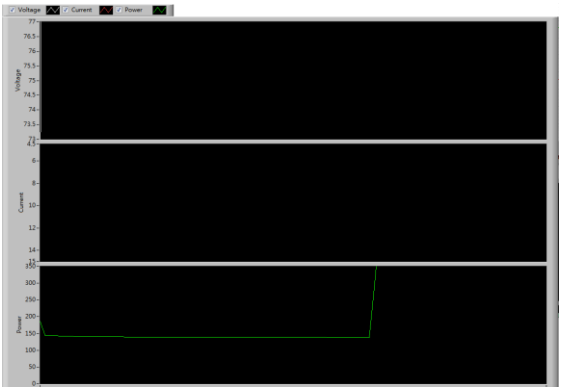
## B: Normal Mode

System is under the normal operation mode after startup. PSW enters the tracking mode after successfully uploading the PV trajectory curve.

## C: IVP Real-Time Record Curve

In the tacking mode, apart from IV and PV trajectories, the both trajectory record charts are also provided, individually.

Diagtam 12



# Appendix E – BATSim Operation Procedure

In the PTS system, BATSim simulates the basic battery mode via the combination of PSW 160-7.2 and PEL-3000, and also simulates the discharge mode via PSW, further simulating charge mode via PEL-3000.

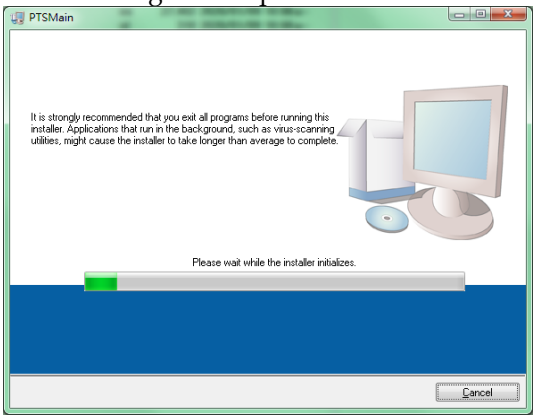
Charge: when external voltage is greater than that of PEL-3000, PEL-3000 absorbs power and thereby simulates the battery charge mode.

Discharge: when external voltage is less than that of PSW, PSW outputs power and thereby simulates the battery discharge mode.

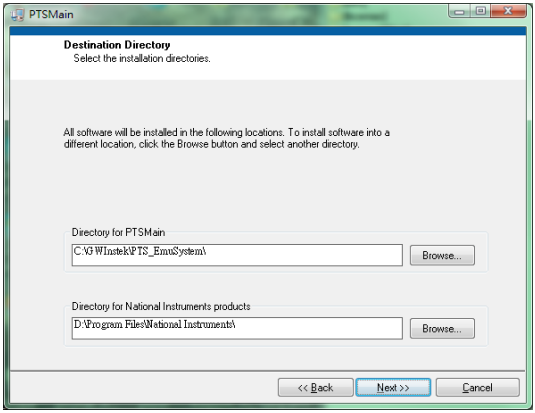
# Installation

Operating steps

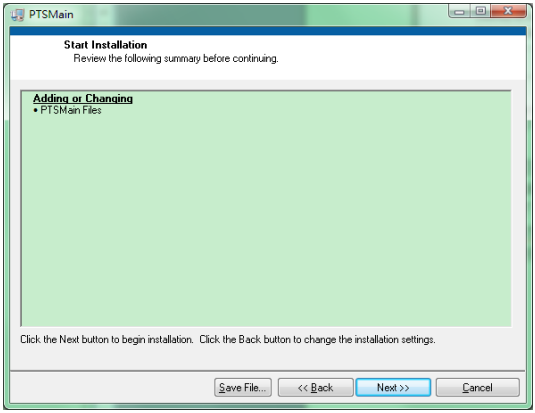
1. Install the complete PTS software: download the PTS5 installer and decompress it to the location c:\PTS installer followed by entering the Volume and executing the Setup.exe as follows.



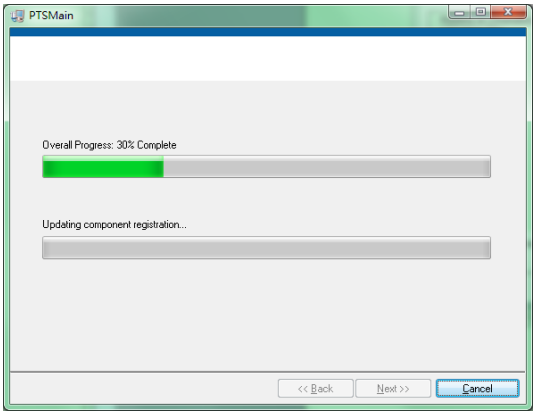

2. The system will search if the required component has been installed. If the required component is not installed yet or the installed one is with old version, the required component will be in the waiting list for installation. In contrast, if the installed one is with higher version than the required one, the installation process will be skipped.



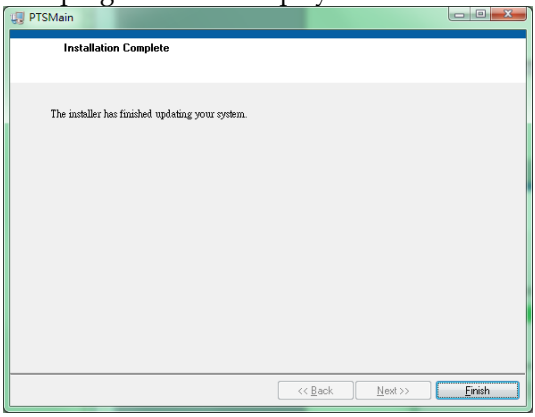

Use the default location and press the "Next" to finish installation. Then, the installed software and the software waiting to be installed including the required executing component will be listed.



3. Press "Next" to proceed to the following installation.




The overall installation progress along with each item progress will be displayed.




4. Download the PTS BATSim package software from the website and decompress it to the previous location for installation. A new directory will be added under the location c:\gwinstek\.

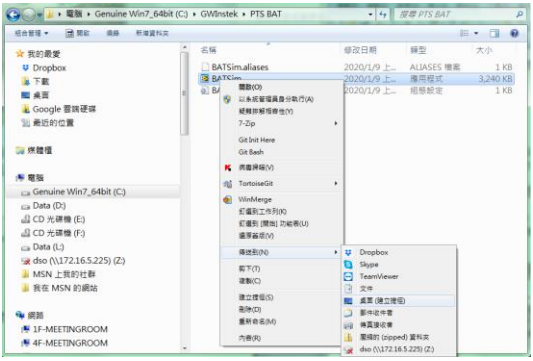
Uninstall

5. In the Control Panel, click the "Programs and Features" item followed by locating the PTSMain one for uninstall.

# Startup

Operating steps

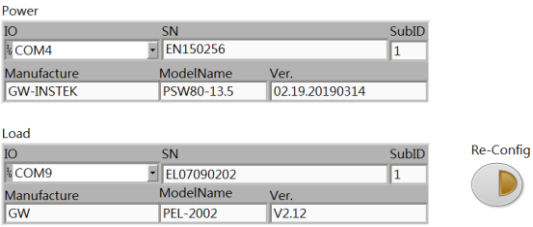
6. Switch to the directory and it is available to create a shortcut on the desktop for convenient execution. See the following screenshot shown.




7. Right click on the BATSim file followed by selecting "Sent to" → "Desktop (create shortcut)" to create a shortcut, which allows you to promptly execute the software from the desktop directly with ease.

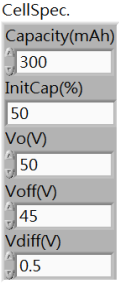
## Interface Introduction

Diagram 1 Device List




User is able to, via the IO setup, manually select the applicable devices for system. Click the "Re-Config" to proceed to setup validation. The basic information of selected devices will be displayed as the above example shown when successful setup. It supports PEL-3000 and PSW series products only.

Diagram 2 Basic parameters settings of simulating battery




- Capacity(mAh): simulating battery capacity
- InitCap(%): initial capacity
- Vo(V): standard output voltage
- Voff(V): simulating battery voltage when empty
- Vdiff(V): simulating voltage difference when internal charge and discharge

Diagram 3 Battery cell indicator

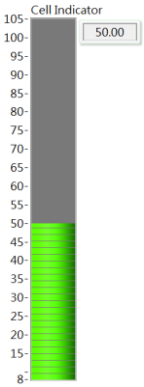



Diagram 4 Battery status display

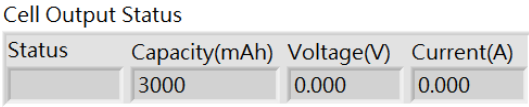
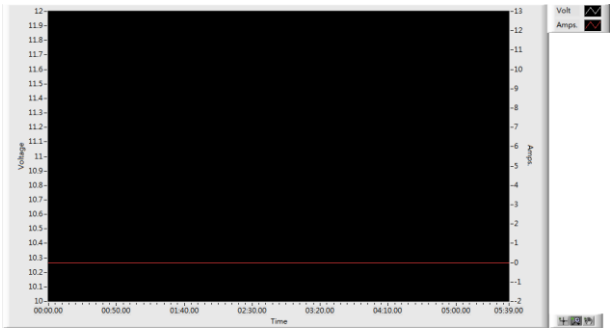


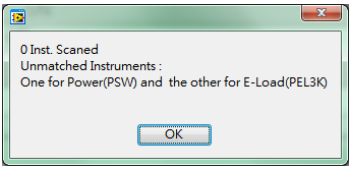

Diagram 5 Battery charge and discharge simulating record curve




During the process of system running, the latest voltage and current readings from device will be loaded and displayed within the above curve chart in accordance with the charge (PEL) and discharge (PSW) behaviors.

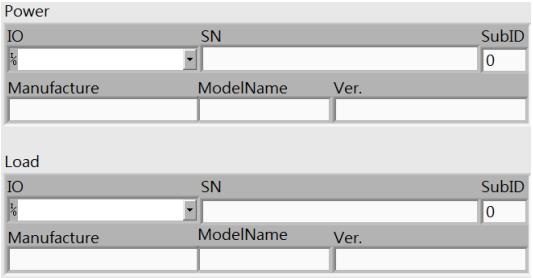
# Operation

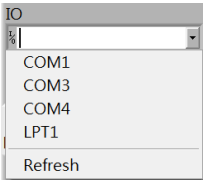
Device validation will start automatically after software startup. The following message will be shown when none of devices have been connected properly.




Select the applicable power and load devices respectively and make the reconnection.

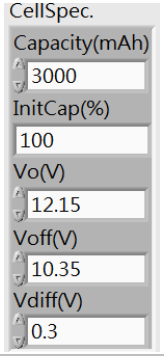
## Device Connection



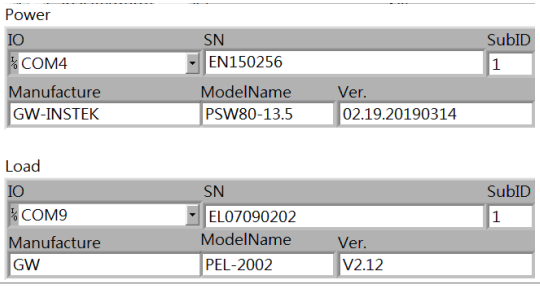

Expand the list of available devices for system and select the applicable resources configuration for power and load individually. Recheck the physical connection when none of connected devices are displayed. Press "Refresh" and see if devices are shown. Contact your local dealer if it doesn't work out still.

## Simulating Parameter Setup



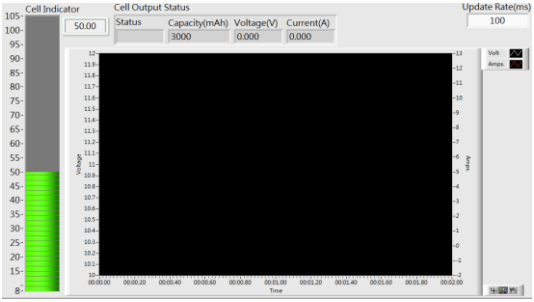

- Capacity(mAh): simulating battery capacity
- InitCap(%): initial capacity
- Vo(V): standard output voltage
- Voff(V): simulating battery voltage when empty
- Vdiff(V): simulating voltage difference when internal charge and discharge


After setup, press "Re-Config" to proceed to validation.




- Power: PSW series devices are required.
- Load: PEL series devices are required.

# Monitor Screen



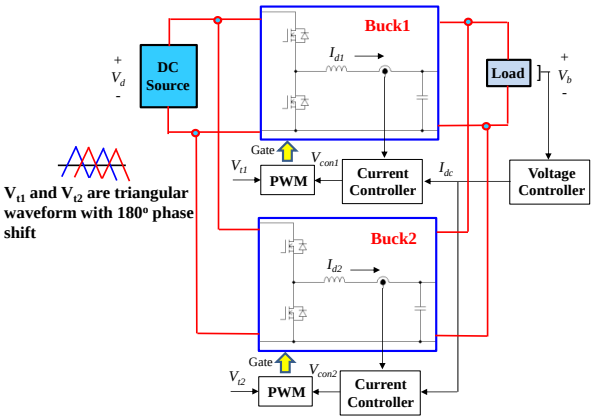
# Appendix F Design Principles

## Experiment 1 Interleaved Buck Converter

The two-phase interleaved buck converter, as shown in Appendix F 1.1, features a current loop and a voltage control loop to maintain the $V_b$ voltage. The voltage loop uses the error from voltage feedback, adjusted by the voltage controller, to obtain the current command ($I_{dc}$) and sends it to the current controllers of the two converters. The two current controllers then use the error from the inductor current feedback, adjusted by the current controller, to obtain the control voltages ($V_{con1}$ and $V_{con2}$) for PWM. The PWM sawtooth waves ($V_{t1}$ and $V_{t2}$) of the two converters are of the same frequency but have a phase difference of 180 degrees to achieve interleaved control. The two PWM trigger signals are interleaved, which also interleaves the ripple of the inductor current, resulting in an output current frequency that is twice the switching frequency, helping to reduce the value of the filter and thus its size. Since the design of the inductor current loop is the same as that of the boost converter, it will be explained in Experiment 2. Here, only the design of the voltage loop is described.

Figure Appendix F 1.1

Two-phase interleaved buck converter




The equivalent circuit of the voltage loop of the current-controlled buck converter is shown in Figure Appendix F1.2(a), from which it can be derived:

$$\frac{V_b}{I_b} = \frac{1+\frac{s}{\omega_z}}{1+\frac{s}{\omega_o}}, \quad \omega_z = \frac{1}{CR_e}, \quad \omega_p = \frac{1}{CR} \qquad \text{(Appendix F1.1)}$$

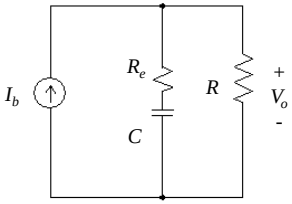
The command of the current loop is generated by the voltage loop. The control block diagram combining the current and voltage loops is shown in Figure Appendix F1.2(b), where it is assumed that the bandwidth of the current loop is much wider than that of the voltage loop, thus the current loop can be considered ideal (i.e., $\widetilde{i_d} = \widetilde{i_{dc}}$), kv is the voltage sensing ratio, LPF2 is a low-pass filter, which combines with the proportional-integral (PI) voltage controller to form a type 2 controller. The Bode plot of the voltage loop is shown in Figure Appendix F1.2(c), and the zero crossover frequency of the voltage loop $u_v$ needs to be much lower than the bandwidth of the current loop, and can be set as $u_v = u_I/4$, $z = u_v/4$, $p = f_s/10$.

According to the current and voltage control loops of the synchronous buck converter, two sets of converters are paralleled and the PWM phases are interleaved by 180 degrees, resulting in the control loop of the two-phase interleaved bidirectional DC-DC converter as shown in Figure Appendix F1.3. Its circuit loop

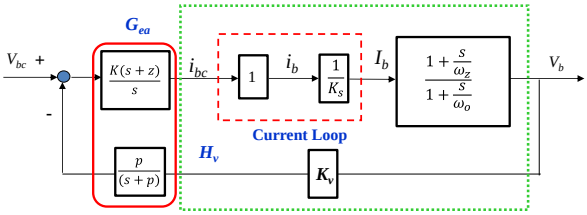
response is the same as the current control loop in Figure Appendix F2.5, while the voltage loop is the same as in Figure Appendix F1.2.

Figure Appendix F1.2

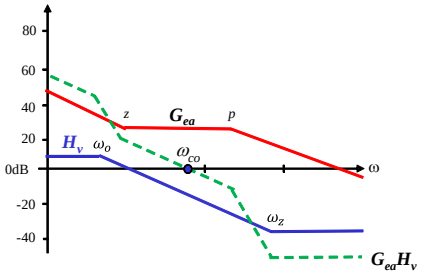
Synchronous buck converter voltage loop design(a) Equivalent circuit




(b) Voltage control loop




(c) Bode Plot



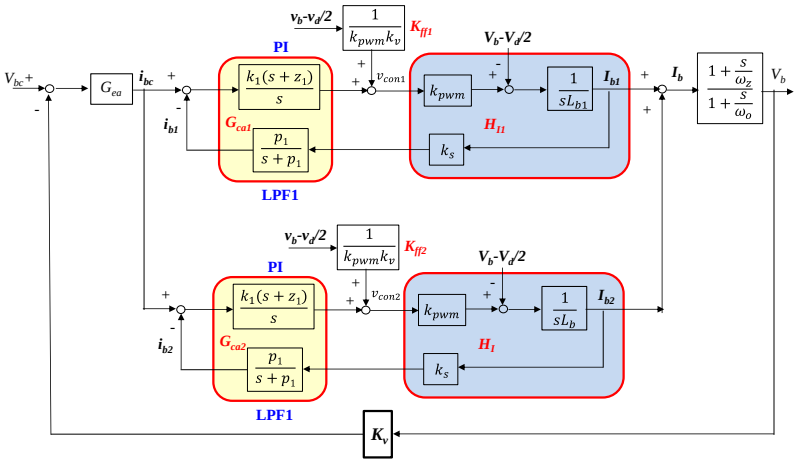



Figure Appendix F1.3 Two-Phase Interleaved Buck Converter Control Architecture

# Experiment 2 Interleaved Boost Converter

The control architecture of the interleaved bidirectional DC-DC converter is illustrated in Appendix F2.1. It comprises a current loop and a voltage control loop, which are employed to maintain the DC bus voltage ($V_d$). The voltage loop utilizes the error from the voltage feedback, which is processed by the voltage controller to generate the current command ($I_{dc}$). This current command is then sent to the current controllers of the two converters. The current controllers, in turn, use the error from the inductor current feedback, processed by the current controller, to generate the control voltages for the PWM ($V_{con1}$ and $V_{con2}$). The PWM sawtooth waves ($V_{t1}$ and $V_{t2}$) of the two converters have the same frequency but are phase-shifted by 180 degrees to achieve interleaved control, as shown in Appendix F2.2. The interleaved PWM trigger signals cause the ripple of the inductor currents to also be interleaved, resulting in an output current frequency that is twice the switching frequency. This helps in reducing the value of the filter, thereby decreasing the filter size.

Figure Appendix F2.1

Control Architecture of Interleaved Bidirectional DC-DC Converter

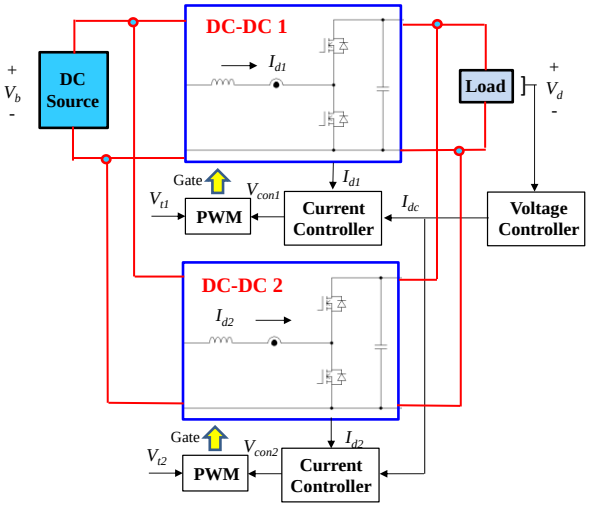
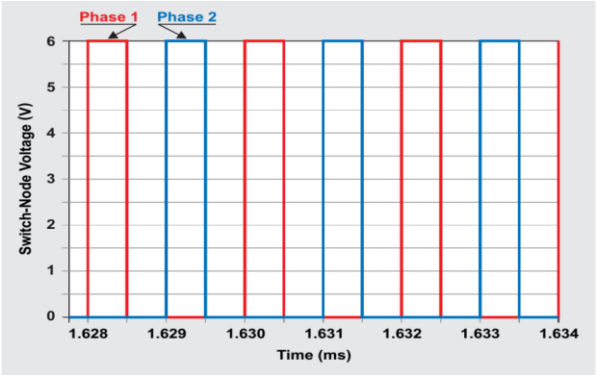


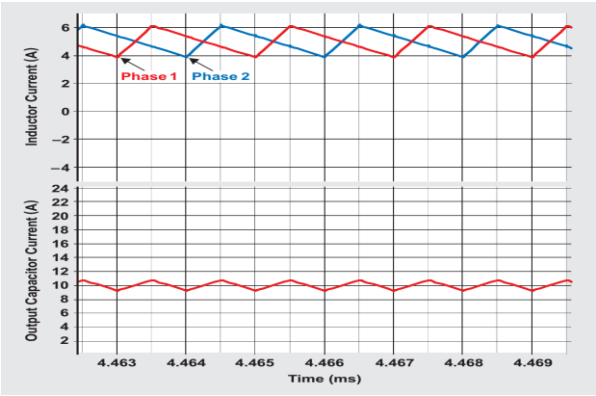
Figure Appendix F2.2

Two-phase interleaved waveform

(a) PWM trigger signal




(b) Inductor Current




The bidirectional DC-DC circuit employs a half-bridge configuration as illustrated in Appendix 2.3. From Figure Appendix F2.3, it can be derived that:

$$L\frac{dI_d}{dt} = dV_d - V_b = \frac{v_{con}}{2v_{tm}}V_d + \frac{V_d}{2} - V_b \quad \text{(Appendix F2.1)}$$

$$d = \frac{1}{2} + \frac{v_{con}}{2V_{tm}} \quad \text{(Appendix F2.2)}$$

$$\frac{dI_d}{dt} = k_{pwm}\, v_{con} + \frac{V_d}{2} - V_b \quad \text{(Appendix F2.3)}$$

$$k_{pwm} = \frac{V_d}{2v_{tm}} \quad \text{(Appendix F2.4)}$$

Using Appendix F2.3, the current loop controller can be designed as shown in Figure Appendix F2.4. The block $H_I$ is plotted based on the small-signal transfer function from Appendix F2.3. The parameter *ks* represents the current sensor's sensing ratio (V/A), and LPF1 is the low-pass filter applied during sensing. The current controller employs Proportional-Integral (PI) control, and the combination of PI and LPF1 forms a type-2 controller. The PI controller generates a feedback control signal $V_{fb}$, which, when combined with the feedforward control signal $V_{ff}$, results in the control voltage vcon for the PWM. The purpose of the feedforward control is to eliminate disturbances. $\frac{V_d}{2} - V_b$ Disturbance to the current loop. The zero-crossing frequency (equivalent to bandwidth) uI of the current loop is designed to be 1/8 to 1/10 of the switching frequency. The Bode plot of the current loop is shown in Appendix F2.5, where $z$ can be set to $u_I/3$ and $p$ to $f_s/4$.

Figure Appendix F2.3

Half-Bridge DC-DC Converter

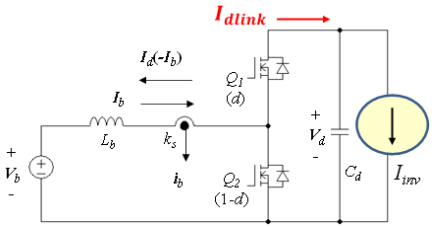



Figure Appendix F2.4

Current Control Loop

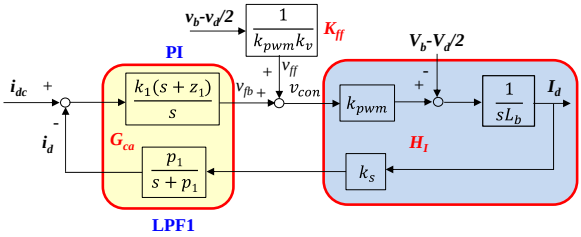


Figure Appendix F2.5

Bode Plot of Current Loop

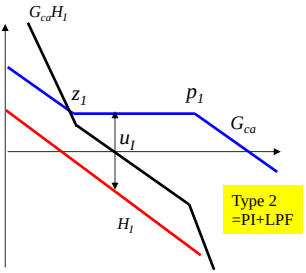



Figure Appendix F2.3, under steady-state conditions, can be derived from the power balance:

$$I_{dlink}\, V_d = -V_b I_d \qquad \text{Appendix F2.5}$$

As shown in Appendix F2.3, when the DC voltage is maintained at a constant value, the output current of the DC-DC converter, $I_{dlink}$, is equal to the equivalent input current of the inverter, $I_{inv}$. By removing the steady-state value of the balanced current, the DC link voltage loop can be represented by the small-signal model in Appendix F2.6(a), from which the following can be derived:

$$\frac{\widetilde{V_d}}{\widetilde{I_{dlink}}} = \frac{1}{sC_d} \qquad \text{(Appendix F2.6)}$$

By utilizing Appendix F 2.5, it can be obtained:

$$\widetilde{I_{dink}} = \frac{-V_b}{V_d}\widetilde{I_d} \qquad \text{(Appendix F2.7)}$$

From (Appendix F 2.6) and (Appendix F 2.7), it can be derived:

$$\frac{\widetilde{V_d}}{\widetilde{I_d}} = \frac{\widetilde{V_d}}{\widetilde{I_{dlink}}}\frac{\widetilde{I_{dlink}}}{\widetilde{I_d}} = (-\frac{V_b}{V_d})\frac{1}{sC_d} \qquad \text{(Appendix F2.8)}$$

The command of the current loop is generated by the voltage loop. The control block diagram combining the current and voltage loops is shown in Figure Appendix F2.6(b), where it is assumed that the bandwidth of the current loop is significantly wider than that of the voltage loop, thus the current loop can be considered ideal (i.e., $\widetilde{i_d} = \widetilde{i_{dc}}$ ), kv is the voltage sensing ratio, LPF2 is a low-pass filter, which combines with the proportional-integral (PI) voltage controller to form a type 2 controller. The Bode plot of the voltage loop is shown in Figure Appendix F2.6(c). Considering the low-

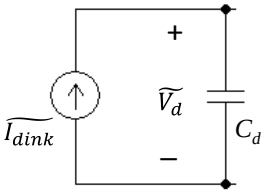
frequency ripple of $I_{inv}$ under unbalanced three-phase load in the inverter, the zero-crossing frequency uv of the voltage loop needs to be much lower than the second harmonic to reduce the ripple of the inductor current command idc, where $z$ can be set as $u_v/4$, $p$ as $f_s/10$.

Based on the aforementioned current and voltage control loops of the half-bridge DC-DC converter, two sets of converters are paralleled and the PWM phase is interleaved by 180 degrees to obtain the control loop of the two-phase interleaved bidirectional DC-DC converter as shown in Figure Appendix F 2.7. The response of its circuit loop is the same as the control loop in Figure Appendix F 2.4, and the voltage loop is the same as in Figure Appendix F 2.6.

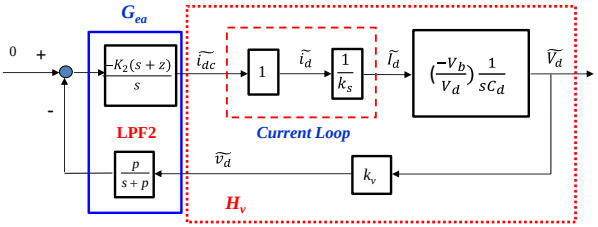
Figure Appendix F2.6

Small-signal model of the voltage loop of the two-phase DC-DC converter

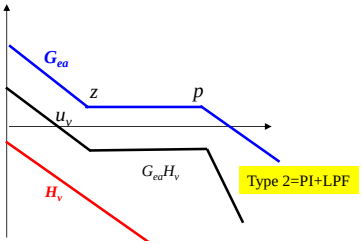
(a) Equivalent circuit




(b) Voltage control loop




(c) Bode Plot



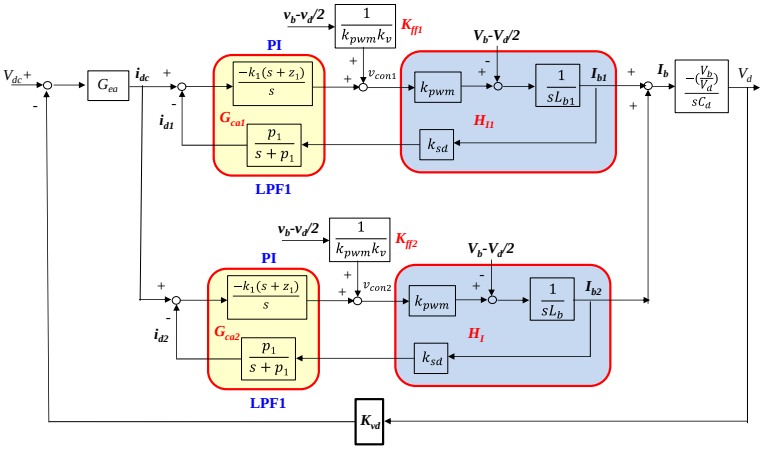


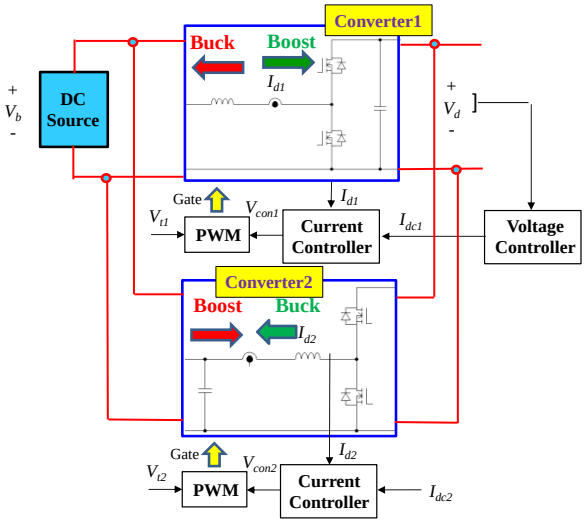

Figure Appendix F2.7 Control loop of the two-phase interleaved bidirectional DC-DC converter

# Experiment 3 Bidirectional DC-DC Converter

Combining the synchronous buck converter from Lab1 and the synchronous boost converter from Lab2, as shown in the circuit of Figure Appendix F3.1, one operates in buck mode, and the other in boost mode. Their inputs and outputs are connected together, with the low-voltage side ($V_b$) connected to the power supply. This setup can verify that both converters have bidirectional power adjustment capability, and energy can be recovered, with one acting as the load for the other, without the need for an additional load. Converter 1 has both voltage and current loops, with the voltage $V_d$ maintained by Converter 1, while Converter 2 only has a current loop, with the current command set by $I_{dc2}$, which can be positive or negative. When $I_{dc2}$ is positive, Converter 2 acts as the load for Converter 1, with Converter 1 operating in boost mode and Converter 2 in buck mode. When Idc2 is negative, Converter 1 acts as the load for Converter 2, with Converter 1 operating in buck mode and Converter 2 in boost mode.

Figure Appendix F3.1

Bidirectional DC-DC converter



# Experiment 4 Three-Phase Four-Wire Boost Standalone Inverter

The boost circuit was introduced in Experiment 2, and the following will explain the standalone inverter.

The control architecture of the three-phase four-wire inverter is shown in Figure Appendix F4.1. From Figure Appendix F4.1, it can be derived:

$$L\frac{dI_{oa}}{dt} = V_{An} - V_{an} \quad \text{(Appendix F4.1)}$$

$$L\frac{dI_{ob}}{dt} = V_{Bn} - V_{bn} \quad \text{(Appendix F4.2)}$$

$$\frac{dI_{oc}}{dt} = V_{Cn} - V_{cn} \quad \text{(Appendix F4.3)}$$

$$I_{oA} + I_{oB} + I_{oC} = I_{oN} \quad \text{(Appendix F4.4)}$$

The voltage of the ABC three arms using SPWM switching can be expressed as: utilizing

$$V_{in} = \frac{v_{coni}}{2v_{tm}} V_d,\ i = A, B, C \quad \text{(Appendix F4.5)}$$

Utilizing (Appendix F 4.1)~(Appendix F 4.5), it can be derived:

$$\begin{bmatrix} L\frac{dI_{oa}}{dt} \\ L\frac{dI_{ob}}{dt} \\ L\frac{dI_{oc}}{dt} \end{bmatrix} = \frac{V_d}{2v_{tm}} \begin{bmatrix} v_{conA} \\ v_{conB} \\ v_{conC} \end{bmatrix} - \begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} \quad \text{(Appendix F4.6)}$$

Definition:

$$k_{pwm} = \frac{V_d}{2v_{tm}} \quad \text{(Appendix F4.7)}$$

It can be derived:

$$\begin{bmatrix} L\dfrac{dI_{oa}}{dt} \\ L\dfrac{dI_{ob}}{dt} \\ L\dfrac{dI_{oc}}{dt} \end{bmatrix} = k_{pwm}\begin{bmatrix} v_{conA} \\ v_{conB} \\ v_{conC} \end{bmatrix} - \begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix}$$

(Appendix F4.8)

Utilizing the abc-dq0 axis transformation yields:

$$\begin{bmatrix} L\dfrac{dI_{od}}{dt} \\ L\dfrac{dI_{oq}}{dt} \\ L\dfrac{dI_{o0}}{dt} \end{bmatrix} = k_{pwm}\begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}\begin{bmatrix} V_{cond} \\ V_{conq} \\ V_{con0} \end{bmatrix} - \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}\begin{bmatrix} V_{od} \\ V_{oq} \\ V_{o0} \end{bmatrix} - \begin{bmatrix} 0 & \omega L & 0 \\ -\omega L & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}\begin{bmatrix} I_{od} \\ I_{oq} \\ I_{o0} \end{bmatrix}$$

(Appendix F4.9)

Similarly, the output voltage can also be obtained:

$$\begin{bmatrix} C\dfrac{dV_{od}}{dt} \\ C\dfrac{dV_{oq}}{dt} \\ C\dfrac{dV_{o0}}{dt} \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}\begin{bmatrix} I_{od} \\ I_{oq} \\ I_{o0} \end{bmatrix} - \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}\begin{bmatrix} I_{Ld} \\ I_{Lq} \\ I_{o0} \end{bmatrix} - \begin{bmatrix} 0 & \omega C & 0 \\ -\omega C & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}\begin{bmatrix} V_{od} \\ V_{oq} \\ V_{o0} \end{bmatrix}$$

(Appendix F4.10)

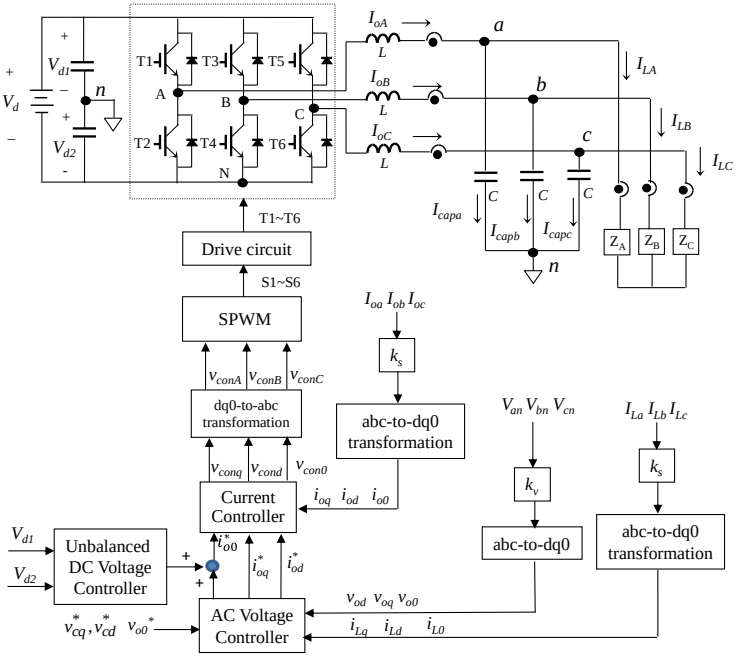


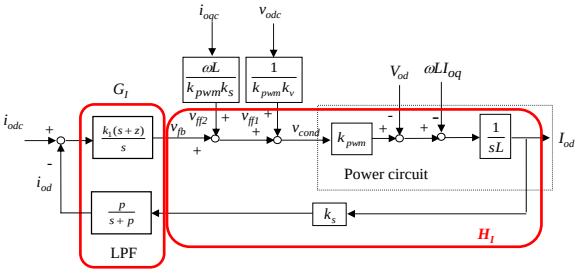

Figure Appendix F4.1 Control Architecture of Three-Phase Four-Wire Standalone Inverter

Utilizing (Appendix F4.9), the current loop of the converter can be designed as shown in Figure Appendix F4.2. The power circuit block is drawn using (Appendix F4.9). The controller employs both feedback control ($v_{fb}$) and feedforward control ($v_{ff1}$ and $v_{ff2}$). The feedforward control is used to directly counteract the disturbances of $V_{od}$, $\omega LI_{oq}$ (d-axis, q-axis, and 0-axis principles are similar) on the current loop. The feedback control consists of a proportional-integral ($G_I$) and low-pass filter (LPF) forming a type II error amplifier. The Bode plot of the control loop is shown in Figure Appendix F4.3(d). The bandwidth of the current loop can be set to 1/10~1/8 of the switching frequency.

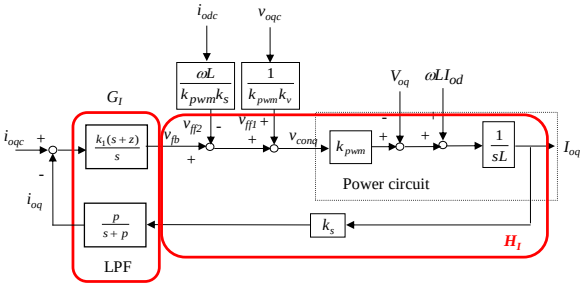
Figure Appendix F4.2

Current Control Loop of Standalone Inverter

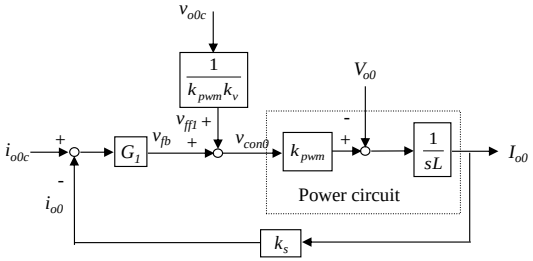
(a) d-axis



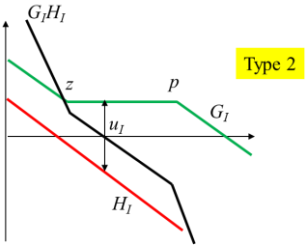

(b) q-axis




(c) 0-axis




(d) Bode Plot

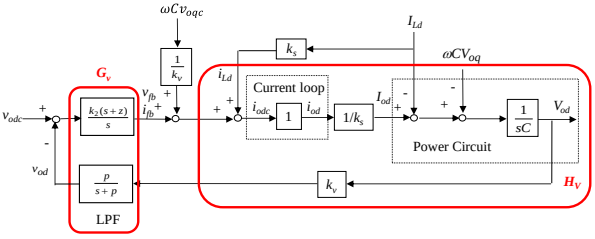



Utilizing (Appendix F4.10), the voltage loop of the converter can be designed as shown in Figure Appendix F4.3. The power circuit block is drawn using (Appendix F4.10), and the current loop is set to be ideal, meaning the current tracking response is set to 1. The

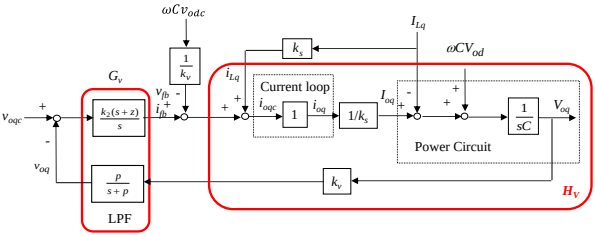
controller employs both feedback control and feedforward control. The feedforward control directly counteracts the disturbances of the load current ($i_{Ld}$, $i_{Lq}$, and $i_{L0}$) on the voltage loop. The feedback control consists of a proportional-integral ($G_v$) and low-pass filter (LPF) forming a type II error amplifier. The Bode plot of the control loop is shown in Figure Appendix F4.3(d). The bandwidth of the voltage loop can be set to 1/4 of the current loop bandwidth. The commands for the d-axis and 0-axis are set to zero. The voltage control of the 0-axis is used to balance the three-phase line voltage, ensuring balance under unbalanced three-phase load conditions.

Figure Appendix F4.2

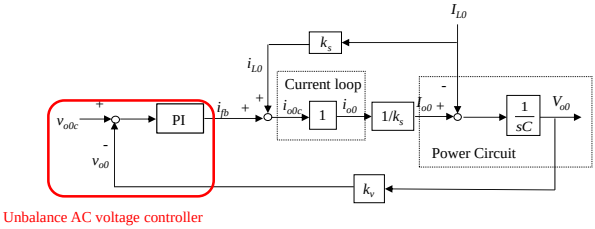
Voltage Control Loop of Standalone Inverter(a) d-axis




(b) q-axis

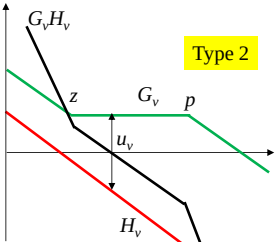



(c) 0-axis




Unbalance AC voltage controller

(d) Bode Plot



# Experiment 5 Three-Phase Four-Wire Photovoltaic Grid-Connected Inverter

Based on the PEK-540 two-stage circuit architecture, a grid-connected three-phase four-wire PV inverter as shown in Figure Appendix F5.1 can be realized. The input of the two sets of DC-DC converters is the photovoltaic module, forming a multi-string PV inverter. The purpose of the DC-DC converter input from the photovoltaic module is to boost the PV module voltage to the DC bus voltage and enable the photovoltaic module to operate at its maximum power point. The second stage inverter then feeds the power into the grid. The control architecture of the DC-DC converter is shown in Figure Appendix F5.2, which is a three-loop control architecture. The outermost loop is the maximum power point tracking control loop (MPPT), which generates the voltage command ($v_{pc}$) for the photovoltaic module. The middle loop is the voltage control loop, which aims to make the photovoltaic module voltage ($v_p$) follow its command. The voltage controller generates a current command ($I_{Lc}$) for the innermost current loop, which aims to make the inductor current ($I_L$) follow this current command. The current loop generates the final PWM control voltage ($v_{conp}$), which is then compared with the PWM triangular wave ($v_t$) to obtain the duty cycle of the switch.

As derived from Appendix F5.2:

$$L\frac{dI_L}{dt} = dV_d - V_{pv} \qquad \text{(Appendix F5.1)}$$

The duty cycle can be expressed as:

$$d = \frac{1}{2} + \frac{v_{conp}}{2V_{tm}} \qquad \text{(Appendix F5.2)}$$

The amplitude of the triangular wave is denoted as vtm. By substituting (Appendix F 5.2) into (Appendix F 5.1), the following can be obtained:

$$L\frac{dI_L}{dt} = k_{pwm}\, v_{conp} + \frac{V_d}{2} - V_{pv} \qquad \text{(Appendix F5.3)}$$

Among $k_{pwm} = \frac{V_d}{2v_{tm}}$ (Appendix F5.4)

Appendix Figure F5.1

Photovoltaic Grid-Connected Three-Phase Four-Wire Inverter

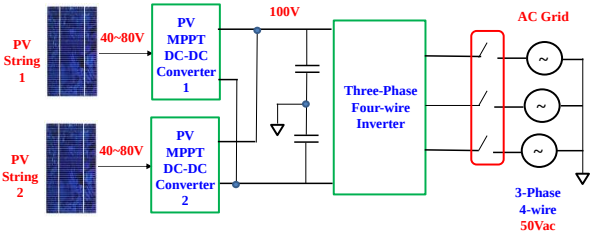
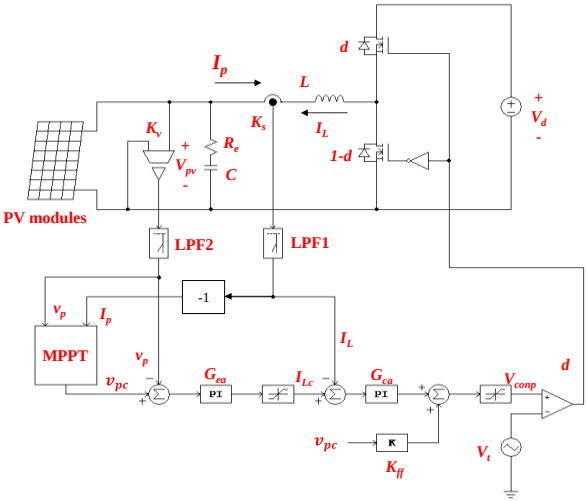



Figure Appendix F5.2

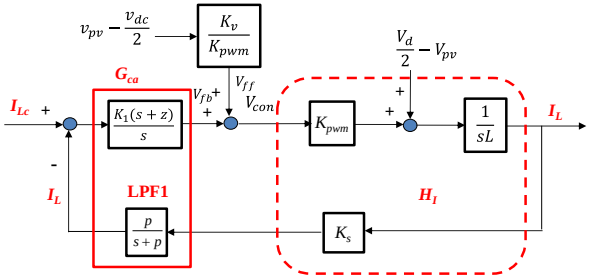
MPPT Control Architecture of Photovoltaic Module DC-DC Converter



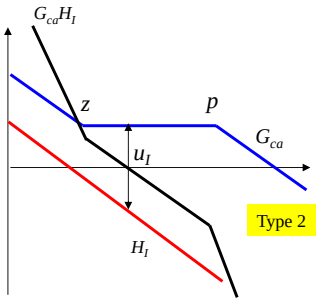

The current loop controller can be designed using Appendix F 5.3, as illustrated in Figure Appendix F 5.3(a). The block $H_I$ is plotted based on the small-signal transfer function from Appendix F 5.4. The parameter ks represents the current sensor's sensing ratio (V/A), and LPF1 is the low-pass filter applied during sensing. The current controller employs Proportional-Integral (PI) control, and the combination of PI and LPF1 forms a type-2 controller. The PI controller generates a feedback control signal $V_{fb}$, which, when added to the feedforward control signal $V_{ff}$, results in the control voltage $v_{con}$ for the PWM. The purpose of the feedforward control is to eliminate. $\frac{V_d}{2} - V_{pv}$ Disturbance to the current loop. The zero-

crossing frequency (equivalent to bandwidth) $u_I$ of the current loop is designed to be 1/8 to 1/10 of the switching frequency. The Bode plot of the current loop is shown in Appendix F 5.3(b), where $z$ can be set to $u_I/3$ and p to $f_s/4$.

Figure Appendix F5.3 Design of the Current Loop for PV DC-DC Converter(a) Control Block Diagram




(b) Bode Plot




The PV module can be regarded as a voltage source, and the voltage loop can be represented by the small-signal model shown in Appendix F 5.4(a), from which it can be derived:

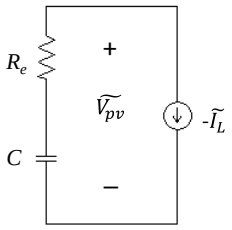
$$\frac{\widetilde{V_{pv}}}{\widetilde{I_L}} = \frac{-(1+\frac{s}{\omega_z})}{sC}, \quad \omega_z = \frac{1}{R_e C} \qquad \text{(Appendix F5.5)}$$

The command of the current loop is generated by the voltage loop. The combined control block diagram of the current and voltage loops is shown in Appendix F Figure 5.4(b). It is assumed that the bandwidth of the current loop is significantly wider than that of the voltage loop, thus the current loop can be considered ideal (i.e.$\widetilde{i_L} = \widetilde{i_{Lc}}$)$Kv$ represents the voltage sensing ratio, and LPF2 is a low-pass filter, which, combined with the proportional-integral (PI) voltage controller, forms a type 2 controller. The Bode plot of the voltage loop is shown in Appendix F 5.4(c). The zero-crossing frequency of the voltage loop, uv, must be significantly lower than

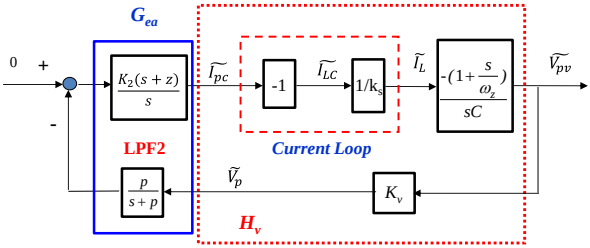
the bandwidth of the current loop and can be set to $u_v=u_I/4$, $z = u_v/4$, $p = f_s/10$.

Figure Appendix F5.4

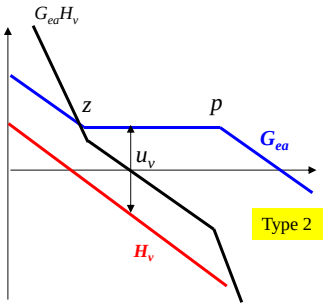
Design of Voltage Loop for PV DC-DC Converter(a) Small-Signal Equivalent Circuit




(b) Control Block Diagram




(c) Bode Plot



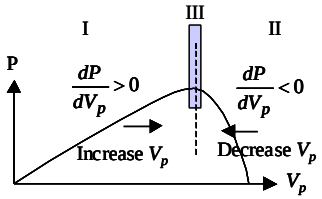

Maximum Power Point Tracking (MPPT) control generally employs the Perturbation and Observation (P&O) method. The concept, as illustrated in Appendix Figure F5.5(a), involves moving the operating point on the $P$-$V_p$ characteristic curve. The slope $dP/dV_p$ calculated from the current sample determines whether the operating region is in Interval I or Interval II. If in Interval I, the next movement direction is to increase $V_p$; conversely, if in Interval II, the next movement direction is to decrease $V_p$. Each time, the operating point must be moved and reassessed, hence the name Perturbation and Observation method. The P&O method must be

executed through a program, with its flowchart shown in Appendix Figure F5.5(b).

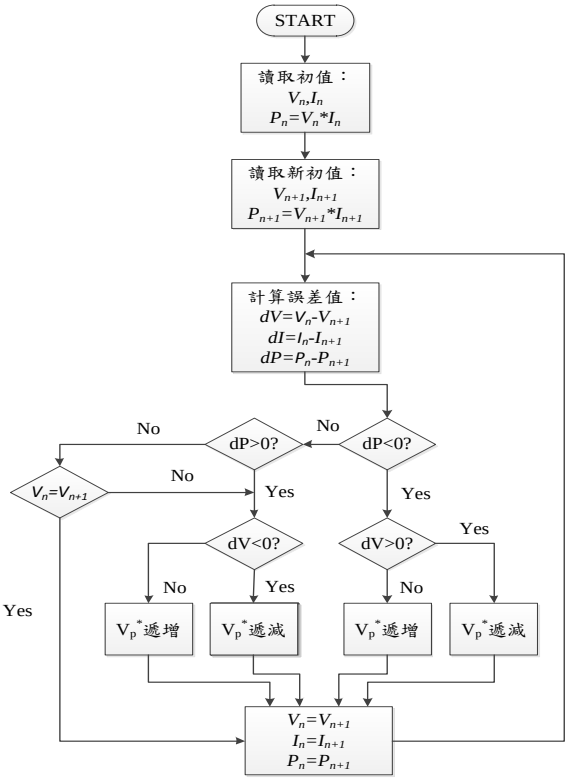
Appendix Figure F5.5

MPPT Control Method

(a) Perturbation Observation Method Concept




(b) Perturbation Observation Method Procedure



# Experiment 6 Three-Phase Four-Wire Battery Energy Storage System

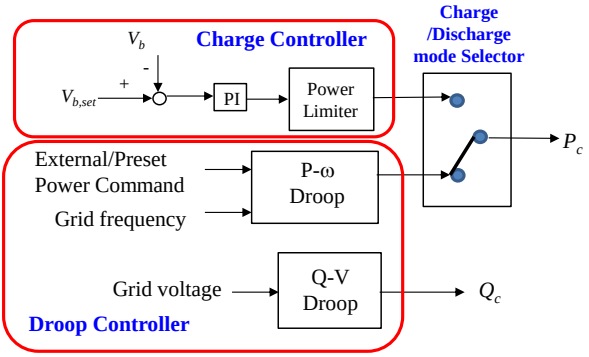
Due to the previous chapters having already discussed the applications of DC-DC converters and standalone inverters, the following sections will focus on the energy management controller in grid-connected mode.

## A. P-ω and Q-V droop control

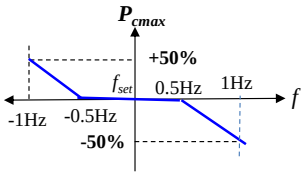
In the event of normal grid operation, the energy management controller is depicted in Appendix F6.1(a). The real power command for the inverter can originate from the battery charger or from an external (or preset) command regulating the load level. To assist in supporting the grid voltage, the PCS must adjust the real and reactive power commands based on the grid voltage and frequency. Appendix F6.2(b) illustrates the P-ω droop control method. When the grid frequency falls below the normal $f_{set}$ value, the PCS provides real power higher than the original set value. Conversely, when the grid frequency exceeds the normal $f_{set}$ value, the real power output is reduced. Here, the adjustment range of P-ω is set to ±1Hz. The normal real power output setting is maintained within ±0.5Hz. If it exceeds 0.5Hz, the output setting will be linearly increased (or decreased). When it reaches ±1Hz, it will increase or decrease by 50%. Figure Appendix F6.1(c) shows the Q-V droop adjustment method. The Q-V droop adjustment range is set to ±20% of the rated voltage. When the $V_{pcc}$ voltage is lower than the rated value, the PCS provides a higher virtual power than the original setting. On the contrary, when the $V_{pcc}$ voltage is higher than the rated value, the virtual power output setting is reduced. The adjustment method is linear increase or decrease, and when the voltage reaches ±20% of the rated voltage, the virtual power setting value is adjusted to ±50%.

Figure Appendix F6.1

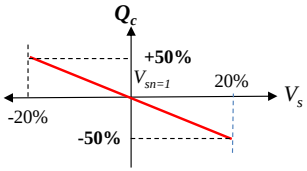
Grid-connected mode controller during normal operation of the municipal power supply(a) Composition of Power Management Controller




(b) P-ω Droop Control




(c) Q-V Droop Control




## B. PQ Controller and Active Power Filter (APF) Controller

Figure Appendix F6.2 includes the PQ controller and APF controller, which are located within the management controller's inner loop. The PQ controller receives commands (*Pc* and *Qc*) generated by the aforementioned power management controller, adjusts them through Proportional-Integral (PI) control to obtain the current commands $i_{oqcm}$ and $i_{odcm}$, and then the APF controller derives the final current commands. The purpose of the APF controller is to compensate for load current harmonics (q and d axes), reactive power, and load current imbalance. To achieve these compensation functions, it utilizes the load current on the q-axis ($i_{Lq}$) to obtain the fundamental wave of the active load current ($i_{Lq1}$) through a low-pass filter, calculates the harmonic of the active

current ($i_{Lqh}$) from the difference between the two, and finally, the current command on the q-axis is obtained by adding ioqcm and iLqh ($i_{oqca}$=$i_{oqcm}$+$i_{Lqh}$), enabling the PCS to compensate for the active current harmonics of the load. The reactive power and reactive current harmonics of the load need to be fully compensated, so the current command on the d-axis is obtained by adding $i_{odcm}$ and $i_{Ld}$ ($i_{odca}$=$i_{odcm}$+$i_{Ld}$). To compensate for the load current imbalance, the current command on the 0-axis is generated from the 0-axis component of the load current ($i_{o0ca}$=$i_{L0}$).

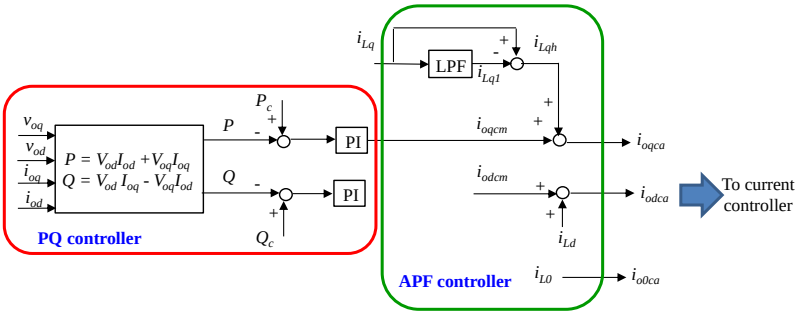



Figure Appendix F6.2 PQ Controller and APF Controller

## C. Phase-Locked Loop Controller

The Phase-Locked Loop (PLL) controller, as shown in Figure Appendix F6.3, determines the presence of grid voltage. When the Grid-on signal is selected, it uses the grid signal on the d-axis ($V_{sd}$) to generate a frequency correction signal (Δω) through a Proportional-Integral controller. Adding Δω to the preset frequency $\omega_0$ yields the phase-locked frequency $\omega_1$, which, after integration, produces the angle signal θ. This θ is then fed back to the abc-dq axis transformation, achieving synchronization when Δω is corrected to zero. The PLL output frequency signal can also be used for grid voltage frequency detection, and the θ angle can be used to generate synchronized sine wave signals. In the absence of grid power, the Grid-on signal selects the PLL to generate the angle signal θ from the preset frequency $\omega_0$ for use in independent mode axis transformation.

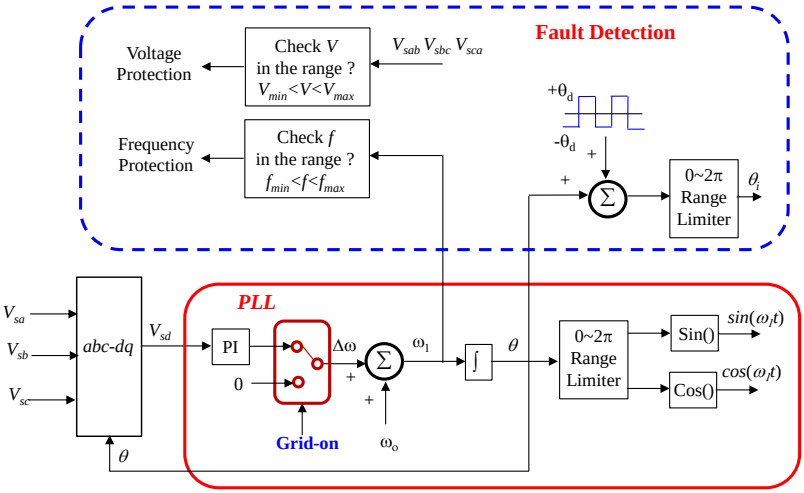



Figure Appendix F6.3 Phase-Locked Loop (PLL) Controller

# Experiment 7 Three-Phase Four-Wire Hybrid System

Experiment seven integrates experiments five and six to form a hybrid system, using one phase of the interleaved converter from experiment six as a photovoltaic converter. The design method is the same as before, so it will not be elabor