Three-phase Inverter Experiment Module

PEK-130

USER MANUAL

GW INSTEK PART NO. 82EK-11000M01

ISO-9001 CERTIFIED MANUFACTURER

GW INSTEK

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Table of Contents

Introduction

As the figure 0.1 shown, PEK-130, the Three Phase Inverter Module, is based on the structure of Three Phase Three Wire Inverer with fully digital control system. The purpose of this it, as shown in the figure 0.2, is to provide a learning platform for power converter of specifically digital control, having users, via PSIM software, to understand the principle, analysis as well as design of power converter through simulating process. More than that, it helps convert, via SimCoder tool of PSIM, control circuit into digital control and proceed to simulation with the circuit of DSP, eventually burning the control program, through simulating verification, in the DSP chip. Also, it precisely verifies the accuracy of designed circuit and controller via control and communication of DSP.

Figure 0.1

Experiment module of three-phase inverter

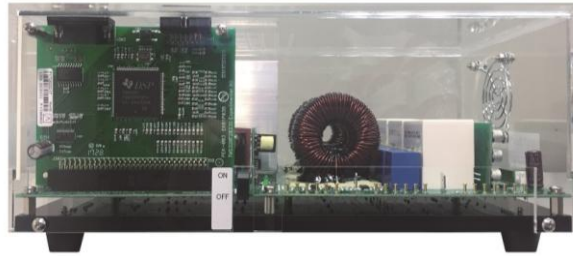
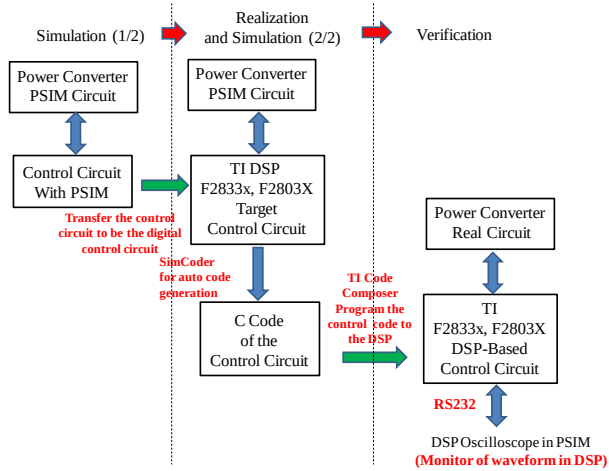


Figure 0.2

The process in details



Thre are 4 experiments can be fulfilled by PEK-130 as follows:

1. Three Phase SVPWM Inverter
2. Three Phase Stand-alone Inverter
3. Three Phase Grid-connected Inverter
4. Single Phase Three-arm Rectifier-Inverter

In addition to PEK-130, it is required to utilize PEK-005A auxiliary power module as figure 0.3 shown and PEK-006 JTAG burning module as figure 0.4 shown for experiments. Also, PTS-3000 experiment platform as figure 0.5 shown is necessary for completing the experiments.

Figure 0.3

Auxiliary power module

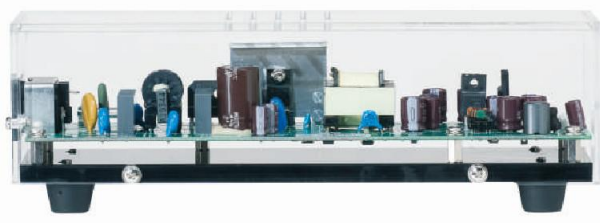


Figure 0.4

JTAG burning module

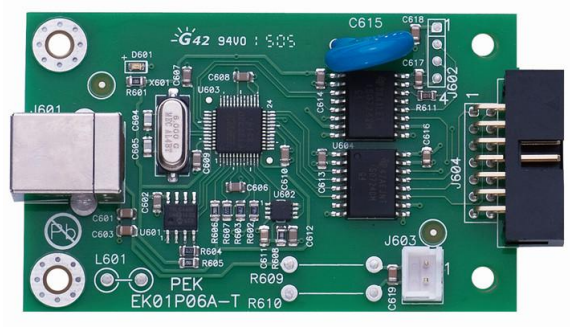


Figure 0.5

PTS-3000 experiment platform

Refer to the appendix A for the circuit diagrams of PEK-130, which can be divided into power circuit, sensing circuit, drive circuit and protection circuit. The sensing circuit is further divied into 2 sections; one is for test point measurement, and the other one is for feedback DSP control, both of which have varied attenuation amplifications individually as the following table 0-1 and table 0-2 shown.

Table 0.1 PEK-130 test point measurement ratio

	Sensing item	Sensing ratio
1	DC link voltage (VDC)	0.037
2	Inverter A phase output current (IO-A)	0.8
3	Inverter B phase output current (IO-B)	0.8
4	Inverter C phase output current (IO-C)	0.8
5	Inverter A phase load current (IL-A)	0.8
6	Inverter B phase load current (IL-B)	0.8
7	Inverter C phase load current (IL-C)	0.8
8	Inverter output AB arm line voltage (VO-AB)	0.019
9	Inverter output BC arm line voltage (VO-BC)	0.019
10	Inverter output CA arm line voltage (VO-CA)	0.019
11	Grid-connected AB arm line voltage (VS-AB)	0.019
12	Grid-connected BC arm line voltage (VS-BC)	0.019
13	Grid-connected CA arm line voltage (VS-CA)	0.019

Table 0.2 PEK-130 DSP feedback ratio

	Sensing item	Sensing ratio
1	DC link voltage (VDC)	0.02
2	Inverter A phase output current (IO-A)	0.3
3	Inverter B phase output current (IO-B)	0.3
4	Inverter C phase output current (IO-C)	0.3
5	Inverter A phase load current (IL-A)	0.3
6	Inverter B phase load current (IL-B)	0.3
7	Inverter C phase load current (IL-C)	0.3
8	Inverter output AB arm line voltage (VO-AB)	0.01
9	Inverter output BC arm line voltage (VO-BC)	0.01
10	Inverter output CA arm line voltage (VO-CA)	0.01
11	Grid-connected AB arm line voltage (VS-AB)	0.01
12	Grid-connected BC arm line voltage (VS-BC)	0.01
13	Grid-connected CA arm line voltage (VS-CA)	0.01

The Description on Chapters

See the chaper arrangements as follows

Introduction	Briefly describes the experimental method, experimental items and circuit setup of the teaching aid. It also explains the contents of each chapter.
Experiment 1 Three-phase SVPWM inverter	Learns the theories of three-phase SPWM and Space Vector PWM, the measuring method of voltage and current for open-loop of three-phase inverter module, the pin layout of TI F28335 DSP IC, the setting for PWM and A/D module of DSP and the method of monitoring DSP internal signal by RS232.
Experiment 2 Three-phase individual inverter	Learns the modularization method for three-phase inverter, axis conversion method for abc-dq, controller design of current and voltage loops, RMS voltage loop design, hardware layout of inverter and SimCoder programming, etc.
Experiment 3 Three-phase grid-connected inverter	Learns the method of phase-lock loop of three-phase grid connected inverter, the controller design of current loop and voltage loop, the hardware layout and the grid-connected SimCoder programming, etc.
Experiment 4 Single-phase three-arm rectifier inverter	It is available to be used for single-phase on-line UPS due to the circuit with 3-arm. This experiment helps you learn the working mode of UPS, controller design of current loop and voltage loop for Rectifier and Inverter, the hardware layout and the SimCoder programming, etc.

Experiment 1 – Three Phase SVPWM Inverter

The purpose of experiment

Learns the principle of three-phase SPWM and Space Vector PWM, the measuring method of open-loop voltage and current for three-phase inverter module, the pin layout of TIF28335 DSP IC, the A/D and PWM module settings of DSP, the DSP internal signal monitored by RS232, etc.

The principle of experiment

1.1 Three-phase SPWM

The principle of sinusoidal pulse width modulation (SPWM) is to compare the three-phase sinusoidal voltage command by controller with the triangular wave followed by comparator to produce PWM signal drive interver, the output from which will be akin to sinusoid with voltage waveform of equivalent frame and inequivalent width. Based on the scale and frequency of sine wave voltage and triangular wave, 2 indexes below can be defined, one of which is Modulation Index as the following description:

$$m_a = \frac{\hat{V}_{control}}{\hat{V}_{tri}} \quad (1.1)$$

In the above equation where Vcontrol is voltage peak scale of three-phase sine wave, whist Vtri indicates peak scale of triangular wave.

The other one is Frequency Modulation Ratio with the definition below:

$$m_f = \frac{f_s}{f_l} \tag{1.2}$$

In the above equation where f_s is triangular wave frequency, whereas f_1 indicates sine wave voltage frequency.

Figure 1.1

Three-phase inverter circuit

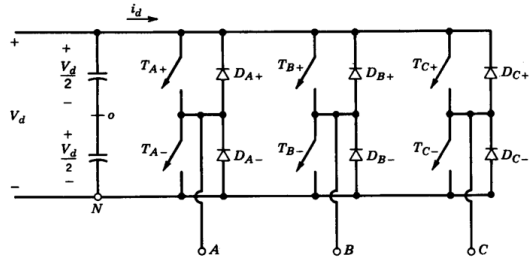
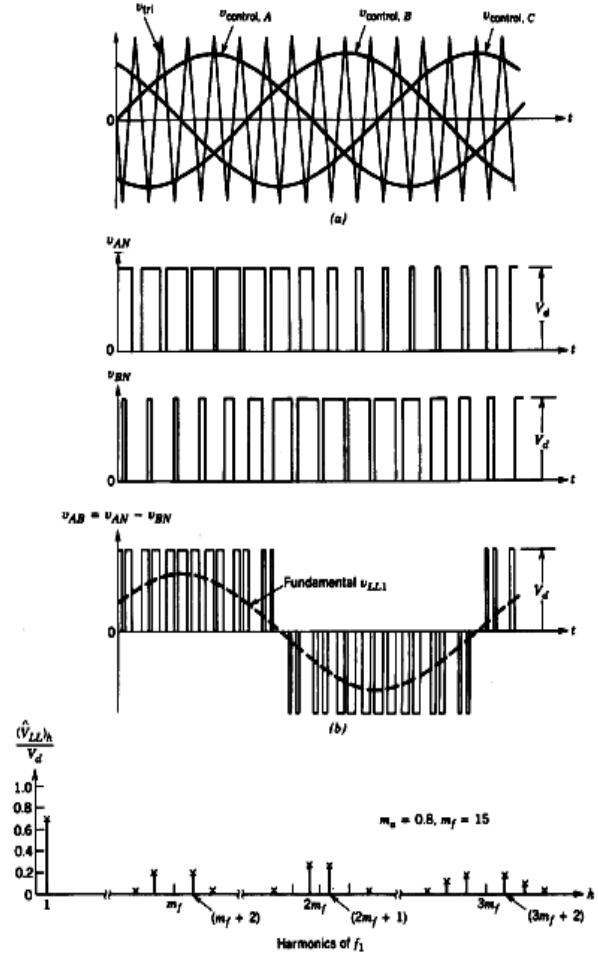


Figure 1.2

SPWM



Take A phase in the figure 1.1 for example, the peack value of basic waveform of voltage V_{AN} is illustrated below:

$$(\hat{V}_{AN})_1 = m_a \frac{V_d}{2} \tag{1.3}$$

Basic waveform line subtracts line voltage scale (RMS):

$$\begin{aligned} V_{LL1} \\ (\text{line}-\text{line, rms}) &= \frac{\sqrt{3}}{\sqrt{2}}(\hat{V}_{AN})_1 \\ &= \frac{\sqrt{3}}{2\sqrt{2}} m_a V_d \\ &\cong 0.612 m_a V_d \quad (\text{ma} \le 1.0) \end{aligned} \tag{1.4}$$

When ma $\leqq$1, from the known linear modulation zone of inverter; that is, when peak value of input sinusoidal voltage command is smaller than that of triangular wave, the input voltage scale will be directly proportional to that of the basic waveform line of output voltage of inverter subtracting the line voltage scale.

1.2 PWM (Space Vector PWM, SVPWM)

Space Vector PWM utilizes the concept of voltage space vector, which produces rotational voltage vector space via switch change for six power components of inverter. The typical three-phase inverter is shown as the figure 1.3, each phase of which has 2 switch components that are S_1, S_3, S_5 located in the upper arm and S_2, S_4, S_6 located in the lower arm, respectively. In the control mode of space vector PWM, the conduction state of each switch component of inverter is complementary, which means that when upper arm is in conduction state lower arm will close and vice versa. In general, a delay time is added prior to switch conduction for comtrol in case of damage to the power components due to simultaneous conduction of upper and lower arms power components. The delay time is called “deadband”.

The switch conduction state for each arm of a, b, c phase is defined here. When a = 1, the upper arm is in switch conduction state and the lower arm switch closes. By contrast, when a = 0, the upper arm switch closes and the lower arm is in switch conduction state. Therefore, there are up to 8 output states for three-phase inverter, and the output results (DC voltage – VDC) of line to line voltage

and phase voltage from each output state are displayed in detail in the table 1.1 below.

Figure 1.3 Architecture of typical three-phase power inverter

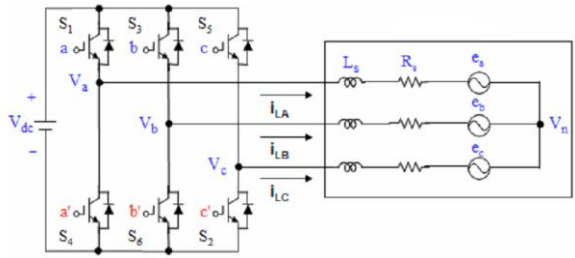


Table 1.1 Changed state of three-phase inverter

Voltage Vectors	Switching Vectors			Line to neutral voltage			Line to line voltage		
	a	b	c	V_{an}	V_{bn}	V_{cn}	V_{ab}	V_{bc}	V_{ca}
V_0	0	0	0	0	0	0	0	0	0
V_1	1	0	0	2/3	-1/3	-1/3	1	0	-1
V_2	1	1	0	1/3	1/3	-2/3	0	1	-1
V_3	0	1	0	-1/3	2/3	-1/3	-1	1	0
V_4	0	1	1	-2/3	1/3	1/3	-1	0	1
V_5	0	0	1	-1/3	-1/3	2/3	0	-1	1
V_6	1	0	1	1/3	-2/3	1/3	1	-1	0
V_7	1	1	1	0	0	0	0	0	0

From the above table 1.1, we may understand the relation between phase voltage and line volage output from three-phase inverter that the table 1.2 is formed by coordinate axis converted to $a\beta$ flat surface and the relation of conversion is as the following:

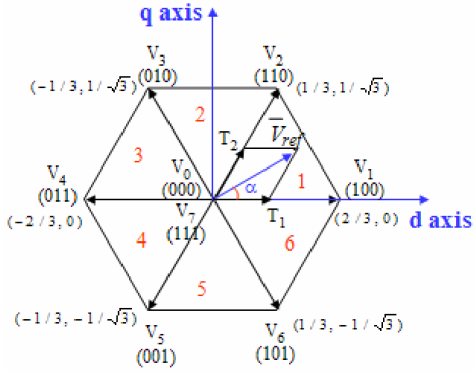
$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix}$$

Table 1.2 Switch change state

	V_α	V_β
$\vec{V}_0$	0	0
$\vec{V}_1$	$-\frac{V_{DC}}{3}$	$-\frac{V_{DC}}{3}$
$\vec{V}_2$	$-\frac{V_{DC}}{3}$	$\frac{V_{DC}}{3}$
$\vec{V}_3$	$-\frac{2V_{DC}}{3}$	0
$\vec{V}_4$	$\frac{2V_{DC}}{3}$	0
$\vec{V}_5$	$\frac{V_{DC}}{3}$	$-\frac{V_{DC}}{\sqrt{3}}$
$\vec{V}_6$	$\frac{V_{DC}}{3}$	$\frac{V_{DC}}{\sqrt{3}}$
$\vec{V}_7$	0	0

Hence, the different 8 voltage vectors can be acquired via the 8 switch change states. The 8 voltage vectors are called the basic voltage vectors where 6 are effective voltage vectors ($\vec{V}_1$, $\vec{V}_2$, $\vec{V}_3$, $\vec{V}_4$, $\vec{V}_5$ and $\vec{V}_6$) and the rest 2 are zero vectors ($\vec{V}_0$ and $\vec{V}_7$). As the figure 1.4 shown, we can divide voltage space surface, via the 6 effective voltage vectors, into 6 zones where the α axis and β axis of αβ surface are relative to the horizontal axis and vertical axis of AC motor, respectively. $\vec{V}_{ref}$ indicates reference voltage vector of output.

Figure 1.4 Basic vector space



Any size of reference voltage $\vec{V}_{ref}$ for output can be displayed by any 2 vectors of the 6 effective voltage vectors from the figure 1.4. And the output voltage within the component (conduction time) of 2 effective voltage vectors can be acquired by algebra.

1.3 Axis Conversion

(1) Static coordicate conversion

Convert the three-phase abc static coordinates into the *aβ* static coordinate axis system, which is called Clark conversion. Based on the figure 1.5 indicating the relation of 2 coordinates system, we can acquire the following coordinate conversion formula:

$$\begin{bmatrix} f_\alpha \\ f_\beta \\ f_o \end{bmatrix} = [T] \begin{bmatrix} f_a \\ f_b \\ f_c \end{bmatrix} \quad (1.5)$$

Where $f_\alpha \cdot f_\beta \cdot f_o$ indicate the variable quantity of voltage and current under the *aβ* axis, whilst $f_a \cdot f_b \cdot f_c$ indicate the variable quantity of voltage and current under the *abc* axis

$$[T] = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix}$$ is coordinate axis matrix

On the contrary, when coordinate axis $\alpha\beta$ is converted to three-phase abc coordinate system, we call the conversion as the reverse Clark conversion, the formula of which is illustrated below:

$$\begin{bmatrix} f_a \\ f_b \\ f_c \end{bmatrix} = [T]^{-1} \begin{bmatrix} f_\alpha \\ f_\beta \\ f_o \end{bmatrix} \quad (1.6)$$

Where:

$[T]^{-1} = \begin{bmatrix} 1 & 0 & 1 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} & 1 \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} & 1 \end{bmatrix}$ is coordinate axis matrix

The above is the relation between three-phase abc coordinate system and static coordinate system, of which the undetermined coefficient before conversion matrix is $\frac{2}{3}$ when adopting non-power invariant rule, while it will be $\sqrt{\frac{2}{3}}$ when adopting power invariant rule, which is what we utilize here. In addition, when conducting the static coordinate axis conversion, with respect to three-phase balance system, zero-sequence symmetrical component $f_o = \frac{1}{3}(f_a + f_b + f_c)$ can be simply ignored. The figure 1.6 indicates the waveform of abc static coordinate axis converted to $\alpha\beta$ static coordinate axis via PSIM simulation.

Figure 1.5 Static coordinate axis

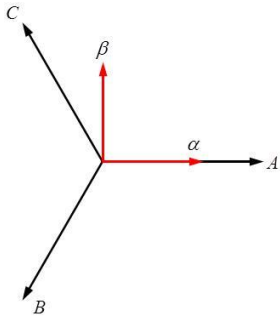
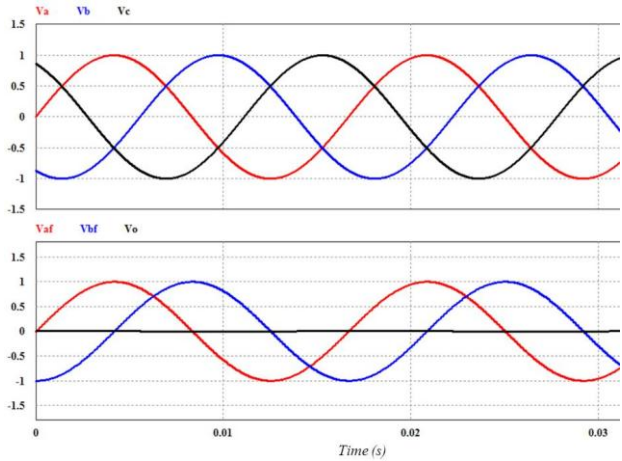


Figure 1.6 Waveform of PSIM simulated static coordinate axis conversion



(2) Synchronized rotational coordinate axis conversion

In the last chapter where abc static coordinate system is conveted, via coordinate axis conversion, to $\alpha\beta$ static coordinate axis system, we further convert $\alpha\beta$ static coordinate axis to DQ synchronized rotational coordinate axis system, which can be called Park conversion. If three-phase system is balanced, zero-axis symmetrical component can be ignored and both DQ axis and $\alpha\beta$ axis will be put on the two-dimensional surface. As the figure 3.7 displayed, the rotational coordinate will swirl in accord with the speed of angle ω_e, and therefore the coordinate conversion formula can be acquired as following:

$$\begin{bmatrix} f_\alpha \\ f_\beta \end{bmatrix} = [Q] \begin{bmatrix} f_d \\ f_q \end{bmatrix} \tag{1.7}$$

Where:

$$[Q] = \begin{bmatrix} \cos(\theta_e) & \sin(\theta_e) \\ -\sin(\theta_e) & \cos(\theta_e) \end{bmatrix}$$

By contrast, if DQ axis of rotational coordinate system is converted to $\alpha\beta$ coordinate system, we call it reverse Park conversion with the affiliated conversion formula shown below:

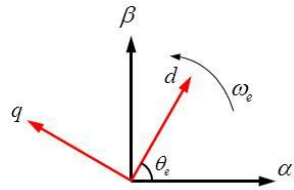
$$\begin{bmatrix} f_d \\ f_q \end{bmatrix} = [Q]^{-1} \begin{bmatrix} f_\alpha \\ f_\beta \end{bmatrix} \tag{1.8}$$

Where:

$$[Q]^{-1}=\begin{bmatrix}\cos(\theta_e) & -\sin(\theta_e)\\ \sin(\theta_e) & \cos(\theta_e)\end{bmatrix}$$

θ_e is included angle, which can be displayed $\theta_e=\int_0^t \omega_e dt+\theta_e(0)$

Figure 1.7 Synchronized rotational coordinate axis



(3) Arbitrary rotational coordinate axis conversion

From the above 2 sections, we can realize that the static coordinate axis conversion and synchronized rotational axis conversion can be projectd to DQ coordinate axis via abc coordinate system. As the figure 1.8 shown where coordinate coversion formula is as follows:

$$\begin{bmatrix}f_d\\ f_q\\ f_o\end{bmatrix}=[R]\begin{bmatrix}f_a\\ f_b\\ f_c\end{bmatrix} \tag{1.9}$$

Where:

$$[R]=\frac{2}{3}\begin{bmatrix}\cos(\theta_e) & \cos(\theta_e-\frac{2\pi}{3}) & \cos(\theta_e+\frac{2\pi}{3})\\ -\sin(\theta_e) & -\sin(\theta_e-\frac{2\pi}{3}) & -\sin(\theta_e+\frac{2\pi}{3})\\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2}\end{bmatrix}$$

By contrast, to convert rotational coordinate system DQ axis to $\alpha\beta$ coordinate system, which is called reverse Park conversion and the conversion formula is displayed below:

$$\begin{bmatrix}f_a\\ f_b\\ f_c\end{bmatrix}=[R]\begin{bmatrix}f_d\\ f_q\\ f_o\end{bmatrix} \tag{1.10}$$

Where:

$$[R]^{-1}=\begin{bmatrix}\cos(\theta_e) & -\sin(\theta_e) & 1\\ \cos(\theta_e-\frac{2\pi}{3}) & -\sin(\theta_e-\frac{2\pi}{3}) & 1\\ \cos(\theta_e+\frac{2\pi}{3}) & -\sin(\theta_e+\frac{2\pi}{3}) & 1\end{bmatrix}$$

If it is a three-phase balance system, the zero-phase symmetrical component $f_o=\frac{1}{3}(f_a+f_b+f_c)$ can be simply ignored.

Figure 1.8 Arbitrary rotational coordinate axis

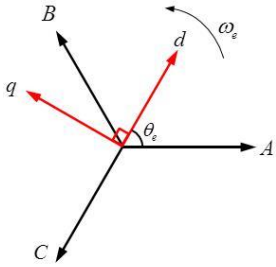
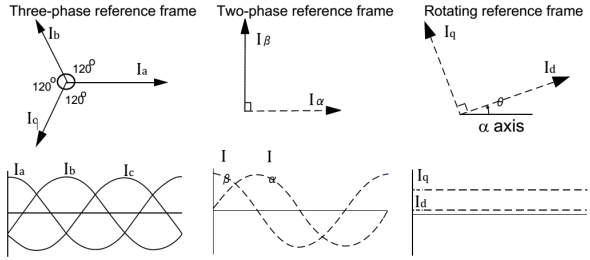


Figure 1.9 Diversified coordinate axis



Prior to the previous abc-dq axis conversion, due to the fact that the voltage detected by three-phase three-wire circuit voltage is line voltage (V_{ab}、V_{bc}、V_{ca}), it is required to utilize the following conversion of line-abc to phase-abc to acquire the virtual-phase voltage (V_{an}, V_{bn} and V_{cn}:

$$\begin{bmatrix}V_{an}\\ V_{bn}\\ V_{cn}\end{bmatrix}=\frac{1}{3}\begin{bmatrix}1 & 0 & -1\\ -1 & 1 & 0\\ 0 & -1 & 1\end{bmatrix}\begin{bmatrix}V_{ab}\\ V_{bc}\\ V_{ca}\end{bmatrix} \quad (1.11)$$

1.4 Zero Sequence Injection SVPWM

In general, Space Vector PWM is used for switch control method in terms of digitalized inverter control realization because [t improves

utilization rate of voltage of inverter and reduces number of times for switch change; however, more calculations to determine switch conduction and dead time also come along with SVPWM. Zero sequence injection PWM shares the identical benefits as SVPWM and is widely adopted in recent years due to much simpler calculation. The principle of zero sequence injection PWM is as the following figure 1.10. When DC link voltage has a virtually neutral point *o*, the voltage of A arm and B arm relative to *o* point is illustrated as follows:

$$V_{ao} = V_{an} + V_{no} \tag{1.12}$$

$$V_{bo} = V_{bn} + V_{n0} \tag{1.13}$$

$$V_{ab} = V_{an} - V_{bn} \tag{1.14}$$

The (1.14) clearly indicates that V_{no} within line voltage will be erased by 2 arms differential; hence, it is feasible to utilize V_n to enhance utilization rate of inverter voltage. The voltage range of each arm relative to *o* point is displayed below:

$$\frac{-V_d}{2} \le V_{ao} \le \frac{V_d}{2} \tag{1.15}$$

Therefore

$$\frac{-V_d}{2} \le V_{an} + V_{no} \le \frac{V_d}{2} \tag{1.16}$$

The range of V_{no} voltage can be acquired from the (1.16) as follows:

$$\frac{-V_d}{2} - V_{an} \le V_{no} \le \frac{V_d}{2} - V_{an} \tag{1.17}$$

When considering the voltage range of V_{an}, it turns out:

$$\frac{-V_d}{2} - V_{\min} \le V_{no} \le \frac{V_d}{2} - V_{\max} \tag{1.18}$$

Where

$$V_{\max} = Max(V_{\text{an}}, V_{bn}, V_{cn}) \tag{1.19}$$

$$V_{\max} = Max(V_{\text{an}}, V_{bn}, V_{cn}) \tag{1.20}$$

When setting V_{no} as the follows, we normally call it mean zero value zero sequence injection:

$$V_{no} = -\frac{1}{2}(V_{\max} + V_{\min}) \tag{1.21}$$

The control voltage waveform of mean zero value zero sequence injection PWM is shown as the figure 1.11. In this chapter we utilize this method to realize PWM; by substituting (1.21) into (1.12) we may acquire:

$$v_{coni} = V_{coni} - \frac{1}{2}(V_{con,\max} + V_{con,nin}) \ (i=A, B, C) \tag{1.22}$$

Where V_{coni} is the control voltage acquired by the calculation from the original control circuit, whilst v_{con} is the control voltage after mean zero sequence injection.

Figure 1.10 Architecture diagram of three-phase inverter

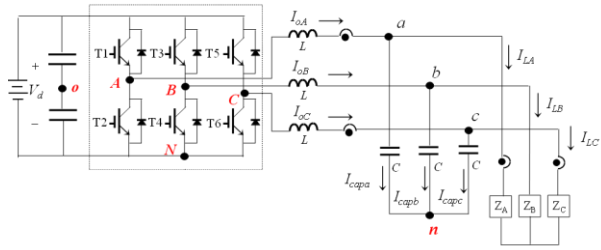
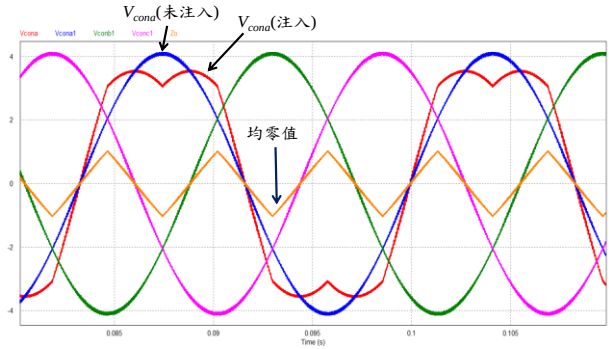


Figure 1.11 Mean zero value zero sequence injection PWM



Circuit Simulation

Inverter Specification

DC Voltage V_d = 100V

AC Voltage V_{LL} = $50V_{rms}$

F_s = 18kHz，V_{tri} = $10V_{pp}$ (PWM)

C_d = 330uF，L = 1mH，C = 10uF

K_s = 0.3 (current sensing factor)

K_v = 0.01 (AC voltage sensing factor)

K_v = 0.02 (DC voltage sensing factor)

As the figure 1.12 shown, of which the simulating circuit is constructed by the previous parameters, the simulating result under linear load mode is illustrated as the figure 1.13 below:

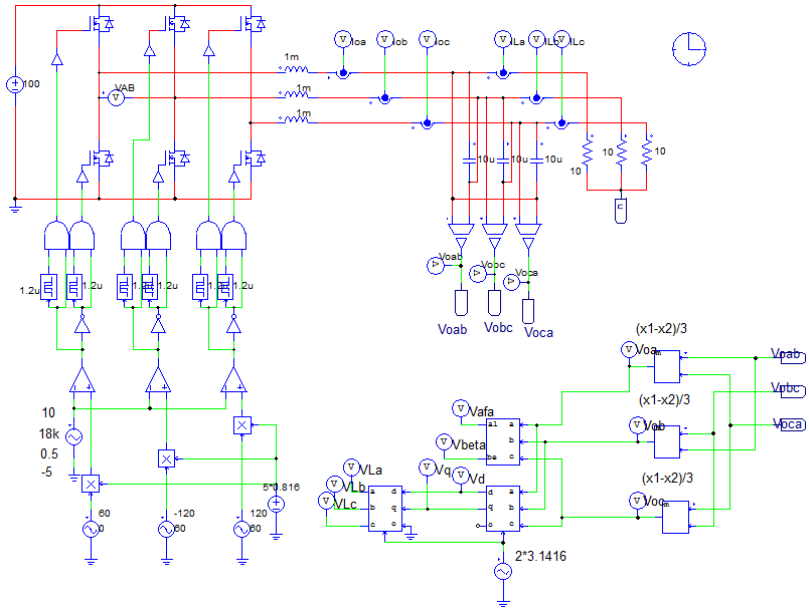


Figure 1.12 Inverter SPWM and axis conversion simulation

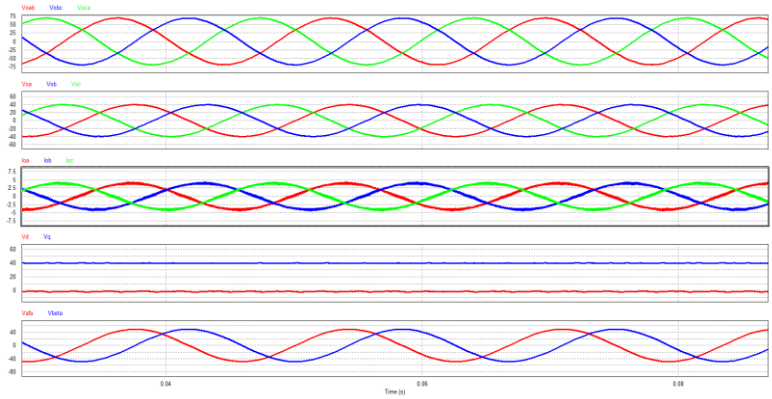


Figure 1.13 Inverter SPWM and simulating result of axis conversion

SimCoder Program Layout & Circuit Simulation

We are heading toward the second stage where the previous analog controller will be digitalized. Refer to the steps below:

(1) Main circuit and sensing establishment

The main circuit and sensing circuit of inverter are shown in the figure 1.14. The required sensing value under control is suggested to be within the range: DC: 0~3V, AC: -1.5V~1.5V.

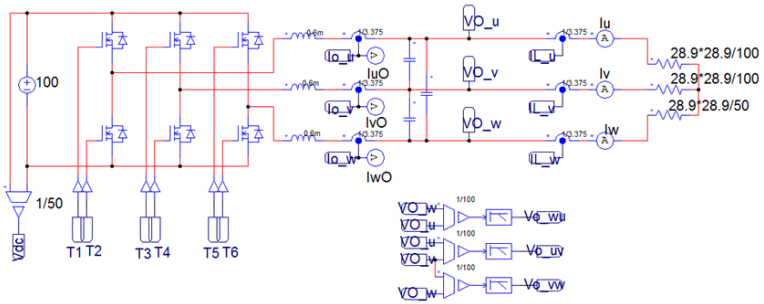


Figure 1.14 Main circuit and sensing circuit of inverter

(2) DSP hardware setup

As the figure 1.15 displayed, select TI F28335 Target followed by setting its pin use of GPIO. This module will utilize 3 groups of PWM & RS232 communication ports, a digital output as well as a digital input.

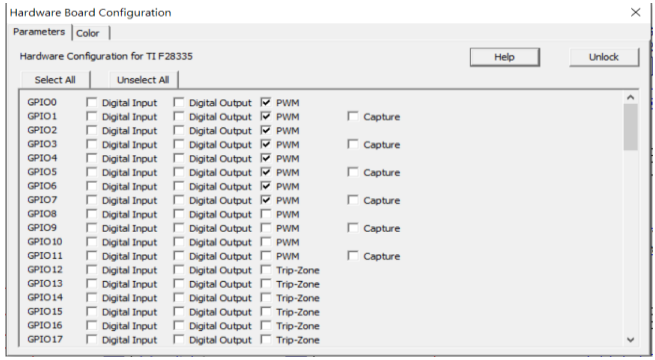
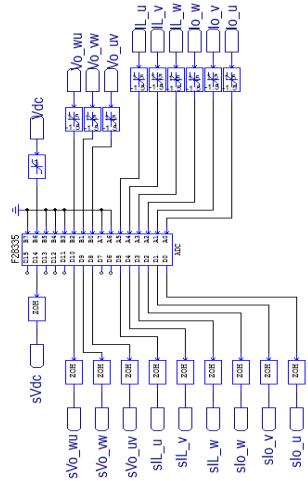


Figure 1.15 TI F28335 Target hardware setup

(3) A/D Converter setting

F28335 A/D Converter is divided into A and B groups, each of which has 8 channels; that is, 16 channels in total from 2 groups. This experiment senses DC voltage, AC output voltage, inverter output current and load current, etc., all of which utilize the 10 channels out of 16 in total. As the figure 1.16(a) displayed, except DC input voltage which is DC signal, the entire are AC signals. The internal setting of A/D Converter is illustrated as the figure 1.16(b) below:

(a)



(b)

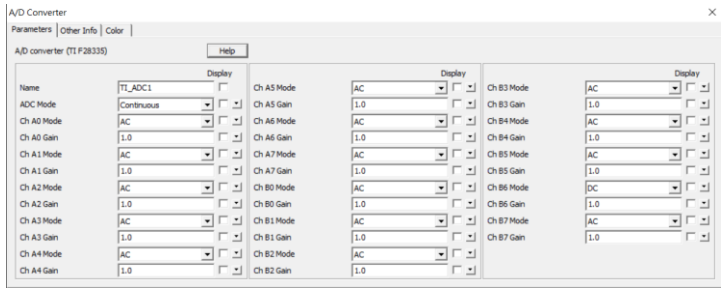
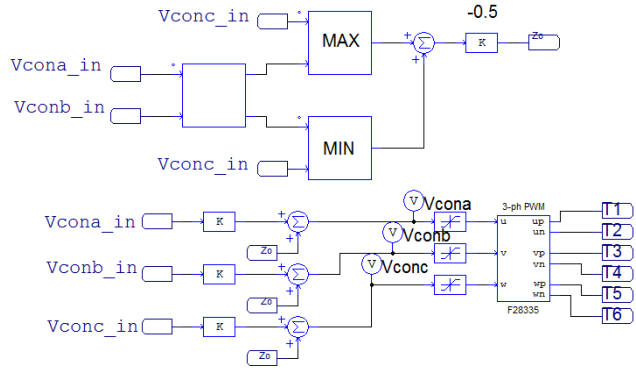


Figure 1.16 DSP A/D Converter Layout: (a) input signal connection diagram (b) internal setting

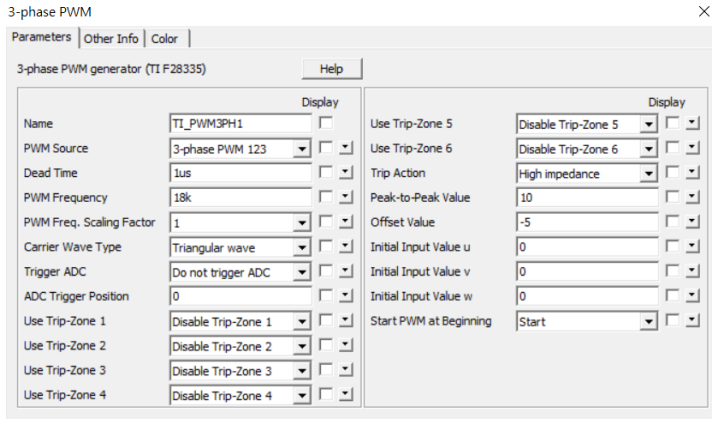
(4) PWM & the affiliated setting

PWM program and the affiliated setting are shown as the figure 1.17(a). The circuit includes zero sequence mean zero injection and PWM module, of which the setting is shown as the figure 1.17(b). The triangular wave utilizing up and down is of 18k Hz frequency with amplitude -5V~+5V along with blank time 1us.

(a)



(b)



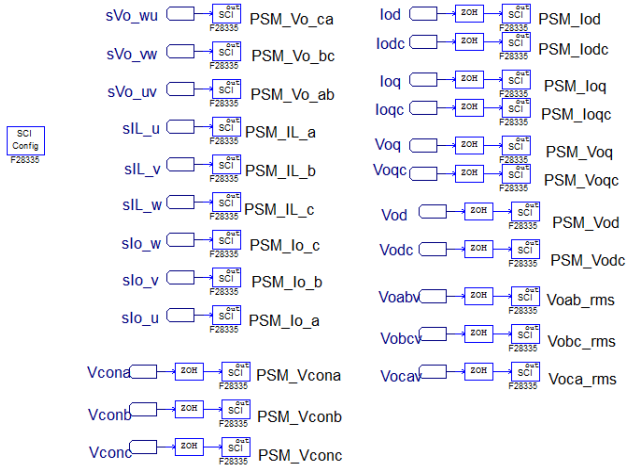
(b)

Figure 1.17 PWM program setting: (a) zero sequence mean zero injection PWM (b) PWM module setting

(5) Communication setting

In order to, during the implementation process, measure the signal of DSP control program so that the working condition of controller can be properly assured. PSIM provides the I/O interface of RS232 and the communication program of this experiment is shown as the figure 1.18. The figure 3.18(a) displays the target waveform by SCI. The figure 1.18(b) illustrates the setting of SCI module including communication port, communication speed, memory storage of debug and buffer, etc.

(a)



(b)

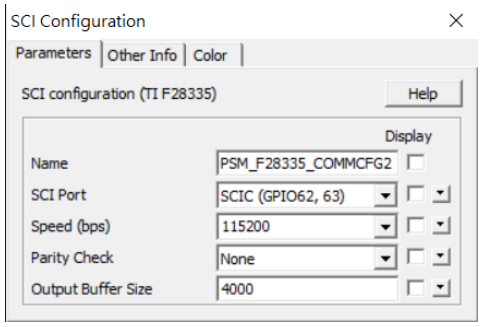


Figure 1.18 Communication program: (a) target signal (b) SCI module setting

(6) Simulation validation

After integrating the several steps of digital control program previously mentioned, it is viable to proceed to simulation. The three-phase SVPWM simulation circuit constructed by SimCoder is shown as the figure 1.19. The simulating result is shown as the figure 1.20 and 1.21. The simulating result of converting SPWM to SVPWM is displayed as the figure 1.22.

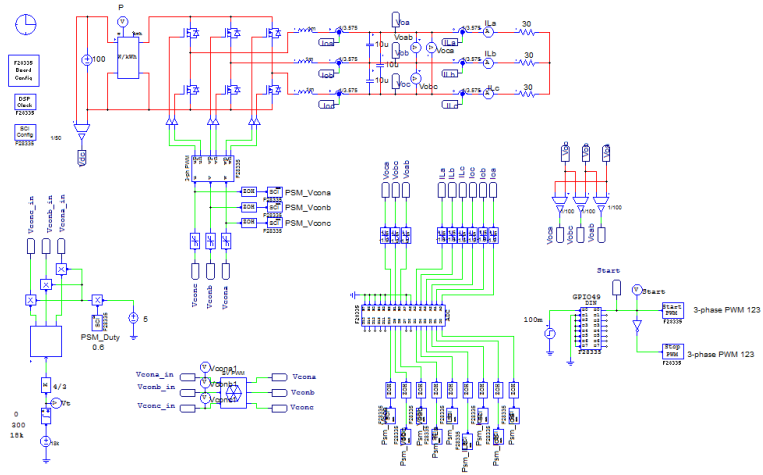


Figure 1.19 Inverter SVPWM simulating circuit constructed by SimCoder

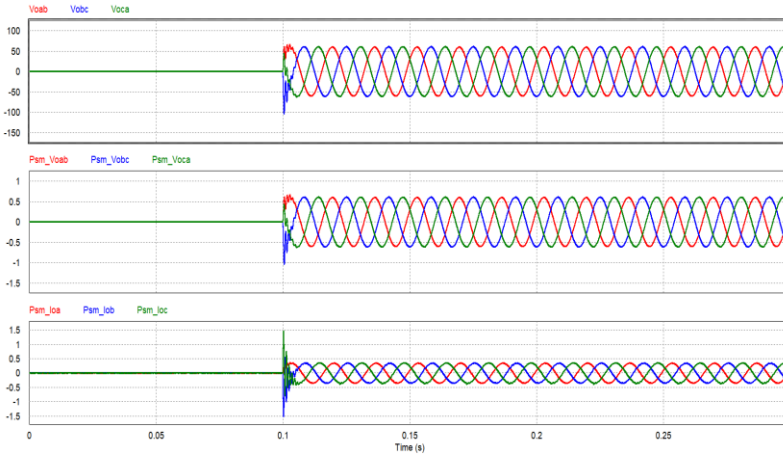


Figure 1.20 Inverter SVPWM simulating result constructed by SimCoder

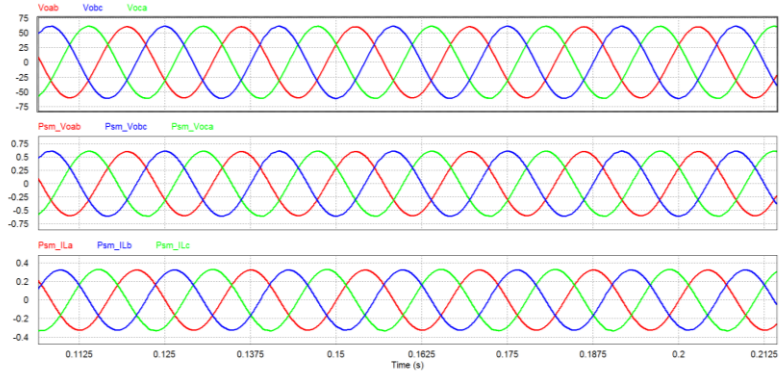


Figure 1.21 Simulating result of output voltage and output current of SVPWM

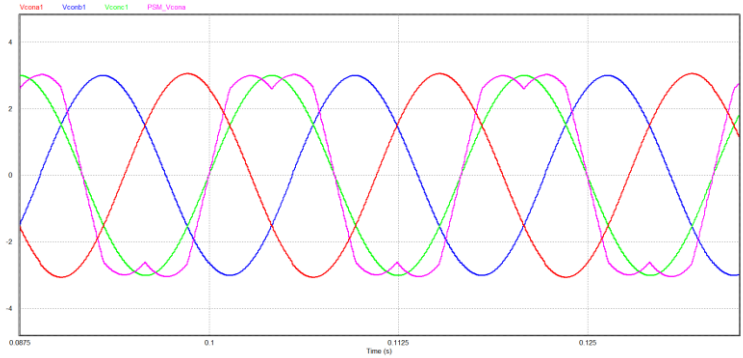


Figure 1.22 Simulating result of SPWM and SVPWM

The simulating circuit diagram of zero sequence injection PWM constructed by SimCoder is shown as the figure 1.23. This method is proposed specifically for SVPWM calculation, which is way to complicated and hard for utilization. The simulating result is shown as the figure 1.24 and 1.25. The simulating comparison result between zero sequence injection PWM and mean value zero sequence signal is illustrated as the figure 1.26.

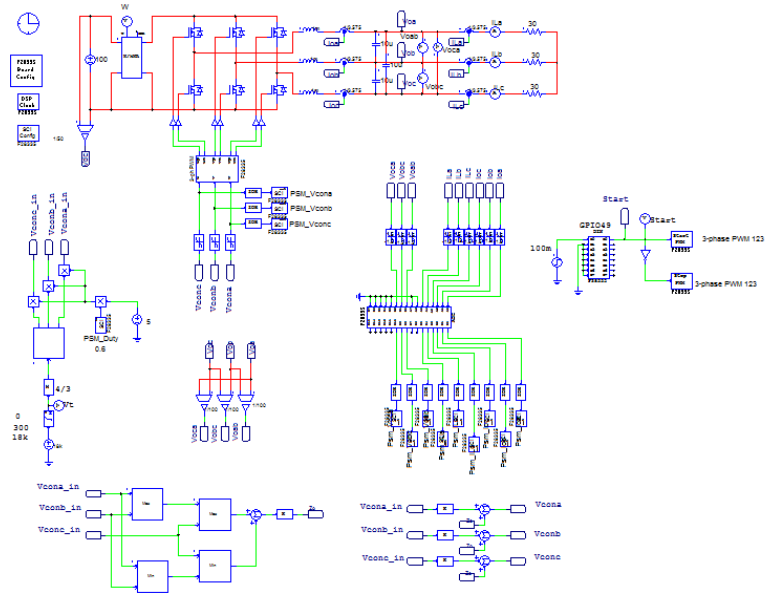


Figure 1.23 Zero sequence injection PWM simulating circuit constructed by SimCoder

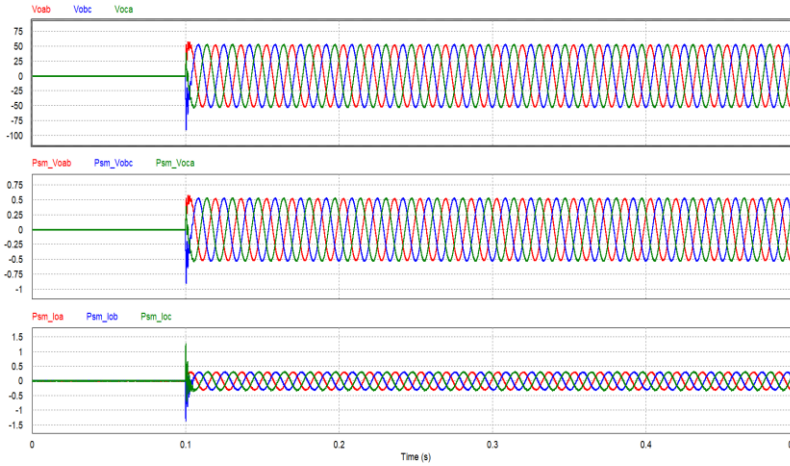


Figure 1.24 Zero sequence injection PWM simulating result constructed by SimCoder

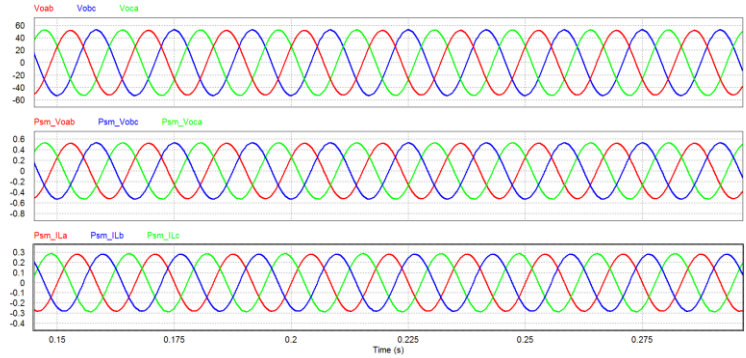


Figure 1.25 Simulating result diagram of output voltage and output current of zero sequence injection PWM

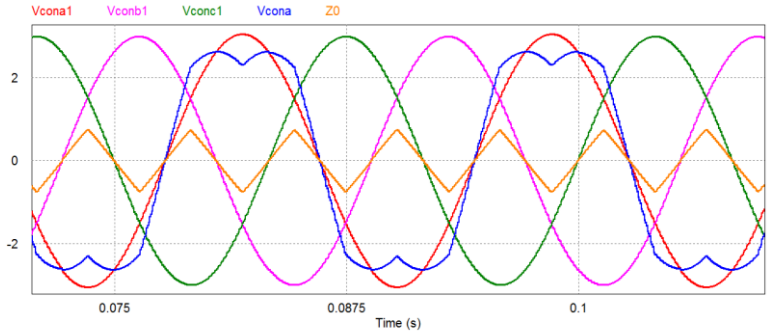


Figure 1.26 Simulating comparison result among SPWM, zero sequence injection PWM and mean value zero sequence signal

After simulating validation for integrated program, it is available to convert control program to, via PSIM SimCoder tool, C code.

Experiment Devices

The required devices for experiemt are as follows:

PEK-130 * 1

PEK-005A * 1

PEK-006 * 1

PTS 3000 * 1 (with GDS-2204E, PSW160-7.2 and GPL-300A)

PC * 1

Experiment Procedure

The experiment wiring is shown as the figure 1.27. Please follow it to complete wiring.

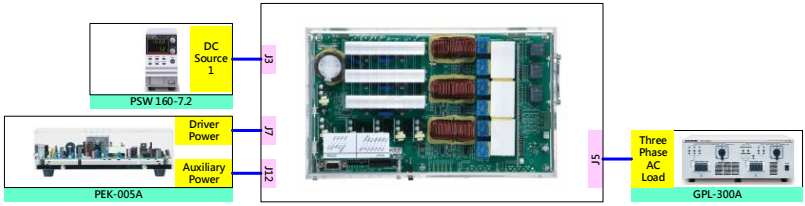


Figure 1.27 Experiment wiring figure

After wiring, make sure the PEK-130 switch is OFF followed by turning the PEK-005A switch ON. The DSP red indicator lights on as the figure 1.28 shown, which means the DSP power is steadily normal.

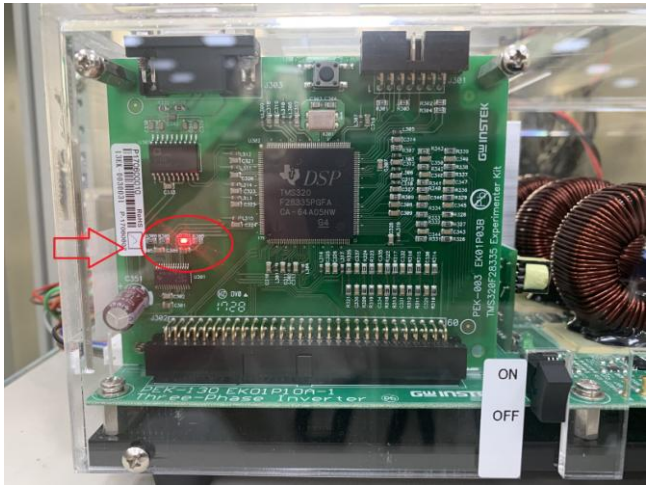


Figure 1.28 DSP normal status with light on

Refer to the appendix B for burning procedure to burn the PEK-130_Lab1_SVPWM_V11.0.3.psimsch program into DSP followed by referring to the appendix C for RS232 connection to proceed to connection.

Connect the test leads of oscilloscope to Vo-AB, Vo-BC and Vo-CA, respectively, as the figure 1.29 shown.

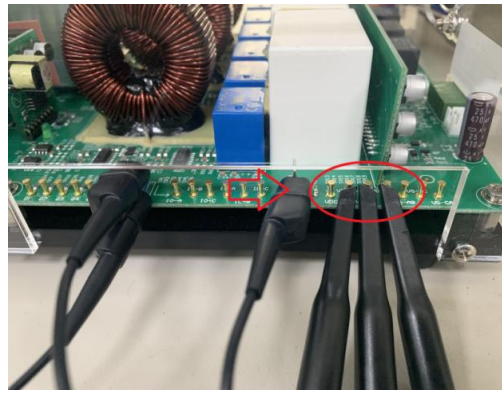


Figure 1.29 Oscilloscope test leads wiring

Set voltage 100V and current 3A for PSW 160-7.2. After powering on GPL-300A, set Resistance Load for Three Phase Load and set OFF for 1TS and 2TS, further setting ON for 3TS. The no load occurs then as the figure 1.30 shown.

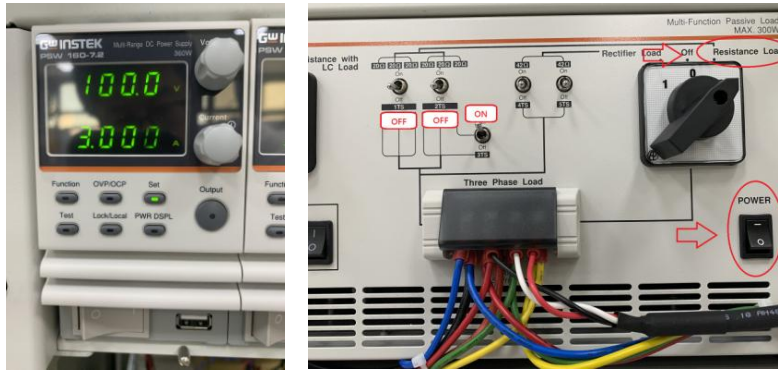


Figure 1.30 The settings of PSW 160-7.2 & GPL-300A

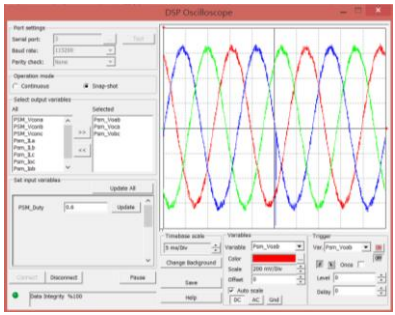
After setting up and PSW power output, turn on the switch of PEK-130.

Experiment Result

(1) Three Phase SVPWM

Figure 1.31(a) shows the voltage waveform when no load and the figure 1.31(b) indicates the result of RS232 sending back to PC side when no load.

(a)

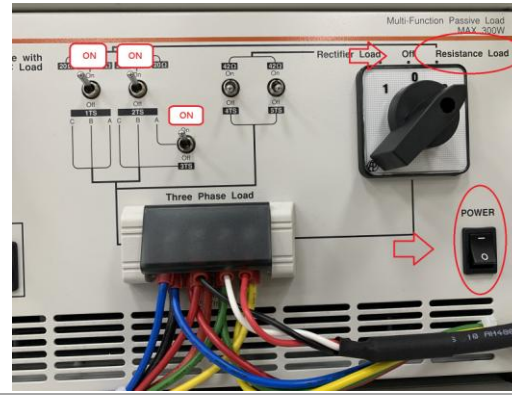


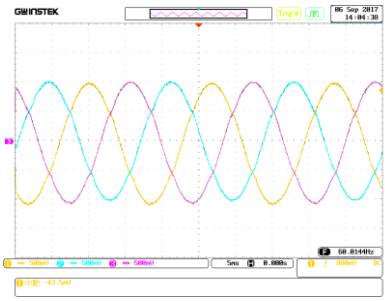
(b)

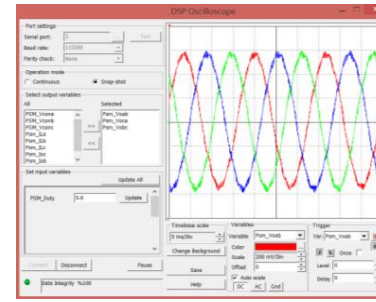
Figure 1.31(a) The voltage waveform when no load (b) The result of RS232 sending back to PC side

From the above no load test, when load-on outout for measurement, the set output of PSW 160-7.2 remains unchanged. Sets the 1TS, 2TS and 3TS of GPL-300A on and it turns out full load as the figure 1.32 shown. The figure 1.33(a) indicates the voltage waveform observed from Test Pin V_O-AB, V_O-BC and V_O-CA when full load. The figure 1.33(b) represents the result of RS232 sending back to PC when full load.

Figure 1.32
The full load setting of GPL-300A



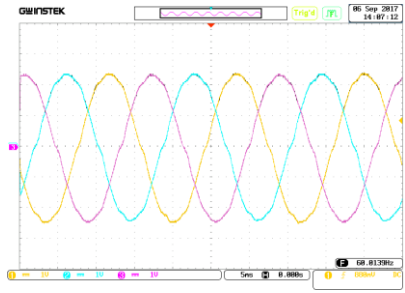


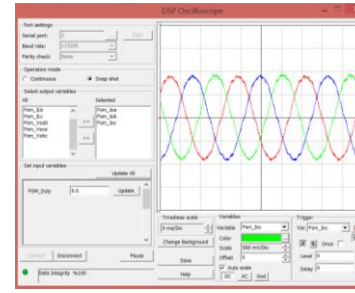


(a) (b)

Figure 1.33 (a) The voltage waveform when full load (b) The result of RS232 sending back to PC

When measuring current, place test leads on Test Pin I_O-A, I_O-B and I_O-C. The figure 1.34 (a) indicates the current waveform when full load. The figure 1.34 (b) indicates the result of RS232 sending back to PC when full load.





(a) (b)

Figure 1.34(a) The current waveform when full load (b) The result of RS232 sending back to PC

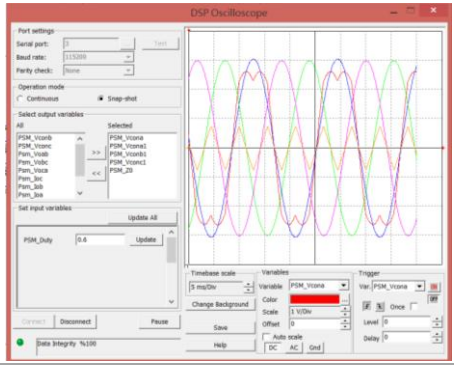
When completing the experiment, turn off the start key of PEK-130 followed by setting GPL-300A to OFF state and then turning off PSW 160-7.2.

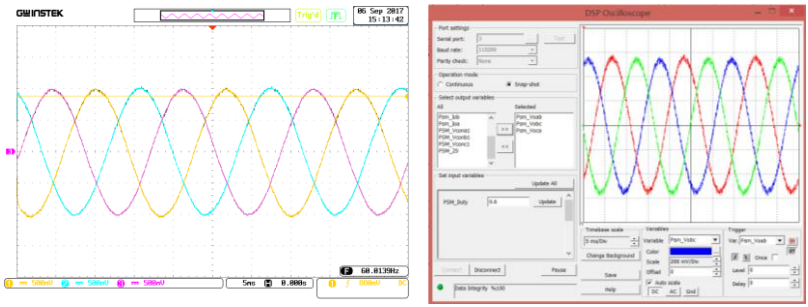
(2) Zero sequence injection PWM

Burn the program PEK-130_Lab1_ZSVPWM_V11.0.3.psimsch into DSP and repeat the above experiment steps. Figure 1.35 indicates the signal diagrams of SPWM, zero sequence injection PWM and mean value zero sequence sent back to PC. Figure 1.36(a) represents the voltage wavoform when no load. Figure 3.36(b) shows the result of RS232 sending back to PC when no load.

Figure 1.35

The signal diagrams of SWPM, zero sequence injection PWM and mean value zero sequence

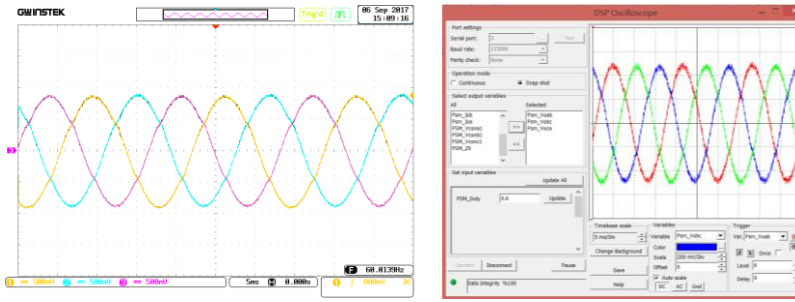




(a) (b)

Figure 1.36 (a) The voltage waveform observed from $V_{O\text{-}AB}$, $V_{O\text{-}BC}$ and $V_{O\text{-}CA}$ when no load (b) The result of RS232 sending back to PC when no load

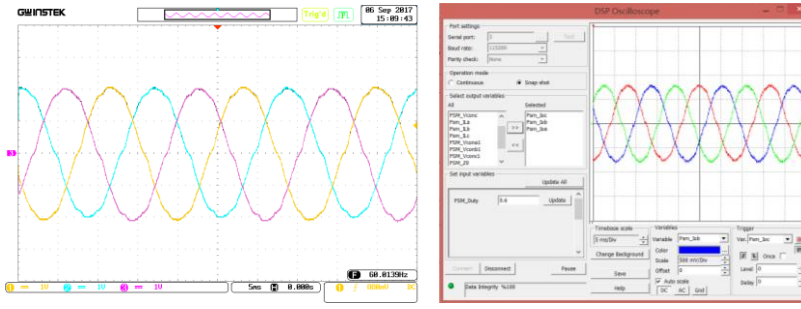
From the above no load test, when load-on outout for measurement, the set output of PSW 160-7.2 remains unchanged. Sets the 1TS, 2TS and 3TS of GPL-300A on and it turns out full load as the figure 1.32 shown. The figure 1.37(a) indicates the voltage waveform when full load. The figure 1.37(b) represents the result of RS232 sending back to PC when full load.



(a) (b)

Figure 1.37 (a) The voltage waveform observed from Vo-AB, Vo-BC and Vo-CA when full load (b) The result of RS232 sending back to PC when full load

When measuring current, place test leads on Test Pin Io-A, Io-B and Io-C. The figure 1.38 (a) indicates the current waveform when full load. The figure 1.38 (b) indicates the result of RS232 sending back to PC when full load.



(a) (b)

Figure 1.38 (a) The current waveform observed from Io-A, Io-B and Io-C when full load (b) The result of RS232 sending back to PC

Experiment 2 – Three Phase Stand-alone Inverter

The purpose of experiment

Learns the modularization of three-phase inverter, the axis conversion of abc-dq, the controller design of current loop and voltage loop, the RMS voltage loop design, the hardware layout of inverter and SimCoder programming, etc.

The principle of experiment

2.1 Three-phase 3-wire modularization and control method model derivation

Three-phase 3-wire inverter circuit is illustrated as the figure 2.1 in which n indicates the virtually voltage neutral point. The conventional control method utilizes dual-loop inductor current control as the figure 2.1 shown where we can, via inverter circuit, acquire as follows:

$$L\frac{dI_{oA}}{dt} = V_{AN} - V_{an} - V_{nN} \quad (2.1)$$

$$L\frac{dI_{oB}}{dt} = V_{BN} - V_{bn} - V_{nN} \quad (2.2)$$

$$L\frac{dI_{oC}}{dt} = V_{CN} - V_{cn} - V_{nN} \quad (2.3)$$

$$C\frac{dV_{an}}{dt} = I_{oA} - I_{LA} \quad (2.4)$$

$$C\frac{dV_{bn}}{dt} = I_{oB} - I_{LB} \tag{2.5}$$

$$C\frac{dV_{cn}}{dt} = I_{oC} - I_{LC} \tag{2.6}$$

Due to the 3-wire circuit that meets the following:

$$I_{oA} + I_{oB} + I_{oC} = 0 \tag{2.7}$$

(2.7) can be acquired via (2.1)+(2.2)+(2.3):

$$V_{nN} = \frac{(V_{AN} + V_{BN} + V_{CN}) - (V_{an} + V_{bn} + V_{cn})}{3} \tag{2.8}$$

By substituting (2.8) into (2.1)~(2.3) we can acquire the follows:

$$\begin{bmatrix} L\frac{dI_{oA}}{dt} \\ L\frac{dI_{oB}}{dt} \\ L\frac{dI_{oC}}{dt} \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ -\frac{1}{2} & 1 & -\frac{1}{2} \\ -\frac{1}{2} & -\frac{1}{2} & 1 \end{bmatrix}\left(\begin{bmatrix} V_{AN} \\ V_{BN} \\ V_{CN} \end{bmatrix} - \begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix}\right) \tag{2.9}$$

$$\begin{bmatrix} I_{capa} \\ I_{capb} \\ I_{capc} \end{bmatrix} = \begin{bmatrix} C\frac{dV_{an}}{dt} \\ C\frac{dV_{bn}}{dt} \\ C\frac{dV_{cn}}{dt} \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}\begin{bmatrix} I_{oA} \\ I_{oB} \\ I_{oC} \end{bmatrix} - \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}\begin{bmatrix} I_{LA} \\ I_{LB} \\ I_{LC} \end{bmatrix} \tag{2.10}$$

Where (i=A, B, C) is the output voltage of A, B and C arms; the widely usded switch control method for inverter is the three-phase SPWM and each arm of three-phase compares control voltage of phase-shift 120 degree (v_{conA}、v_{conB}、v_{conC}) with triangular wave (v_{tri}) individually to further trigger the switch of three arms, of each which output voltage can be indicated as the (2.11) below:

$$V_{iN} = (\frac{1}{2} + \frac{V_{coni}}{2v_{tm}})V_d \text{ (i=A, B, C)} \tag{2.11}$$

Where v_{tm} symbolizes the amplitude of triangular wave; substitute (2.11) into (2.9) to acquire (2.12) as follows:

$$\begin{bmatrix} L\frac{dI_{oA}}{dt} \\ L\frac{dI_{oB}}{dt} \\ L\frac{dI_{oC}}{dt} \end{bmatrix} = \frac{V_d}{3v_{tm}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ -\frac{1}{2} & 1 & -\frac{1}{2} \\ -\frac{1}{2} & -\frac{1}{2} & 1 \end{bmatrix} \begin{bmatrix} V_{conA} \\ V_{conB} \\ V_{conC} \end{bmatrix} - \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ -\frac{1}{2} & 1 & -\frac{1}{2} \\ -\frac{1}{2} & -\frac{1}{2} & 1 \end{bmatrix} \begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} \quad (2.12)$$

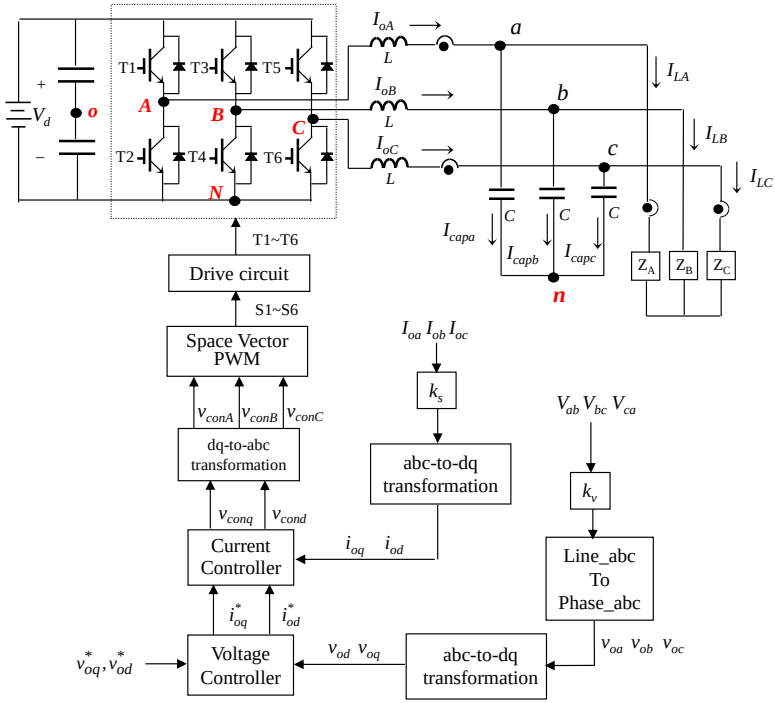


Figure 2.1 Three-phase 3-wire inverter

2.2Axis conversion

It is known that, via the relation between three-phase SPWM control voltage from (2.12) and each phase current, not only determined by control voltage, the each current control is also impacted by other phase control voltage, that is, each phase current control does Not decouple. Therefore, when designing controller

on the abc static frame directly, each phase, under the condition of three phase unbalanced, will influence one another, and the control performance will be afftected as well. In order to overcome the issue, it is generally adopted the method of coordinate axis conversion which decouples the mathematical model as the figure 2.2 shown where the three axes, a, b and c, are static frame that can indicate the components including phase volage and phase current of three phase inverter, whilst α and β indicate static frame of two phase that can convert AC quantity of three phase with difference of 120 degree in each phase to AC quantity of two phase with difference of 90 degree in each phase. *d*, *q* and zero are synchronized rotational axes. In the situation of three-phase balanced, the quantity of zero axis is zero, which can be simplified to vertical *qd* two axes. The equation of three-phase abc static coordinate axis and two-phase *dq0* synchronized rotational axis is as the following:

$$\begin{bmatrix} f_d \\ f_q \\ f_0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos\theta & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \\ \sin\theta & \sin(\theta - \frac{2\pi}{3}) & \sin(\theta + \frac{2\pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} f_a \\ f_b \\ f_c \end{bmatrix} \quad (2.13)$$

$$\begin{bmatrix} f_a \\ f_b \\ f_c \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta & 1 \\ \cos(\theta - \frac{2\pi}{3}) & \sin(\theta - \frac{2\pi}{3}) & 1 \\ \cos(\theta + \frac{2\pi}{3}) & \sin(\theta + \frac{2\pi}{3}) & 1 \end{bmatrix} \begin{bmatrix} f_d \\ f_q \\ f_0 \end{bmatrix} \quad (2.14)$$

Where

$$\theta = \omega t \quad (2.15)$$

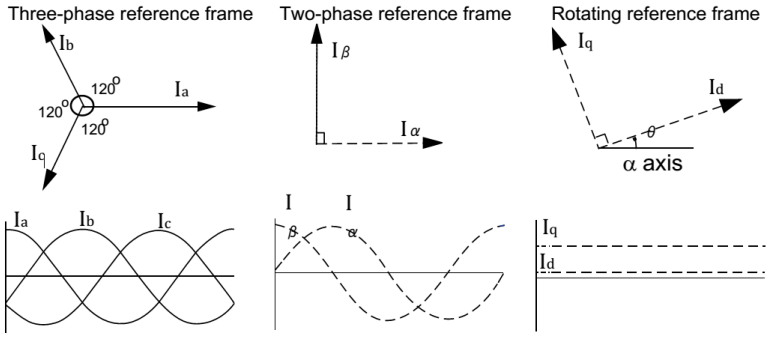


Figure 2.2 Diversified coordinate axes

The state equation of three-phase 3-wire inverter as the figure 2.1 can be acquired by substituting (2.10) and (2.12) into the axis conversion formula of (2.13) and (2.14):

$$\begin{bmatrix} L\dfrac{dI_{od}}{dt} \\ L\dfrac{dI_{oq}}{dt} \\ L\dfrac{dI_{o0}}{dt} \end{bmatrix} = \frac{V_d}{2V_{tm}} \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} V_{cond} \\ V_{conq} \\ V_{con0} \end{bmatrix} - \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} V_{od} \\ V_{oq} \\ V_{o0} \end{bmatrix} - \begin{bmatrix} 0 & \omega L & 0 \\ -\omega L & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_{od} \\ I_{oq} \\ I_{o0} \end{bmatrix} \quad (2.16)$$

$$\begin{bmatrix} C\dfrac{dV_{od}}{dt} \\ C\dfrac{dV_{oq}}{dt} \\ C\dfrac{dV_{o0}}{dt} \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} I_{od} \\ I_{oq} \\ I_{o0} \end{bmatrix} - \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} I_{od} \\ I_{oq} \\ I_{o0} \end{bmatrix} - \begin{bmatrix} 0 & \omega C & 0 \\ -\omega C & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_{od} \\ V_{oq} \\ V_{o0} \end{bmatrix} \quad (2.17)$$

Where V_{coni}(i=d, q) is control voltage of dq axis PWM and V_{tm} is the amplitude of PWM triangular wave.

Before conducting the previous abc-dq axis conversion, it is required to, due to the line voltage (V_{ab}, V_{bc}, V_{ca}) detected by three-phase 3-wire circuit voltage sensing circuit, utilize the conversion of Line-abc to Phase-abc to acquire the virtual phase voltage, V_{an}, V_{bn} and V_{cn}, within (2.12).

$$\begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 1 & 0 & -1 \\ -1 & 1 & 0 \\ 0 & -1 & 1 \end{bmatrix}\begin{bmatrix} V_{ab} \\ V_{bc} \\ V_{ca} \end{bmatrix} \tag{2.18}$$

2.3 Circuit Controller Design

It is feasible, via (2.16), to design current controller of inverter as the figure 2.3 displayed in which the current of both *d* and *q* axes cause pertube to each other. Therefore, the feedforward control signal from the figure 2.3 is used to erase the pertube. Instead, the other feedforward control signal v_{ff1} is used to erase the pertube from the phase output voltage to current loop. kv and ks are voltage and current sensing gain, respectively. The current error amplifier G_I can adopt *P* and *PI* or type II error amplifier to design. When adopting P control (G_I=k_1), current loop response can be acquired as follows via current feedback loop:

$$\frac{i_{o,i}^{*}}{i_{o,i}} = \frac{\frac{k_{pwm}k_s k_1}{L}}{s + \frac{k_{pwm}k_s k_1}{L}} = \frac{u_I}{s + u_I} \quad ,i = d, q \tag{2.19}$$

The u_I here indicates bandwidth of current loop:

$$u_I = \frac{k_{pwm} k_s k_1}{L} \tag{2.20}$$

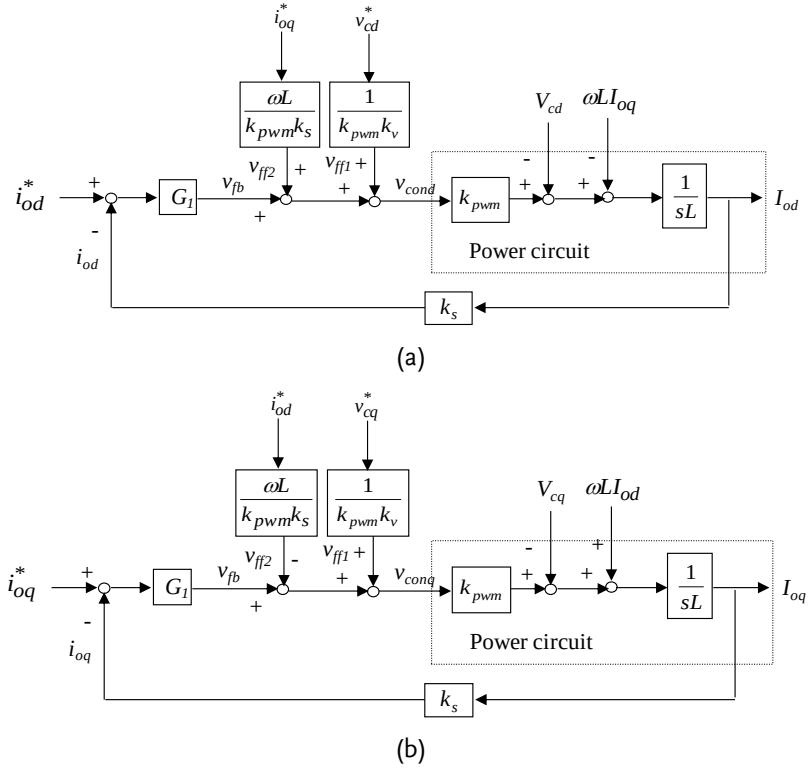
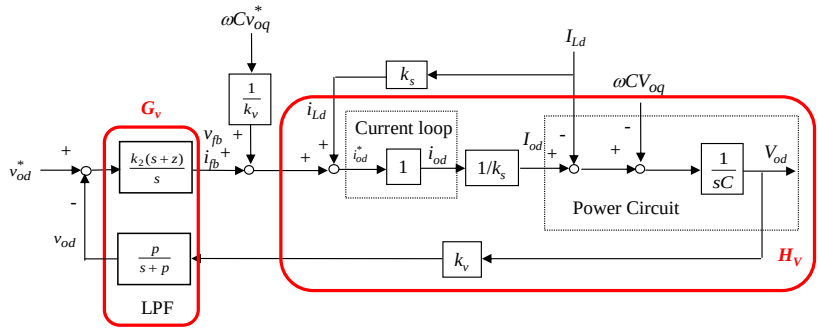


Figure 2.3 Current control loop of inverter: (a)d axis, (b)d axis

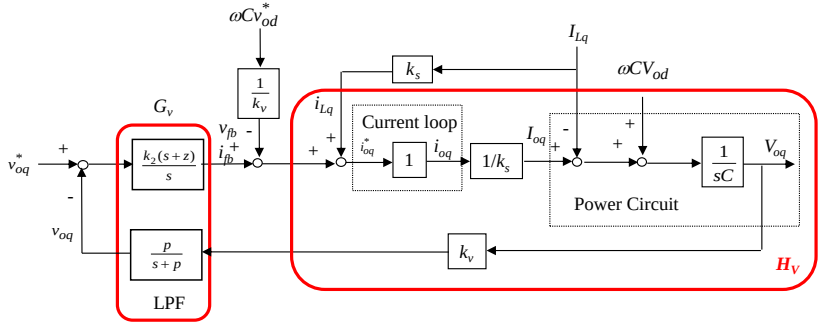
2.4 Voltage Controller

The voltage loop control block diagram of inverter is displayed as the figure 2.4 where electrical circuit block is drawn by (2.17). In addition, if bandwidth of current loop response has to be four times more than that of voltage loop response, the current loop response (2.19) can be regarded as "1" when analyzing voltage loop response. The voltage controller also adopts both feedforward and feedback controls. Due to sensing load current, the convert controller adds

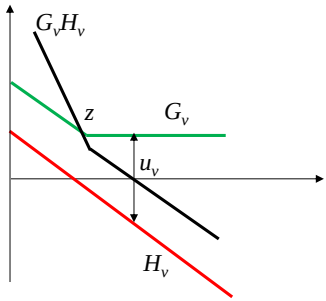
the sensing load current in current command to directly dissipate the perturbation that load current causes to voltage loop. In addition, it utilizes voltage command (v_{od}* and v_{oq}*) multiplied by ωC and adds other axis current command to dissipate the perturbation from capacitance current (ωCV_{od} and ωCV_{oq}). The voltage feedback controller G_v is the second-class error amplifier, which is composed of a feedback proportional integral controller and a low-pass filter (LPF) of voltage feedback signal. Refer to the figure 2.3(c) for the bode plot of voltage loop where bandwidth of voltage loop is positioned in the ¼ of bandwidth of current loop. In order to acquire well voltage adjustment rate and the three-phase voltage balance even under three-phase load unbalance, RMS value has to be able to adjust dynamically for each line voltage, respectively. The voltage RSM controller, which is provided by this thesis as the figure 2.5 shown, calculates RSM value of 3 line voltages individually followed by the comparison with RMS command v_{cm}* and, via G_m adjustment, the generation of an amplitude modified signal (A_{m1} A_{m2}, A_{m3}), which is used to modify the amplitude command A_{m0} of the original line voltage. The final line voltage amplitude commands A_{mab}, A_{mbc} and $A_{mca,\ etc.,}$ will be multiplied by the three-phase sinusoid sin(ωt+π/6), sin(ωt-π/2) and sin(ωt+5π/6), which is relative to virtual phase voltage phase shift by 30 degrees, to acquire the transient voltage command of three-phase line voltage. Eventually, the final voltage loop command v_{od}* and v_{oq}* can be obtained via *Line-abc* to *Phase-abc* conversion and *abc-dq* axis conversion.



(a)



(b)



(c)

Figure 2.4 Voltage control loop of inverter: (a)d axis, (b)q axis, (c)voltage loop bode plot

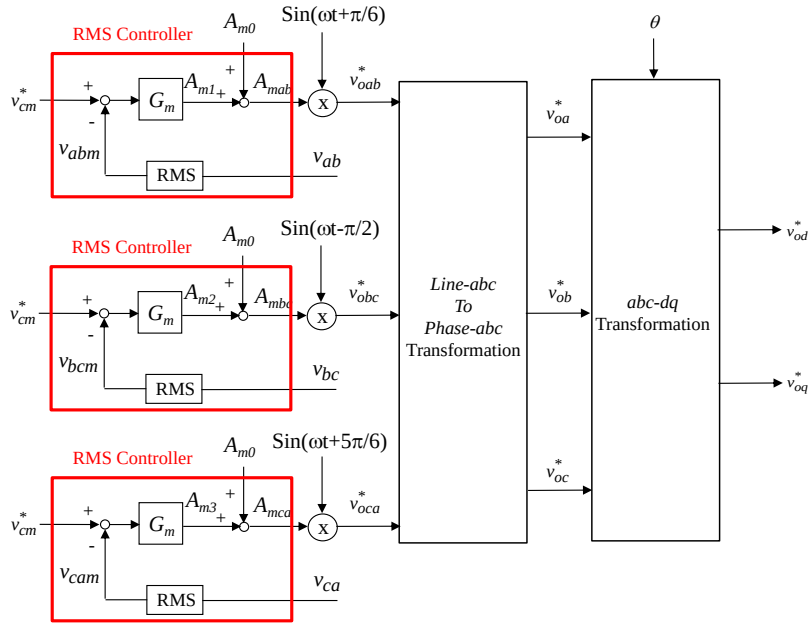


Figure 2.5 Voltage RMS value controller

Circuit Simulation

The 250W inverter conforming to the following specification will be applied to validate the several control methods mentioned previously.

Inverter Specification

- $R_a/R_b/R_c$ = 20 ohms，out-of-balance load $R_a/R_b/R_c$ = 20/10/10 ohms
- DC Voltage V_d = 100V，AC Voltage V_{LL} = $50V_{rms}$
- F_s = 18kHz，V_{tri} = 10Vpp (PWM)，C_d = 330uF，L = 1mH，C = 10uF
- K_s = 0.3 (current sensing factor)
- K_v = 0.01 (AC voltage sensing factor)
- K_v = 0.02 (DC voltage sensing factor)

PSIM Simulation

The simulating circuit built by the previous parameters is shown as the figure 2.6. The simulating result under linear balanced load is shown as the figure 2.7 and 2.8. That modify load to out-of-balance load $R_a/R_b/R_c$ = 20/10/10 ohms is shown as the figure 2.9. The simulating result under linear out-of-balance load is shown as the figure 2.10 and 2.11 in which dq axis current under out-of-balance load has 2 times ripples and both voltage and current follow the command closely.

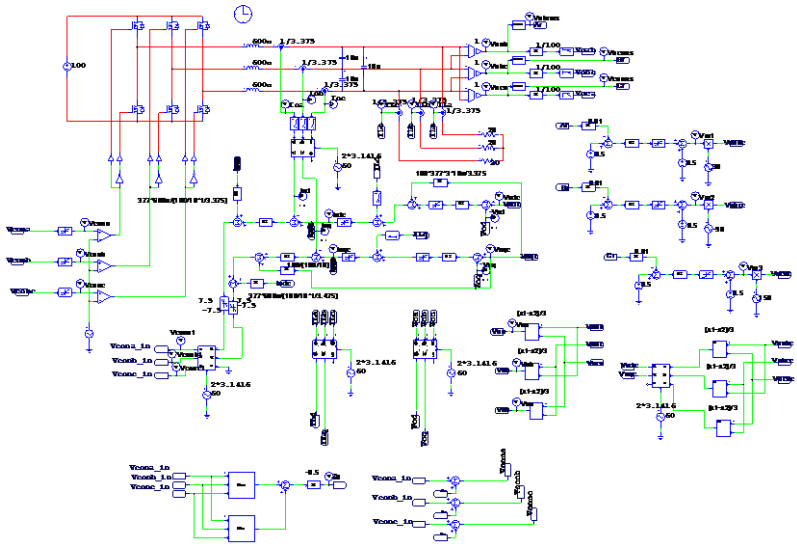


Figure 2.6 Three-phase inverter stand-alone simulating circuit

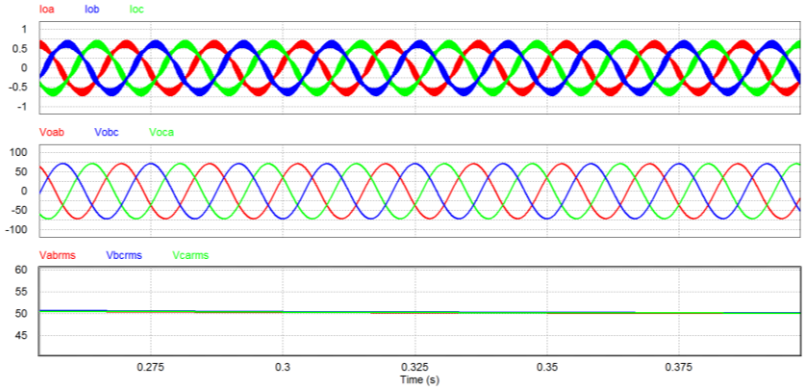


Figure 2.7 The simulating result of voltage output and current output under linear balanced load

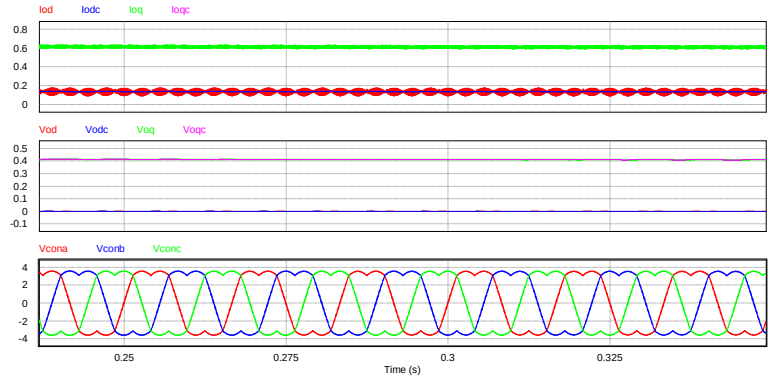


Figure 2.8 The simulating result of D axis and Q axis under linear balanced load

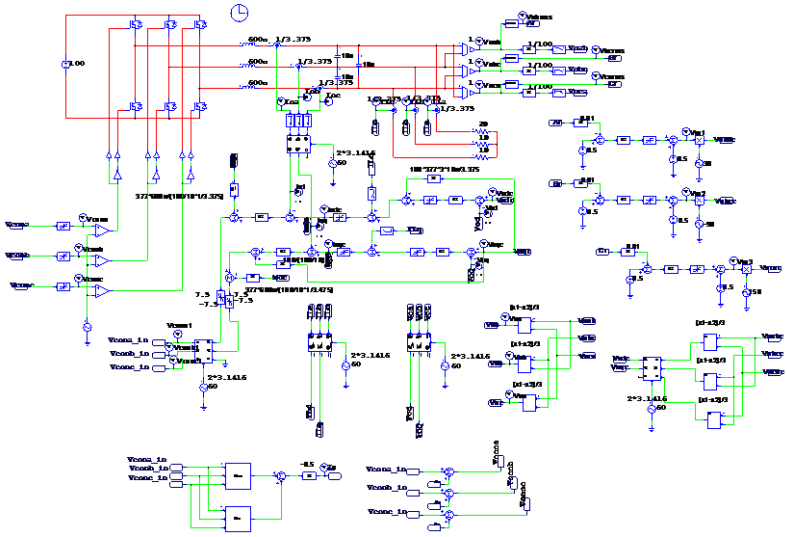


Figure 2.9 Three-phase inverter stand-alone out-of-balance load simulating circuit

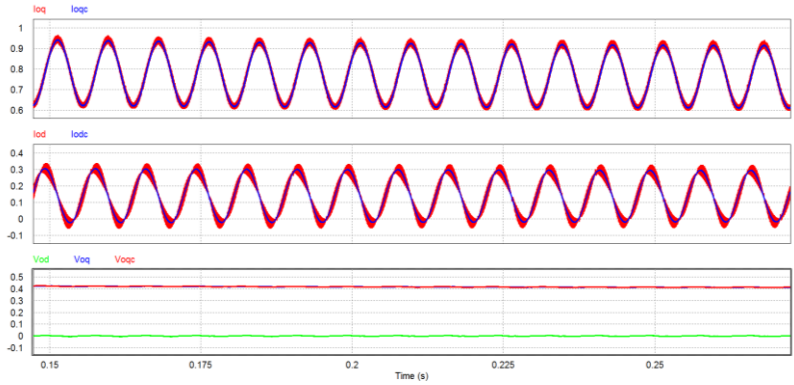


Figure 2.10 The simulating result of voltage and current tracking waveforms of out-of-balance load control loop

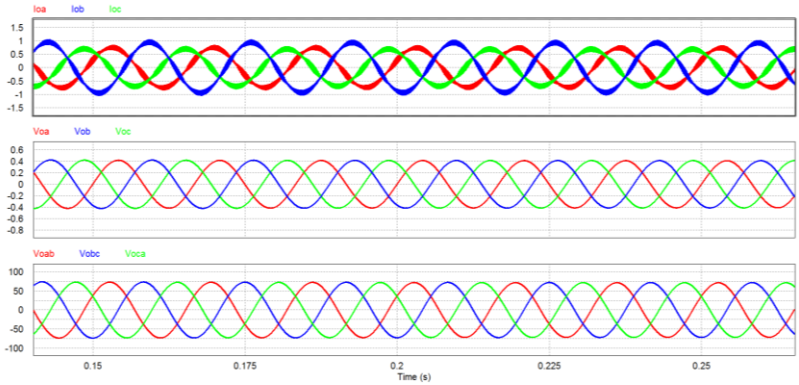


Figure 2.11 The simulating result of voltage output and current output under out-of-balance load

SimCoder Program Layout and Circuit Simulation

The stand-alone simulating circuit of three-phase inverter built by SimCoder is shown as the figure 2.12. The simulating result under linear balanced load is shown as the figure 2.13 and 2.14. The out-of-balance load simulating circuit of three-phase inverter stand-alone built by SimCoder is shown as the figure 2.15. The simulating result under linear out-of-balance load is shown in the figure 2.16 and 2.17.

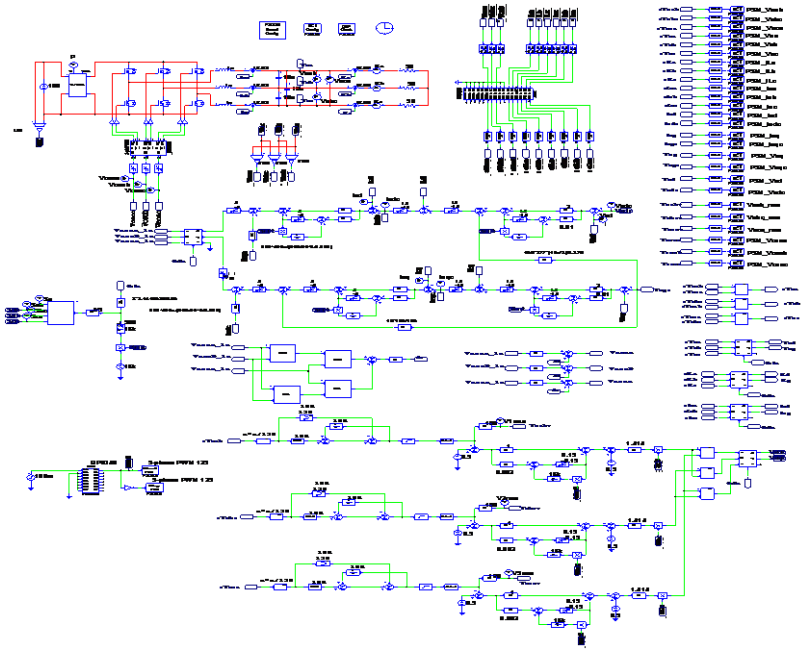


Figure 2.12 The three-phase inverter stand-alone simulating circuit built by SimCoder

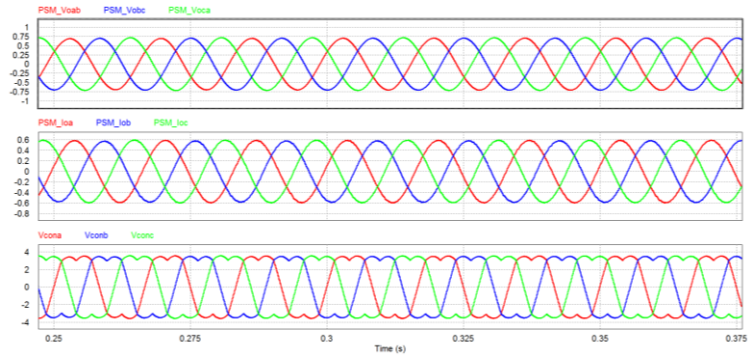


Figure 2.13 The simulating result of three-phase inverter stand-alone built by SimCoder

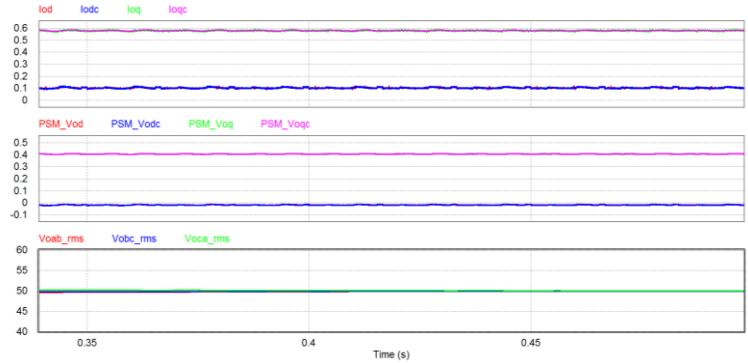


Figure 2.14 The simulating result of D axis and Q axis of three-phase inverter stand-alone built by SimCoder

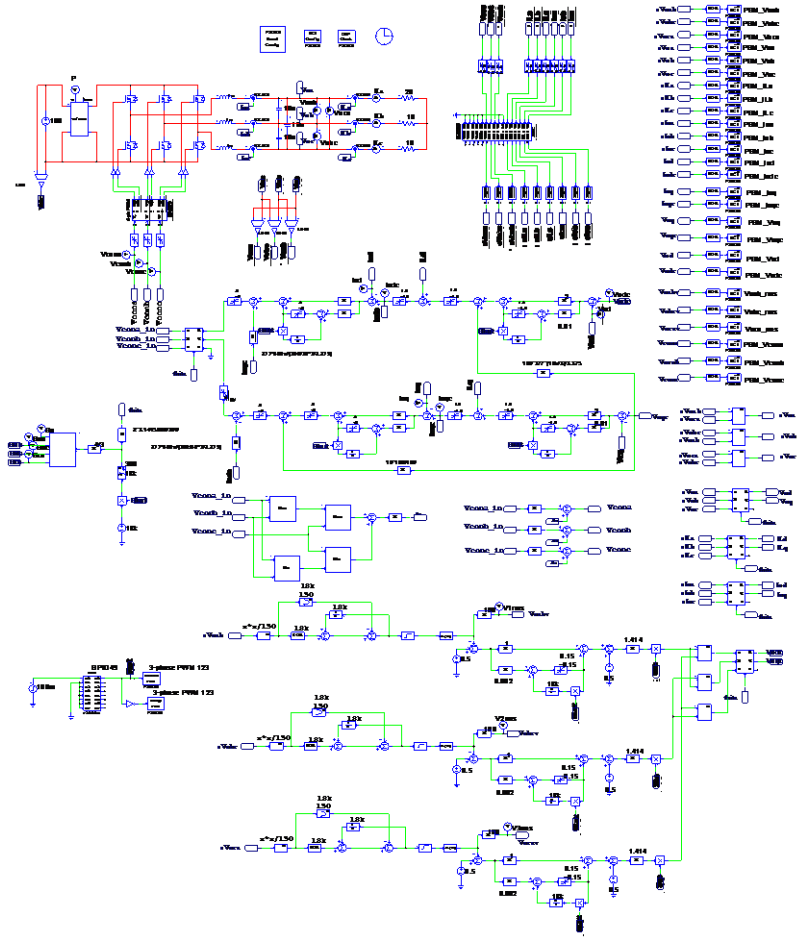


Figure 2.15 The out-of-balance load simulating circuit of three-phase inverter stand-alone built by SimCoder

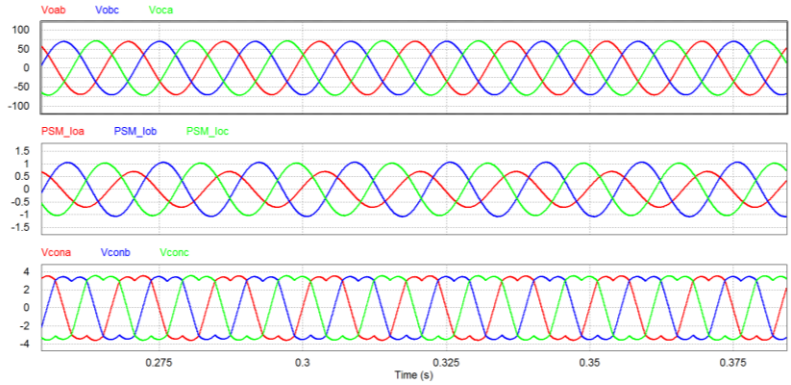


Figure 2.16 The simulating result of voltage output, current output and V_{con} under out-of-balance load

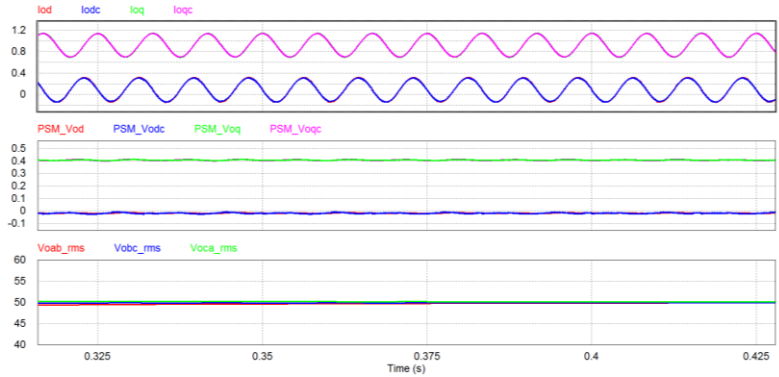


Figure 2.17 The simulating result of D axis and Q axis of RMS value, voltage and current under out-of-balance load

Experiment Devices

The required devices for experiemt are as follows:

PEK-130 * 1

PEK-005A * 1

PEK-006 * 1

PTS 3000 * 1 (with GDS-2204E, PSW160-7.2 and GPL-300A)

PC * 1

Experiment Procedure

The experiment wiring is shown as the figure 2.28. Please follow it to complete wiring.

Figure 2.28 Experiment wiring figure

After wiring, make sure the PEK-130 switch is OFF followed by turning the PEK-005A switch ON. The DSP red indicator lights on as the figure 2.19 shown, which means the DSP power is steadily normal.

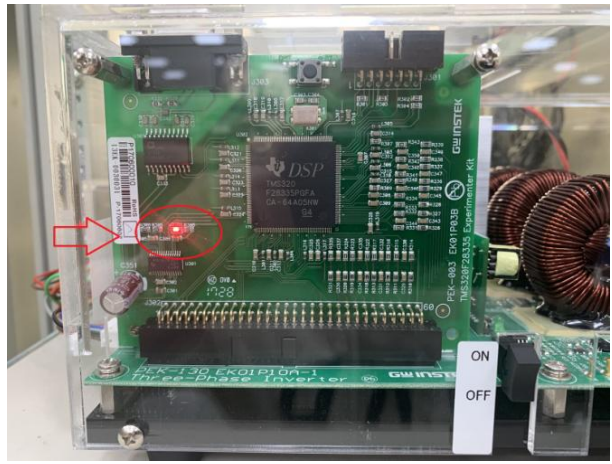


Figure 2.19 DSP normal status with light on

Refer to the appendix B for burning procedure to burn the PEK-130_Lab2_V11.0.3 program into DSP followed by referring to the appendix C for RS232 connection to proceed to connection.

Connect the test leads of oscilloscope to Vo-AB, Vo-BC and Vo-CA, respectively, as the figure 2.20 shown.

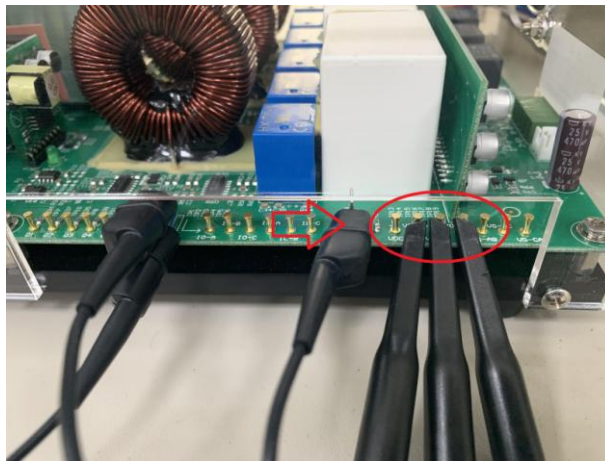


Figure 2.20 Oscilloscope test leads wiring

Set voltage 100V and current 3A for PSW 160-7.2. After powering on GPL-300A, set Resistance Load for Three Phase Load and set OFF for 1TS and 2TS, further setting ON for 3TS. The no load occurs then as the figure 2.21 shown.

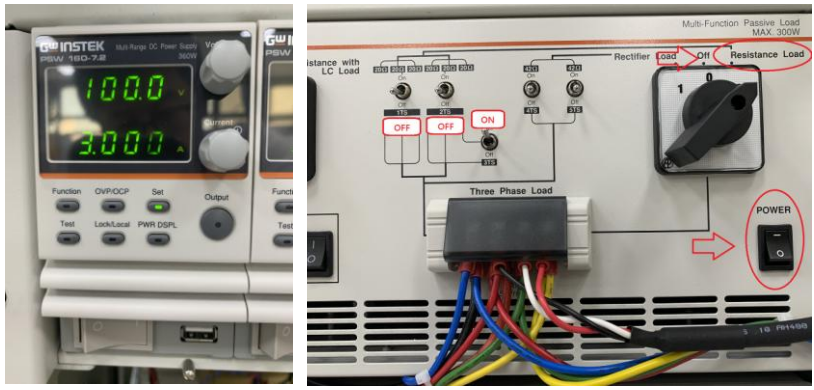


Figure 2.21 The settings of PSW 160-7.2 & GPL-300A

After setting up and PSW power output, turn on the switch of PEK-130.

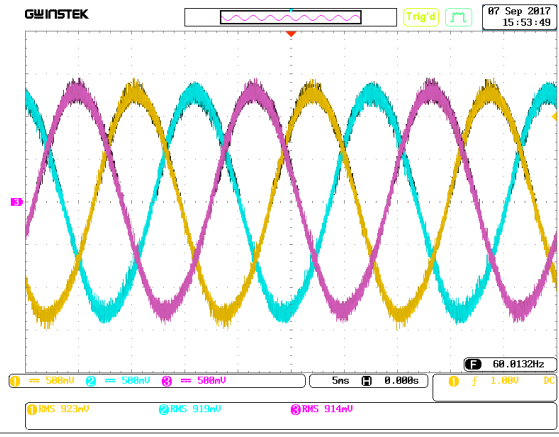
Experiment Result

(1) Three phase inverter stand-alone linear balanced load

The figure 2.22 indicates the voltage waveform when no load

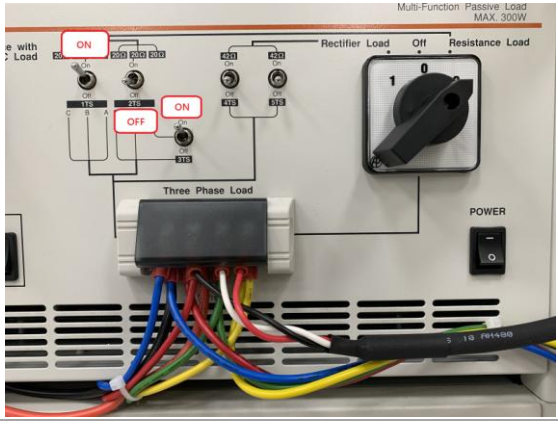
Figure 2.22

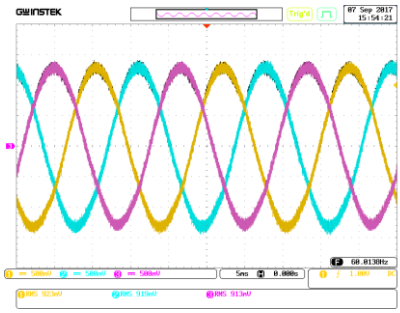
The voltage waveform when no load



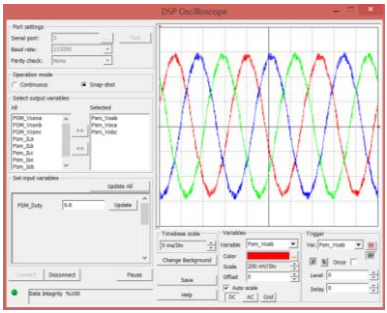
From the above no load test, when load-on outout for measurement, the set output of PSW 160-7.2 remains unchanged. Sets the 1TS and 3TS of GPL-300A on and it turns out half load as the figure 2.23 shown. The figure 2.24(a) indicates the voltage waveform observed from Test Pin V_O-AB, V_O-BC and V_O-CA when half load. The figure 2.24(b) represents the result of RS232 sending back to PC when half load.

Figure 2.23
GPL-300A half load setting





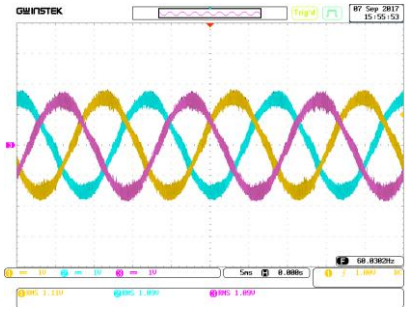
(a)

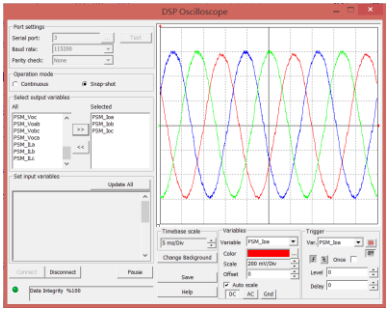


(b)

Figure 2.24 (a) The voltage waveform when half load (b) The result of RS232 sending back to PC

When measuring output current, place test leads on Test Pin I_O-A, I_O-B and I_O-C. The figure 2.25 (a) indicates the current waveform when half load. The figure 2.25 (b) indicates the result of RS232 sending back to PC when half load.





(a) (b)

Figure 2.25 (a) The output current waveform when half load (b) The result of RS232 sending back to PC

It is feasible to observe live-time control signal via DSP oscilloscope of PSIM. The figure 2.26 indicates the dq axis voltage command and tracking of control loop. The figure 2.27 indicates the dq axis current tracking of control loop. The figure 2.28 indicates the three-phase control command. The figure 2.29 indicates the three-phase line voltage RMS value.

Figure 2.26

dq axis voltage tracking

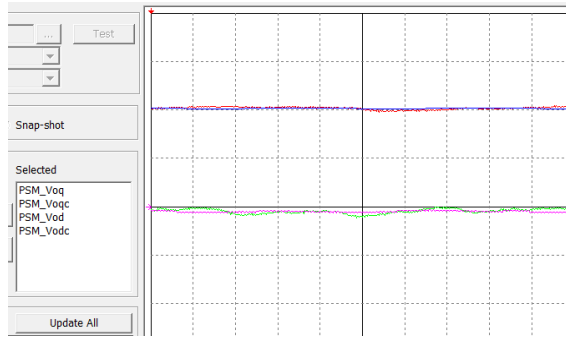


Figure 2.27

dq axis current tracking

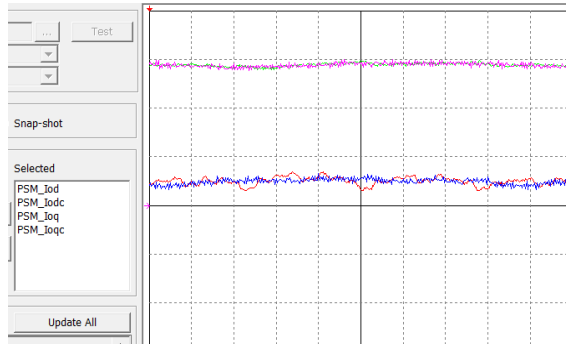


Figure 2.28
Three-phase switch control command

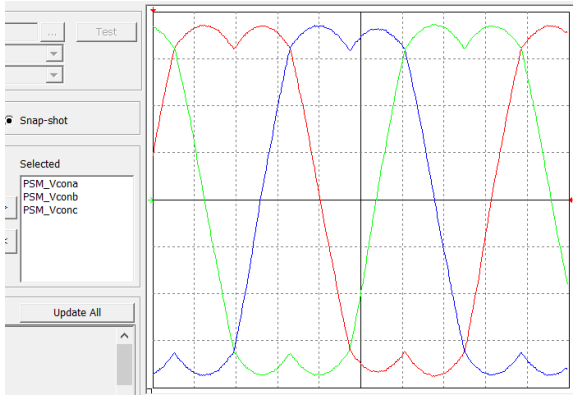
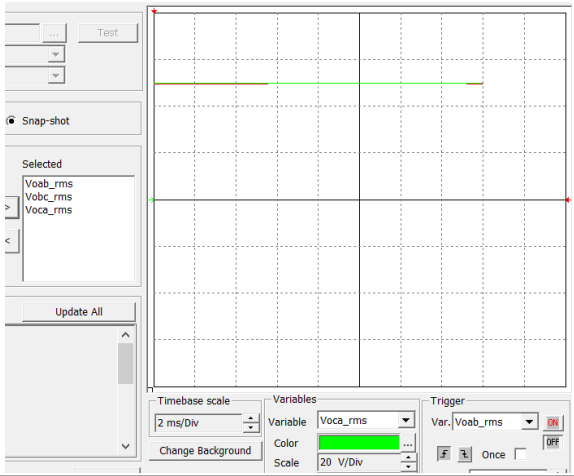


Figure 2.29
Three-phase line voltage RMS value (20V/div)



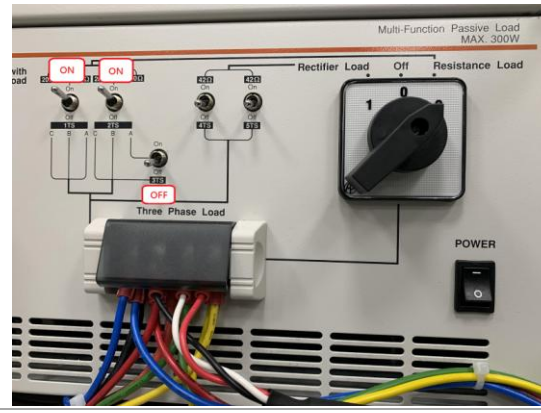
After the experiment, turn off PEK-130 by pressing the power button.

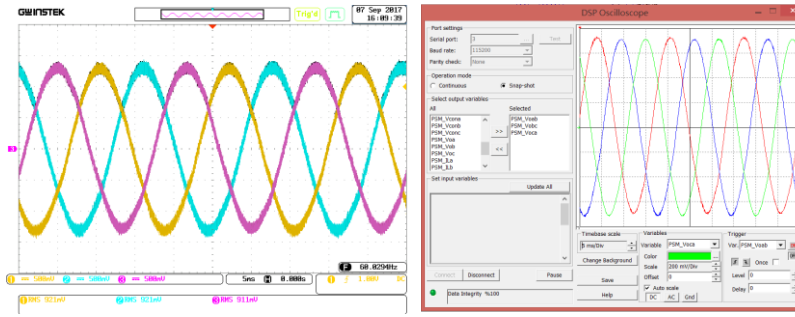
(2) Three-phase inverter stand-alone linear out-of-balance load

Following the previous experiment, when measuring out-of-balance load output, adjust the GPL-300A load to, as the figure 2.30 shown, out-of-balance load ($R_a/R_b/R_c$ = 20/10/10 ohm) followed by turning on the PEK-130 power button and placing test leads on Test Pin V_O-AB, V_O-BC, V_O-CA. The figure 2.31(a) indicates the voltage waveform observed from Test Pin V_O-AB, V_O-BC, V_O-CA

when it is out-of-balance load. The figure 2.31(b) indicates the result of RS232 sending back to the PC side.

Figure 2.30 GPL-300A out-of-balance load setting

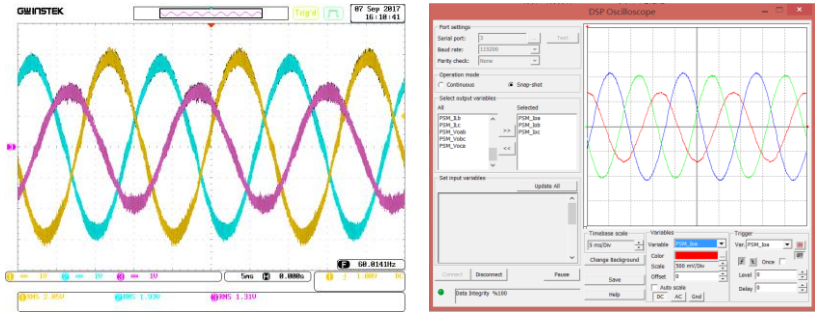




(a) (b)

Figure 2.31 (a) Voltage output waveform of out-of-balance load (b) Result of RS232 sending back to PC side

When testing output current, place test leads on Test Pin I_O-A, I_O-B, I_O-C. The figure 2.32(a) indicates the current output waveform of out-of-balance load. The figure 2.32(b) indicates the result of RS232 sending back to PC side.



(a) (b)

Figure 2.32 (a) Current output waveform of out-of-balance load (b) Result of RS232 sending back to PC side

It is feasible to observe live-time control signal via DSP oscilloscope of PSIM. The figure 2.33 indicates the dq axis voltage command and tracking of control loop. The figure 2.34 indicates the dq axis current tracking of control loop. The figure 2.35 indicates the three-phase line voltage RMS value. The figure 2.36 indicates the three-phase control command.

Figure 2.33

dq axis voltage tracking when out-of-balance load

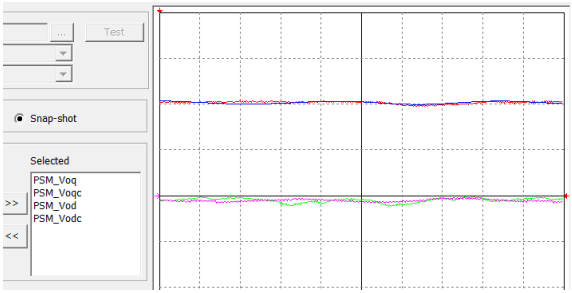


Figure 2.34

dq axis current tracking when out-of-balance load

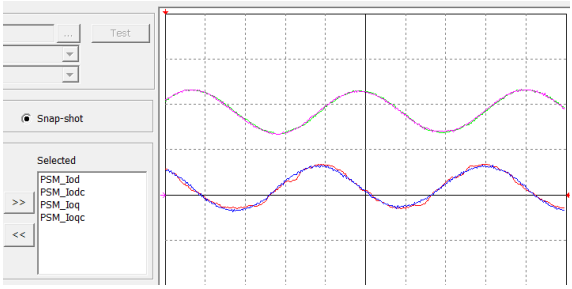


Figure 2.35

Three-phase line voltage RMS value (20V/div)

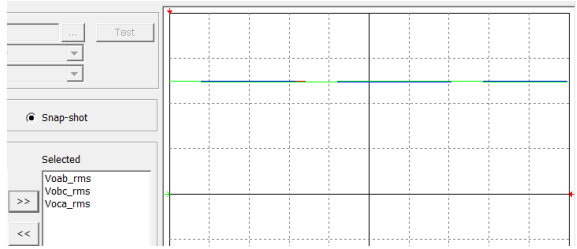
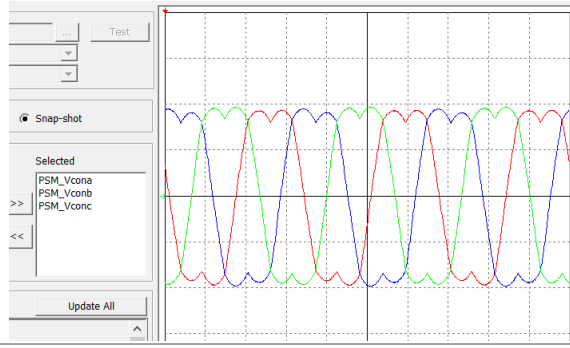


Figure 2.36

Three-phase switch control command



After experiment, turn off the power button of PEK-130 followed by turning off both PSW 160-7.2 and lastly GPL-300A.

Experiment 3 – Three Phase Grid-Connected Inverter

The purpose of experiment

Learns the principle of three-phase grid-connected, the method of phase-lock loop, the controller design of current loop and voltage loop, the hardware layout and the SimCoder programming, etc.

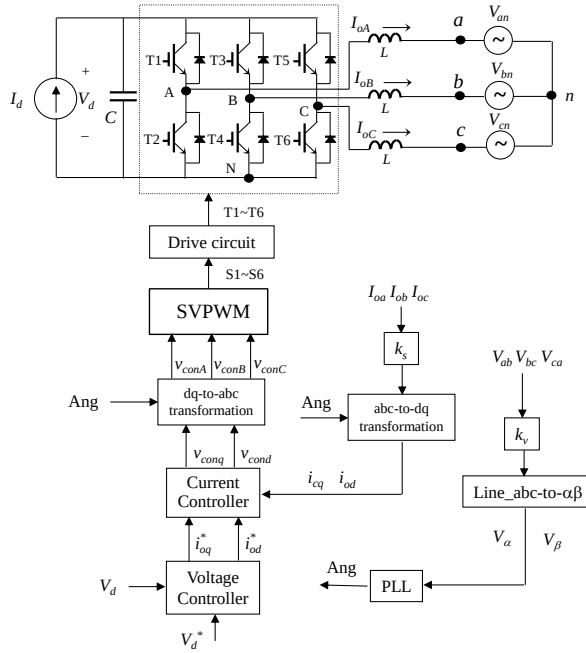
The principle of experiment

3.1 Introduction

The three-phase grid-connected inverter is the necessity required by several renewable energy power systems, energy storage systems and grid interface. The system may cover multi-layer circuit. The experiment emphasizes the control of grid-connected inverter; therefore, the circuit architecture is simplified to the portion of inverter shown in the figure 3.1 where the input current I_d is used to indicate current generated by the previous layer circuit. The inverter is designed by dual loop in which outer loop is DC voltage control loop, whereas inner loop is inductive current control loop. In addition, the current of grid-connected inverter needs to subchronize with grid-connected voltage. Hence, an additional phase-lock loop (PLL) control is needed.

Figure 3.1

The control architecture of three-phase grid-connected inverter



3.2 Current loop design

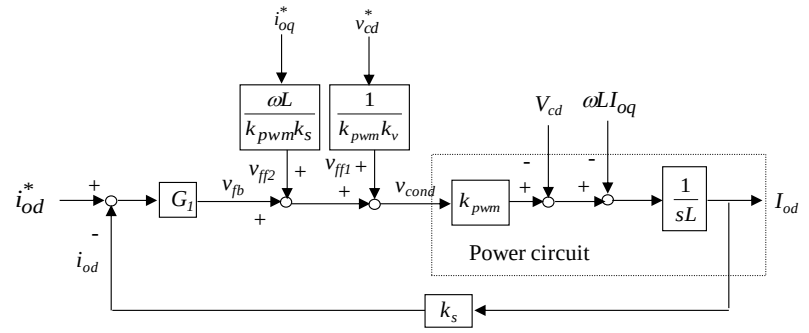
The equivalent circuit model of three-phase grid-connected inverter is identical with the previous Lab2 individual inverter model that can convert circuit to synchronized rotational frame, via *abc-dq* axis conversion, to simplify controller design. The current controller of inverter under *dq* axis is shown as the figure 3.2 in which both currents of *d and q* will cause perturbation on current of the other axis. Therefore, the perturbation is exempted via feedforward control signal v_{ff2} in the figure 3.2. The other feedforward signal v_{ff1}, on the other hand, is used to eliminate the perturbation from the phase output voltage to current loop. k_v and k_s are the sensing gain of voltage and current, respectively. The current error amplifier G_I can be designed by *P* and *PI* or the secondary error amplifier; when adopting P control (G_I=k_1), current loop response can be acquired as follows via current feedback loop:

$$\frac{i_{o,i}^*}{i_{o,i}} = \frac{\frac{k_{pwm}k_s k_1}{L}}{s + \frac{k_{pwm}k_s k_1}{L}} = \frac{u_I}{s + u_I} \quad ,i = d, q \tag{3.1}$$

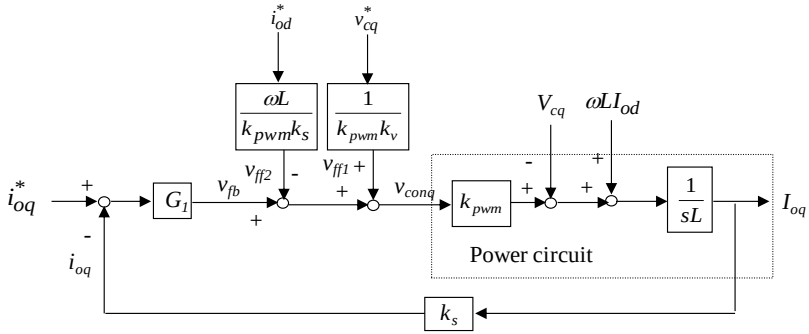
The u_I here indicates bandwidth of current loop:

$$u_I = \frac{k_{pwm}k_s k_1}{L} \tag{3.2}$$

It can be designed by the gain k_1 of current error amplifier.



(a)



(b)

Figure 3.2 Current control loop of inverter: (a) d axis, (b) q axis

3.3 Voltage loop design

The purpose of DC voltage control is to maintain power balance; that is, the power from the previous circuit can be leveraged with the power of inverter infusing into grid-connected electricity. Consequently, after eliminating the DC working point of steady state, the circuit model of equivalently small signal of voltage loop can be shown as the figure 3.3 (a); that is, the inverter can be regarded as small signal value of a current source I_d charging to DC capacitance.

Transient power of AC side can be shown as the following:

$$P_{ac} = V_\alpha I_\alpha + V_\beta I_\beta = V_{s(p)} \sin \omega t \cdot Im \sin \omega t + V_{s(p)} \cos \omega t \cdot Im \cos \omega t \quad (3.3)$$

Where $V_{s(p)}$ is the peak voltage of dq axis, and I_m is the peak current of dq axis. The equation above can be, via trigonometric function, simplified to the follows:

$$P_{ac} = V_{s(p)} I_m \quad (3.4)$$

The figure 3.3 (b) indicates that the current source responses to the DC side; when inverter performs at 100% efficiency, the input power P_a is equal to the output power P_{dc}:

$$P_{dc} = P_{ac} \quad (3.5)$$

Also, the power of DC side can be shown as follows:

$$P_{dc} = V_d I_d \quad (3.6)$$

Therefore

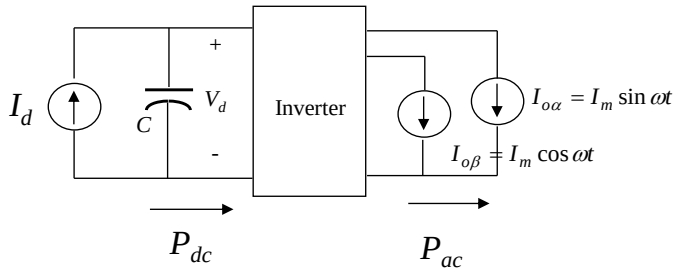
$$V_d I_d = V_{s(p)} I_m \quad (3.7)$$

$$I_d = \frac{V_{s(p)} I_m}{V_d} = K_{dc} I_m \quad (3.8)$$

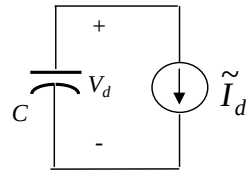
$$\tilde{V}_d = \tilde{I}_d \frac{1}{sC} \quad (3.9)$$

From the figure 3.3 (b), the transfer function of DC current to DC voltage can be shown as the following:

$$\frac{\tilde{V}_d}{\tilde{I}_m} = \frac{K_{dc}}{sC}, \quad K_{dc} = \frac{V_{s(p)}}{V_d} \quad (3.10)$$



(a)



(b)

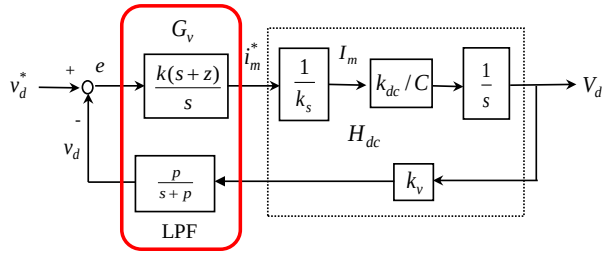
Figure 3.3 Voltage loop: (a) dq axis equivalent circuit, (b) converted to DC side equivalent circuit

DC voltage loop controller design

Based on (3.8), refer to the figure 3.4 for the control block diagram of designing DC voltage in which k_v and k_s are the sensing gain of voltage and current individually. The (3.11) below can be acquired by merging sensing gain with (3.10):

$$H_{dc}(s) = \frac{k_v k_{dc}}{k_s C s} \tag{3.11}$$

Figure 3.4 Voltage loop control block diagram

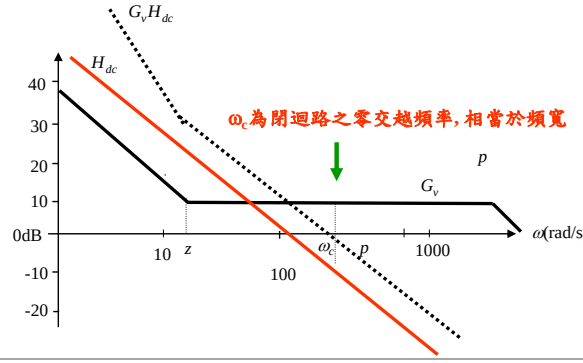


Voltage controller can be designed based on the loop gain of figure 3.4. Due to the fact that three-phase inverter DC voltage has no low-frequency ripple and there is no need to use low-pass filter to attenuate low-frequency ripple of voltage 120Hz or 360Hz to reduce distortion of current command, the controller thus use proportional integral controller and the transfer function of controller is as follows:

$$G_v = \frac{k(s+z)}{s} \tag{3.12}$$

The frequency response of (3.11) and (3.12) is shown as the figure 3.5. ω_c indicating the bandwidth of zero crossing frequency of system. The selection for zero point G_v requires the slope of zero crossing frequency ω_c under rated load of $G_v H_{dc}$ as -20*db/ decade*. Based on the previous condition, zero point z and proportional gain constant k are abel to be designed.

Figure 3.5 Frequency response of voltage loop



3.4 Phase-lock Loop Design

The figure 5.6 indicates the architecture of inverter phase-lock loop which utilizes grid-connected voltage (V_{sa}, $V_{sb\ and}$ V_{sc}) followed by *abc*-$\alpha\beta$ axis conversion to acquire the 2 signals $V_m sin(\omega t)$ and -$V_m cos(\omega t)$. The 2 signals will be multiplied by the latter synchronized signals $cos(\omega_1 t)$ and $sin(\omega_1 t)$ respectively to obtain the following:

$$e = V_m\{\sin(\omega t)\cos(\omega_1 t) - \cos(\omega t)\sin(\omega_1 t)\} \qquad (3.13)$$

According to (3.13), if ω = ω_1, (3.13) will be equal to zero. Hence, it is viable to make use of this condition to design phase-lock loop controller. The signal e , after passing through a proportional integral, obtains a frequency correction signal Δω followed by adding the orginal set frequency ω_o(=377) to acquire a frequency ω_1, which will obtain, after passing through integer, an angle singal θ. The θ will pass through an interval limiter between 0~2π followed by checking the Sine table and Cosine table to acquire $cos(\omega_1 t)$ and $sin(\omega_1 t)$ signals. The error e can be adjusted to zero via proportional integral to achieve phase-lock; that is, ω = ω_1.

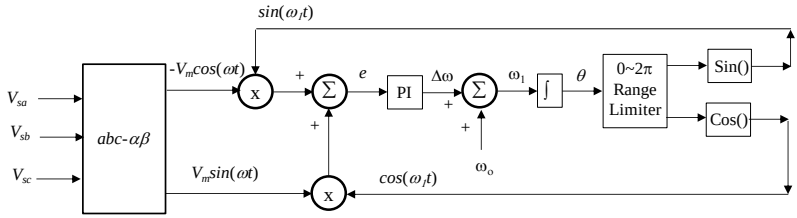


Figure 3.6 Phase-lock loop

3.5 System Simulating Verification

This experiment utilizes the following 250W inverter to validate the previously discussed control methods.

DC Voltage V_d = 100V
AC Voltage V_{LL} = 50V_{rms}
F_s = 18kHz, V_{tri} = 10V_{pp} (PWM Triangular Waveform Amplitude)
C_d = 330uF (DC-Link Capacitor)
L = 1mH
C = 10uF
K_s = 0.3 (current sensing factor)
K_v = 0.01 (AC voltage sensing factor)
K_v = 0.02 (DC voltage sensing factor)

The Matlab program of control loop design is as follows:

```
% Three-phase Stand-alone Inverter
clear;
clc;
PI=3.1416;
Vd=100;
VLL=50;
Vs = 50/1.732;
Vsp = 1.5 * Vs * 1.414;
L=0.6e-3;
C=660e-6;
vtm=5;
kpwm=(Vd/2)/vtm
ks= 1/3.375
kv=1/100
kdc = Vsp/Vd;
fs=18e3;
```

```
% Voltage Loop Design
% Gv = k3(s+z)/s
% LPF = p/s+p
uv = 2 * PI * 20
z = 30
p = 7.23e3 * 2 * PI
tuv = 1/z
numHdc = kv*kdc/(ks*C);
denHdc=[1 0];
Hdc=tf(numHdc,denHdc);
Hdcr = freqresp(Hdc, uv);
Gc = 1/abs(Hdcr);
numGv1= [1 z];
denGv= [1 p 0];
Gv1 = tf(numGv1, denGv);
Gv1r = freqresp(Gv1, uv);
K3r = 1 /(abs(Hdcr) * abs(Gv1r));
K3 = K3r/p
numGv = K3r * numGv1;
Gv = tf(numGv, denGv);
GvHdc = series(Gv, Hdc);
bode(Hdc,Gv,GvHdc);
grid;
```

The calculating results are as follows=>

```
ks =  0.2963
kv =  0.0100
uv =  125.6640
z =   30
p = 4.5428e+004
```

tuv = 0.0333

K3 = 3.9038

The figure 3.7 below shows voltage loop bode plot.

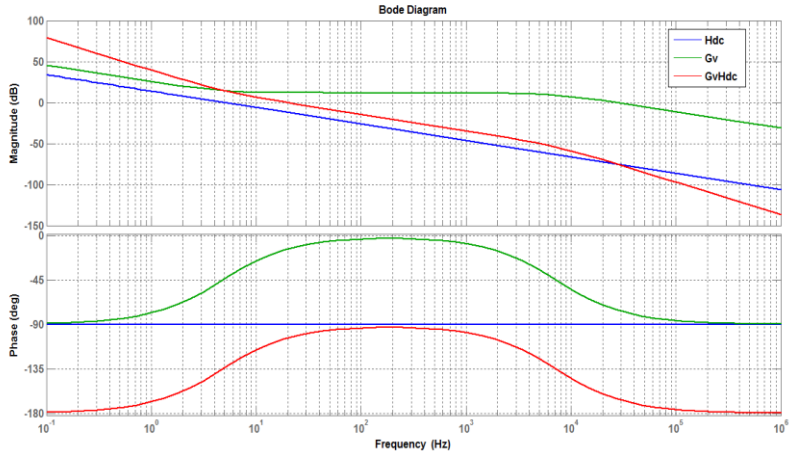


Figure 3.7 Voltage loop bode plot

Circuit Simulation

Inverter Specification

- DC Voltage V_d = 100V
- AC Voltage V_{LL} = 50Vrms 、Frequency 60Hz
- F_s = 18kHz，V_{tri} = 10V_{pp} (PWM)，C_d = 330uF，L = 1mH，C = 10uF
- K_s = 0.3 (current sensing factor)，
- K_v = 0.01 (AC voltage sensing factor)
- K_v = 0.02 (DC voltage sensing factor)

PSIM Simulation

The simulating circuit built by the previous parameters is shown as the figure 3.8. The simulating result is shown as the figure 3.9.

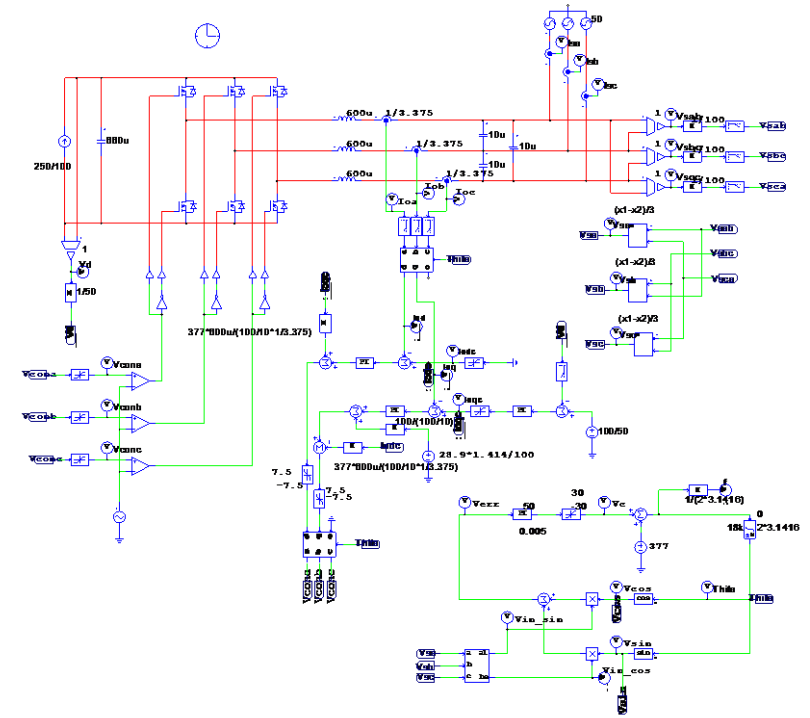


Figure 3.8 Three-phase grid-connected simulating circuit

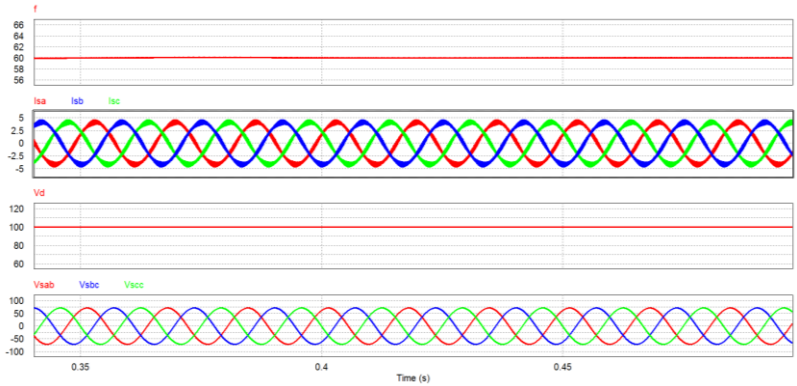


Figure 3.9 Simulating result of three-phase grid-connected electricity

SimCoder Program Layout & Circuit Simulation

The figure 3.10 indicates the simulating circuit of three-phase grid-connected inverter built by SimCoder. The figure 3.11 shows the simulating result.

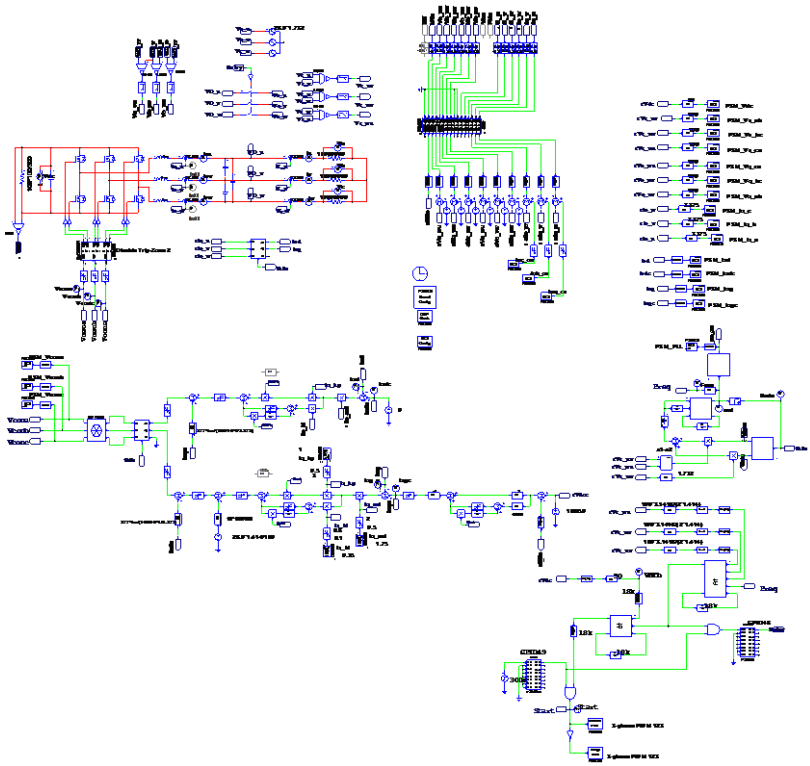


Figure 3.10 Simulating circuit of three-phase grid-connected inverter built by SimCoder

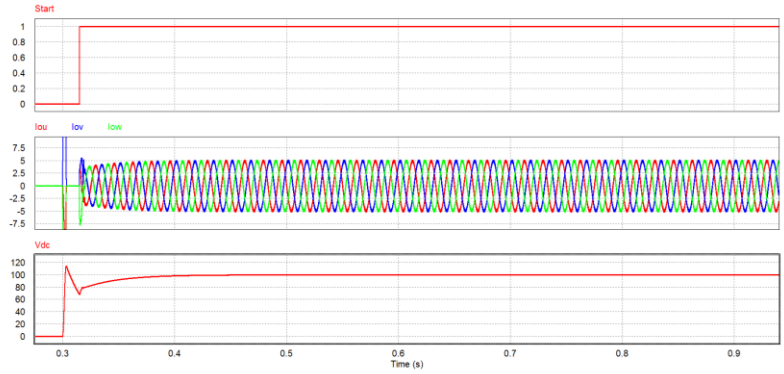


Figure 3.11 Simulating result of three-phase grid-connected inverter built by SimCoder

Experiment Devices

The required devices for experiemt are as follows:

PEK-130 * 1

PEK-005A * 1

PEK-006 * 1

PTS-3000 * 1 (with GDS-2204E, PSW160-7.2 and APS-300, GPL-300A)

PC * 1

Experiment Procedure

The experiment wiring is shown as the figure 3.12. Please follow it to complete wiring.

Figure 3.12 Experiment wiring figure

After wiring, make sure the PEK-130 switch is OFF followed by turning the PEK-005A switch ON. The DSP red indicator lights on as the figure 3.13 shown, which means the DSP power is steadily normal.

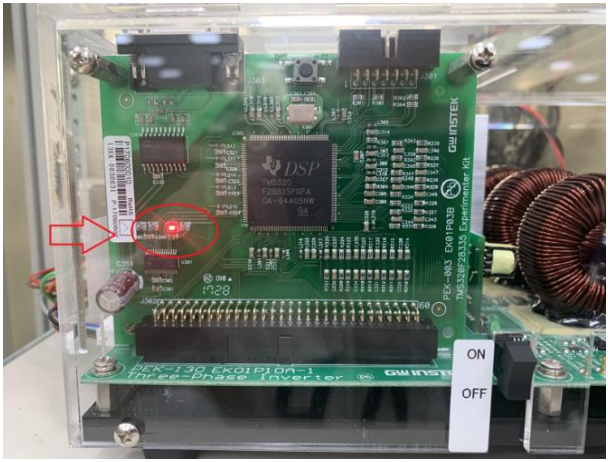


Figure 3.13 DSP normal status with light on

Refer to the appendix B for burning procedure to burn the PEK-130_Lab3_V11.0.3 program into DSP followed by referring to the appendix C for RS232 connection to proceed to connection.

Connect the test leads of oscilloscope to Vo-AB, Vo-BC and Vo-CA, respectively, as the figure 3.14 shown.

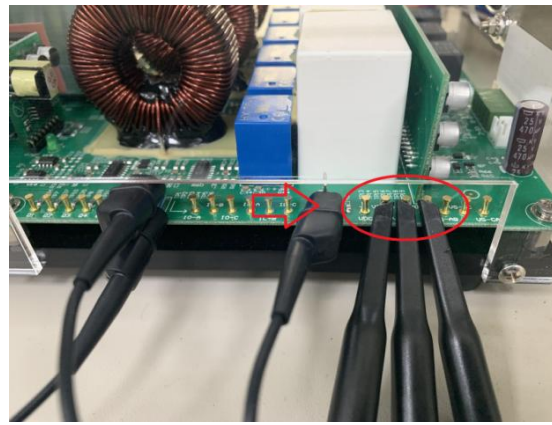


Figure 3.14 Oscilloscope test leads wiring

Set voltage 110V and current 1A for PSW 160-7.2. After powering on GPL-300A, set Resistance Load for Three Phase Load and set OFF for 1TS and 2TS, further setting ON for 3TS. The no load occurs then as the figure 3.15 shown.

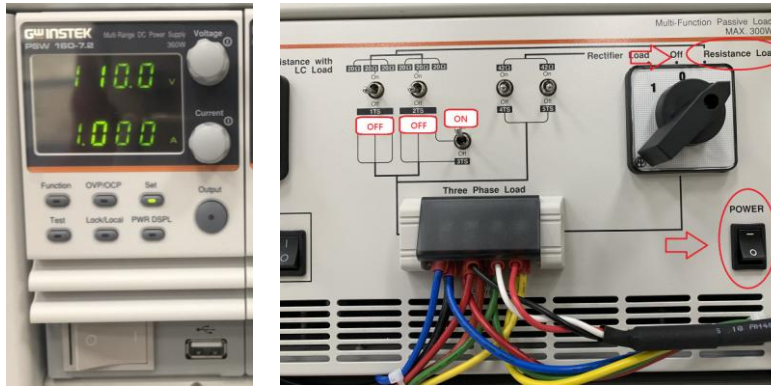


Figure 3.15 The settings of PSW 160-7.2 & GPL-300A

After powering on APS-300, set 60Hz for frequency and 3P4W for mode and 28.86V for output voltage as the figure 3.16 shown.

Figure 3.16 The settings of APS-300

After setting up and PSW with APS-300 power output, turn on the switch of PEK-130.

Experiment Result

(1) No Load

The measurement waveform of three phase voltage output (Vo-AB, Vo-BC, Vo-CA) is shown as the following figure 3.17. On the condition of no load and 100W output power from PSW, APS-300 absorbs all the power due to no load. It has seen that APS power is single phase -30.5W (minus "-" indicates power absorbing) and the three phase total power is -30.5W*3= -91.5W, which is equivalent to the PSW output power with considering the wear and tear of components as the figure 3.18 shown.

Figure 3.17
Measurment waveform of Vo-AB, Vo-BC and Vo-CA

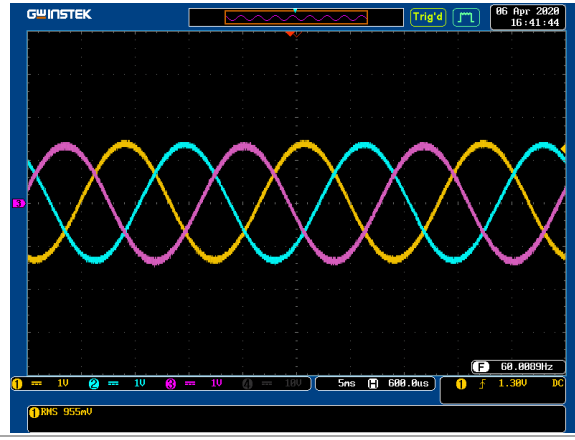


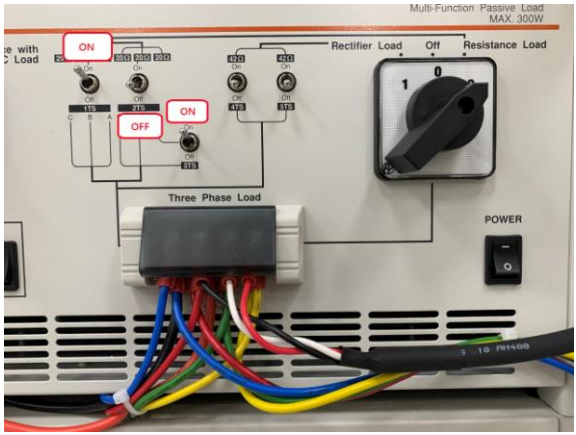
Figure 3.18 Power state of PSW and APS-300 when no load

(2) Half Load (20 Ohm)

Sets 1TS and 3TS ON and 2TS OFF as the figure 3.19 shown when half load.

Figure 3.19

The half load setting of GPL-300A



On the condition of half load (125W) and 100W output power from PSW, APS-300 needs to provides 25W for maintaining power balance of system because PSW output power can not afford to the load demand.It has seen that APS power is single phase 11.2W and the three phase total power is 11.2W*3= 33.6 with considering the wear and tear of components as the figure 3.20 shown.

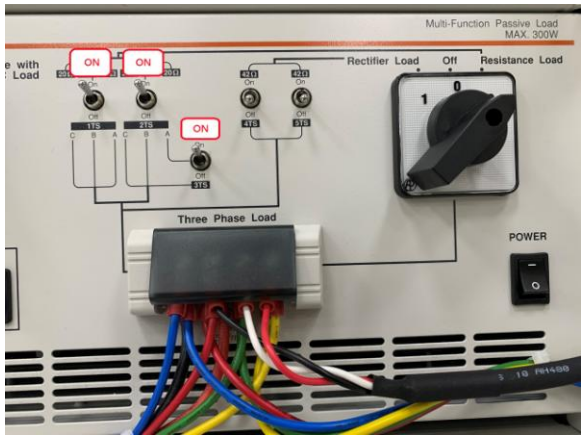
Figure 3.20 Power state of PSW and APS-300 when half load

(3) Full Load (10 Ohm)

Sets 1TS, 2TS and 3TS ON as the figure 3.21 shown when full load.

Figure 3.21

The full load setting of GPL-300A



On the condition of full load (250W) and 100W output power from PSW, APS-300 needs to provides 150W for maintaining power balance of system due to more demands for power from load.It has seen that APS power is single phase 51.6W and the three phase total power is 51.6W*3= 154.8W with considering the wear and tear of components as the figure 3.22 shown.

Figure 3.22 Power state of PSW and APS-300 when full load

After experiment, turn off the power button of PEK-130 followed by turning off both PSW and lastly GPL-300A.

Experiment 4 – Single Phase Three Arms Rectified Inverter

The purpose of experiment

Owning to the equipped three arms, it can also be used for single-phase on-line UPS. This experiment will walk you through the work mode of UPS, the design of current loop and voltage loop controller of both rectifier and inverter, the hardware layout and SimCoder programming, etc.

The principle of experiment

4.1 Circuit Architecture

In addition to the benefits of saving DC capacitance and reducing cost, the COM-arm current of three arms rectified inverter circuit, as shown in the figure 4.1, is the deviation between input current and load current; it needs, on the condition of PFC, the virtual work of charging load, harmonic current and small portion of actual work that compensates loss from inverter. Besides, the conduction loss is way lower than that of the conventional one.

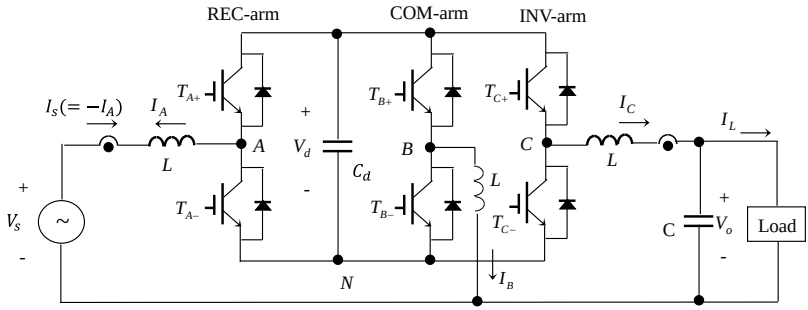


Figure 4.1 Circuit architecture of single-phase three arms rectified inverter

4.2 Circuit Model

From the three arms rectified inverter circuit within the figure 4.1 we can acquire as follows:

$$L\frac{dI_A}{dt} = V_{AN} - V_{BN} - V_S \tag{4.1}$$

$$L\frac{dI_C}{dt} = V_{CN} - V_{BN} - V_O \tag{4.2}$$

$$C\frac{dV_O}{dt} = I_C - I_L \tag{4.3}$$

Each arm adopts PWM switch; control voltages (v_{conA}、v_{conB}、v_{conC}) compare with triangular waveform individually to further trigger switch of three arms, and the output voltage of each arm within (4.1) and (4.2) can be stated as the following:

$$V_{iN} = (\frac{1}{2} + \frac{v_{coni}}{2v_{tm}})Vd \ (i=A, B, C) \tag{4.4}$$

Where v_{tm} is the amplitude of PWM triangular waveform, and we can acquire the following by substituting (4.4) into (4.1) and (4.2):

$$L\frac{dI_A}{dt} = \frac{V_d}{2v_{tm}}v_{conA} - \frac{V_d}{2v_{tm}}v_{conB} - V_s \tag{4.5}$$

$$L\frac{dI_C}{dt} = \frac{V_d}{2v_{tm}}v_{conC} - \frac{V_d}{2v_{tm}}v_{conB} - V_O \tag{4.6}$$

Therefore

$$k_{pwm} = \frac{V_d}{2v_{tm}} \tag{4.7}$$

(4.5) and (4.6) can be restated as follows:

$$L\frac{dI_A}{dt} = k_{pwm}v_{conA} - k_{pwm}v_{conB} - V_s \tag{4.8}$$

$$L\frac{dI_C}{dt} = k_{pwm}v_{conC} - k_{pwm}v_{conB} - V_O \tag{4.9}$$

(4.8) and (4.9) illustrate that the outputs of both rectified arm and inverted arm will be influenced by the common arm; if you want to be free from the interaction effect between the switch of 2 arms, it

requires to decouple (4.8) and (4.9). The simplest method to decouple is to set the control voltage of middle arm as follows:

$$v_{conB} = -\frac{v_o}{2k_{pwm}} \tag{4.10}$$

Therefore, (4.8) and (4.9) can be restated as the following:

$$\mathrm{L}\frac{dI_A}{dt} = \mathrm{k_{pwm}}v_{conA} + \frac{v_o}{2} - V_s \tag{4.11}$$

$$\mathrm{L}\frac{dI_\mathrm{C}}{dt} = \mathrm{k_{pwm}}v_{con\mathrm{C}} - \frac{\mathrm{v_o}}{2} \tag{4.12}$$

4.3 Design of Inverter Controller

The design of current loop controller can be based on the previously inferred circuit model (4.11). The PWM control voltage of actual middle arm is generated, based on (4.10), by the load voltage command (v_{oc}).

$$v_{conB} = -\frac{v_{oc}}{2k_v k_{pwm}} \tag{4.13}$$

Where k_v and k_s are voltage and current sensing proportions respectively. The figure 4.2 refers to the control block diagram of inverter current loop where electric circuit is drawn in accord with (4.11) and ks indicates the current sensing proportion. The current control loop utilizes both feedforward and feedback controls; the feedforward signal v_{ffR} utilizes the normal value (v_{sc}) of input voltage and the load voltage command (v_{oc}), which is set by v_{conB}, to eliminate the perturbation of V_s and $V_o/2$ directly so that current feedback controller k_1 utilizes only a single proportional control. The command response of input current tracking can be inferred, based on the figure 4.2, as follows:

$$\frac{i_A}{i^*_\mathrm{A}} = \frac{\frac{k_{pwm}k_s k_1}{L}}{s + \frac{k_{pwm}k_s k_1}{L}} = \frac{u_{RI}}{s + u_{RI}},\ \mathrm{u_{RI}} = \frac{k_{pwm}k_s k_1}{L} \tag{4.14}$$

Where u_{RI} is equal to bandwidth of current loop, which is designed at the 1/10 of the switch frequency. The input current command i_A* is generated via DC voltage loop, and the deviation of feedback DC voltage (v_d) and DC voltage command (v_{dc}) is adjusted via voltage

controller G_v to obtain a signal of amplitude im, which is multiplied by an unit sinusoid sinωt followed by reverse to obtain a current command (i_{Ac}) of A arm.

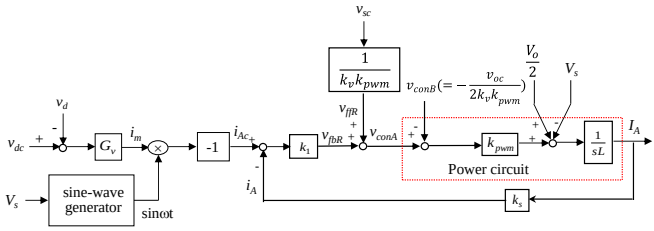


Figure 4.2 The block diagram of inverter current loop control

It is necessary to infer, in accordance with rectifier operating under unit power factor, DC voltage loop model for the design of G_v. Due to the DC link of rectifier providing or undertaking inverter load power and the grid-connected electricity providing or absorbing electricity, the small signal model of DC side can be viewed, in terms of the two-stage circuit integrated by rectifier and inverter, as a DC small signal current (I_d) charging to DC capacitor as the figure 4.3 (a) shown. The input power of AC side is as follows:

$$P_{ac} = V_{s(p)} \sin\omega t \cdot I_m \sin\omega t = \frac{V_{s(p)} I_m}{2} - \frac{V_{s(p)} I_m}{2} \cos 2\omega t \qquad (4.15)$$
$$= \overline{P}_{ac} + \widetilde{P}_{ac2}$$

Where $V_{s(p)}$ an d I_m are input voltage and current peak value respectively. In addition to a DC item, (4.15) includes a second harmonic item, which will cause DC voltage second ripple. The average power of DC side is identical to the DC item of AC side power:

$$\overline{P}_{ac} = P_{dc} \qquad (4.16)$$

The equivalent circuit of figure 4.3 (b) can be acquired through responding AC current source to DC side, and the following is obtained according to (4.16):

$$\frac{V_{s(p)} I_m}{2} = V_d I_d \qquad (4.17)$$

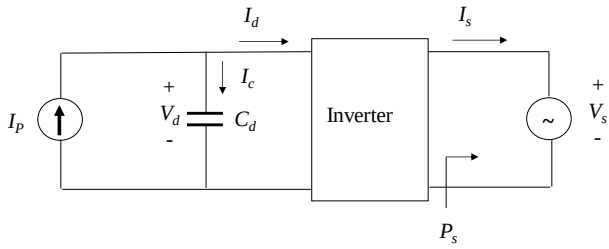
$$I_d = \frac{V_{s(p)} I_m}{2V_d} = k_{dc} I_m \qquad (4.18)$$

The voltage loop model can be acquired as follows by DC current source I_d charging to capacitor C_d:

$$\frac{V_d}{I_m} = \frac{k_{dc}}{sC_d},\ k_{dc} = \frac{V_{s(p)}}{2V_d} \tag{4.19}$$

The block diagram, as the figure 4.4(a) shown, of rectifier DC voltage control loop is acquired based on (4.19). The voltage controller G_v is designed by the figure 4.4(a) where due to current loop bandwidth is way wider than voltage loop bandwidth, the current loop response of (4.14) can be simplified to be equal to 1. Hence, the gain of current amplitude I_m of i_m to actual I_A is reciprocal of current sensing proportion k_s, and the bode plot of voltage loop H_{dc} is displayed as the figure 4.4(b). Considering that DC voltage comes with second ripple, in order to reduce distortion of grid-connected current command, bandwidth of voltage loop must be lower than 120Hz to attenuate second ripple of voltage. Therefore, the bode plot of design of G_v utilizing type II compensator (PI + Low-Pass) is displayed as the figure 4.4(b) where the zero crossing frequency of loop response G_vH_{dc} is generally placed in 20Hz(125.6rad/s).

(a)



(b)

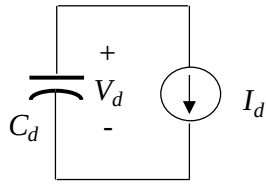
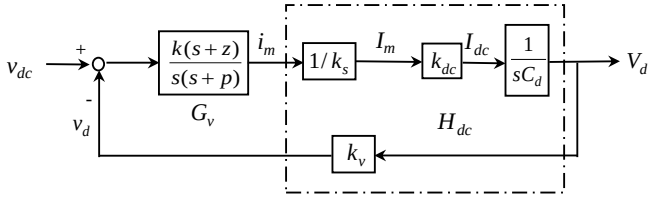


Figure 4.3 Rectifier under unit power factor (a) equivalent circuit (b) small signal equivalent circuit of AC side

(a)



(b)

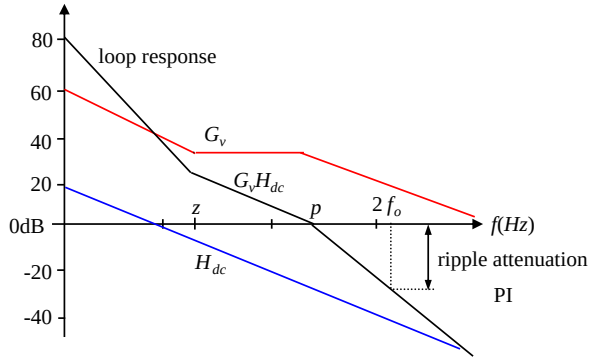


Figure 4.4 Rectifier DC voltage control loop: (a) block diagram (b) bode plot

4.4 Inverter Controller Design

The block diagram of current loop control of inverter is shown as the figure 4.5(a) in which electric circuit is drawn based on (4.12). The current control loop, similarly, utilizes both feedforward and feedback controls; feedforward control utilizes output voltage command (v_o*/2) to eliminate perturbation of V_o/2 directly so that current feedback controller k_1 can use a proportional control only. Input current tracking the command response can be inferred from the figure 4.5(a) as the following:

$$\frac{i_C}{i^*_C} = \frac{\frac{k_{pwm}k_s k_1}{L}}{s + \frac{k_{pwm}k_s k_1}{L}} = \frac{u_{II}}{s + u_{II}}, u_{II} = \frac{k_{pwm}k_s k_1}{L} \qquad (4.20)$$

Where u_{II} is equal to bandwidth of current loop, which is designed at the 1/10 of switch frequency.

Inverter current command i_C* is generated by voltage control loop, and the voltage loop control block diagram is displayed as the figure 4.5 (b) in which electric circuit is drawn based on (4.12). The deviation of feedback output voltage (v_o) and voltage command (v_o*) is adjusted by voltage controller G_{vI} followed by obtaining a signal v_{fi}, which plus a feedforward control signal acquires the ultimate current command (i_C*). Feedforward control signal iL is used to offset the perturbation caused by load current (I_L) to voltage tracking response. The voltage command (v_o*) is generated by an amplitude signal (v_m) multiplied by unit sinusoid sinωt. In order to have output voltage equipped with excellent voltage regulation rate of RMS value, the amplitude signal (vm) is acquired via the deviation of feedback signal (v_{rms}) of voltage RMS value and RMS value command (v_{rmsc}) passing through a deviation modified signal generated by PI-type deviation amplifier (G_{MI}) followed by adding the amplitude signal ($\sqrt{2}v_{rmsc}$) generated by original RMS value command. By doing so, voltage control loop is equipped with transient voltage control and RMS value voltage adjustment to ensure that output voltage is of low distortion with brilliant voltage regulation rate.

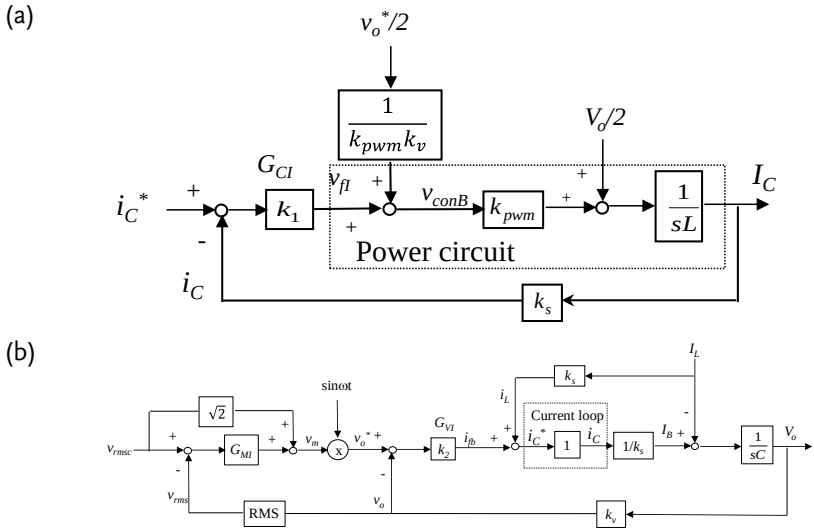


Figure 4.5 Inverter control loop block diagram: (a) current loop (b) voltage loop

Circuit Simulation

Inverter Specification

- Load (3 switchable levels) = 42 /21 /14 ohms
- AC Voltage = 40Vrms，60Hz
- F_s = 18kHz，V_{tri} = 10V_{pp} (PWM)，C_d = 330uF，L = 1mH，C = 10uF
- K_s = 0.3 (current sensing factor)，
- K_v = 0.01 (AC voltage sensing factor)
- K_v = 0.02 (DC voltage sensing factor)

PSIM Simulation

As the figure 4.6 shown, of which the simulating circuit is constructed by the previous parameters, the simulating result under linear load mode is illustrated as the figure 4.7 below:

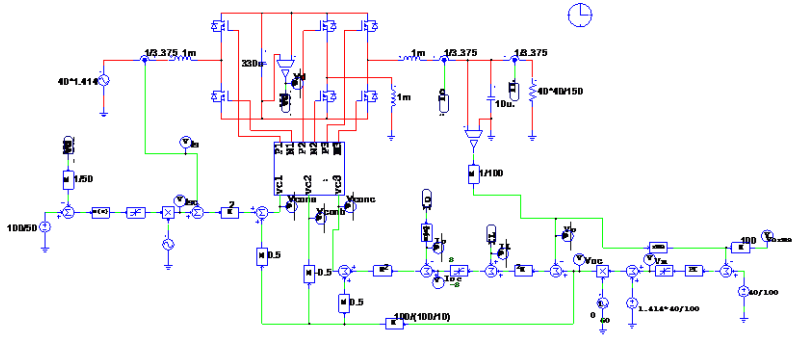


Figure 4.6 Three arms single-phase rectifier – inverter simulating circuit

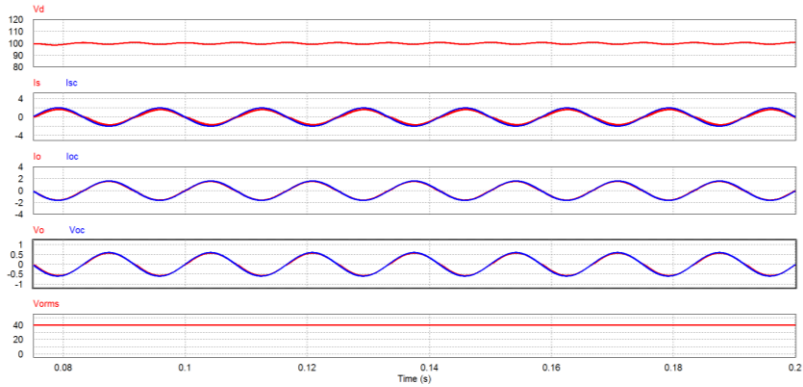


Figure 4.7 Three arms single-phase rectifier – inverter simulating result

SimCoder Program Layout & Circuit Simulation

The three arm single-phase rectifier – inverter simulating circuit built by SimCoder is displayed as the figure 4.8. The simulating result of linear load is shown as the figure 4.9.

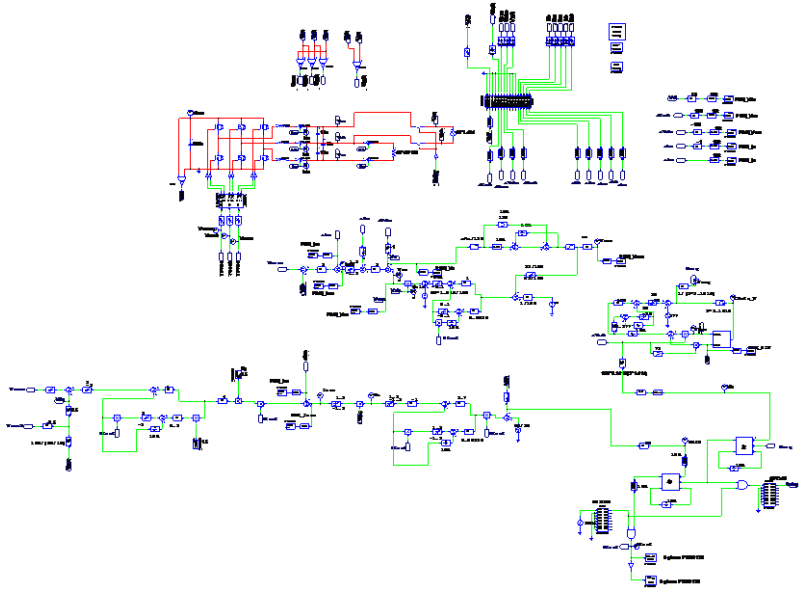


Figure 4.8 Three arms single-phase rectifier – inverter simulating circuit

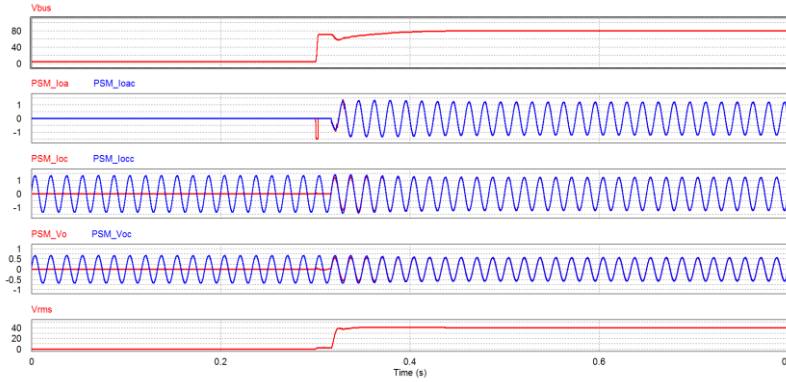


Figure 4.9 Simulating result of three-arms single-phase rectifier – inverter built by SimCoder

Experiment Devices

The required devices for experiemt are as follows:

PEK-130 * 1

PEK-005A * 1

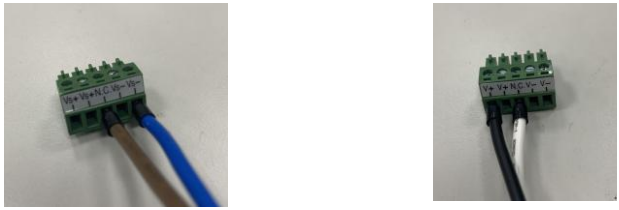
PEK-006 * 1

PTS 3000 * 1 (with GDS-2204E, APS-300 and GPL-300A)

PC * 1

Experiment Procedure

Due to the fact that the single phase input is utilized in three phase inverter for this experiment, the single phase terminals of APS-300 and GPL-300A have to be modified as shown in the figure 4.10 followed by the wiring method shown in the figure 4.11.



(a) (b)

Figure 4.10 (a) APS-300 modified terminal setting (b) GPL-300A modified terminal setting

Figure 4.11 Experiment wiring figure

After wiring, make sure the PEK-130 switch is OFF followed by turning the PEK-005A switch ON. The DSP red indicator lights on as the figure 4.12 shown, which means the DSP power is steadily normal.

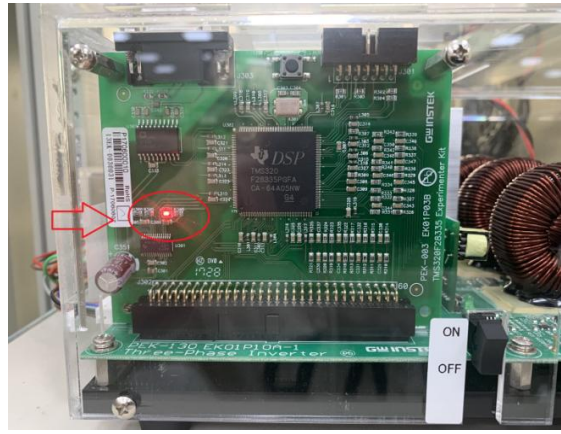


Figure 4.12 DSP normal status with light on

Refer to the appendix B for burning procedure to burn the PEK-130_Lab5_V11.0.3 program into DSP followed by referring to the appendix C for RS232 connection to proceed to connection.

Connect the test leads of oscilloscope to Vo-AB, Vo-BC and Io-A, respectively, as the figure 4.13 shown.

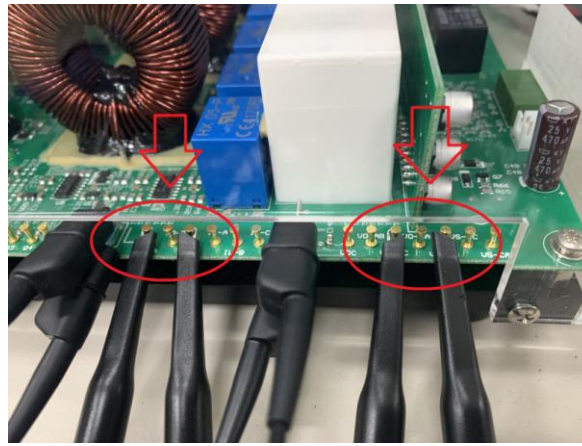
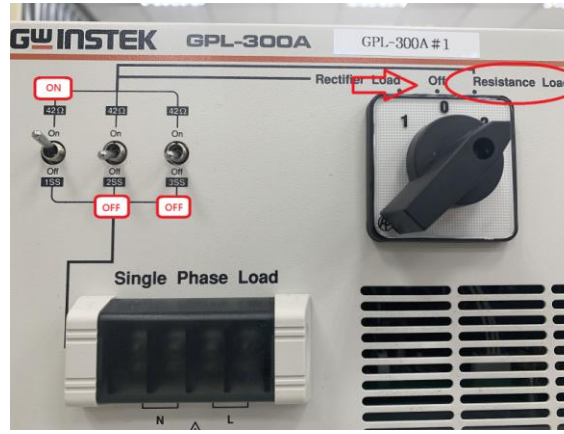


Figure 4.13 Oscilloscope test leads wiring

After powering on GPL-300A, set Resistance Load for Three Phase Load and set ON for 1SS, further setting OFF for 2SS and 3SS. The load is 42ohm then as the figure 4.14 shown.

Figure 4.14

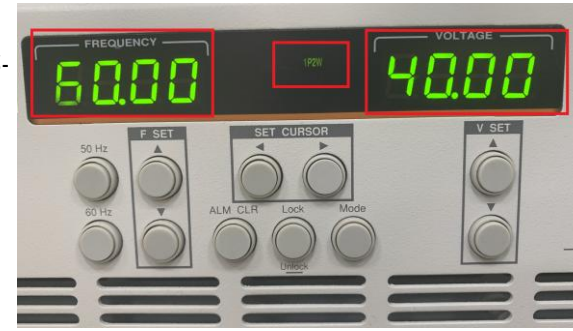
The settings of GPL-300A (42ohm)



After powering on APS-300, set 60Hz for frequency and 1P2W for mode and 40V for output voltage as the figure 4.15 shown.

Figure 4.15

The settings of APS-300



After setting up and APS-300 power output, turn on the switch of PEK-130.

Experiment Result

(1) Three arm single phase rectifier – inverter linear load

The figure 4.16 indicates waveforms of output voltage current and input voltage current. Due to the reversal between current direction and current sensing, it is required to reverse current measuremt test lead. The figure 4.17 has shown that yellow waveform measurement is input voltage Vs-AB, and green is input current Io-A (inverse), and pink is output current Io-C (inverse), and lastly blue is output voltage Vo-BC.

Figure 4.16

Waveforms of output voltage current and input voltage current (load 42ohm)

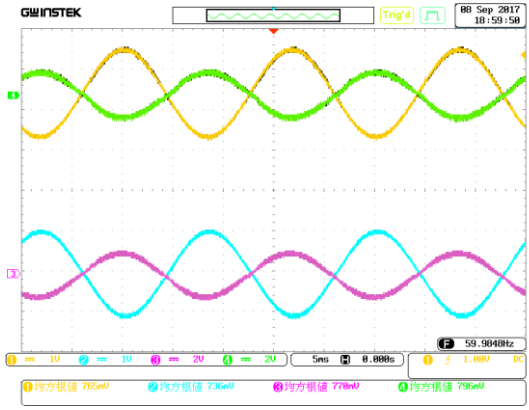
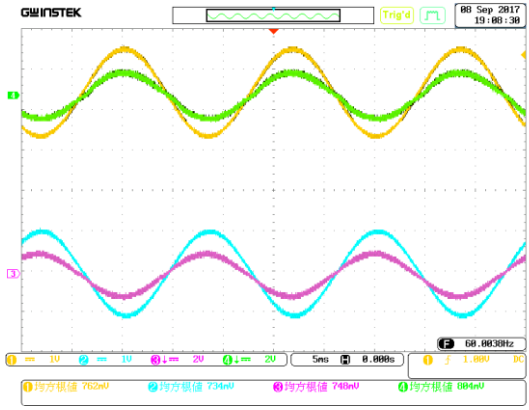


Figure 4.17

Waveforms of output voltage current and input voltage current after inversion



The test above is of load 42 ohms and switchable to 21 ohms as the figure 4.18 shown where both 1SS and 2SS are set ON, whereas 3SS is set OFF. The figure 4.19 indicates the waveforms of output voltage current and input voltage current (load 21 ohm).

Figure 4.18

Settings of GPL-300A (21 ohm)

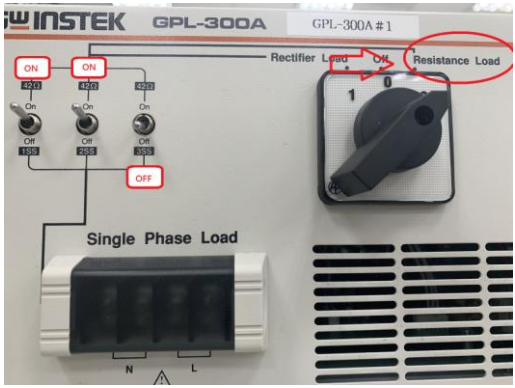
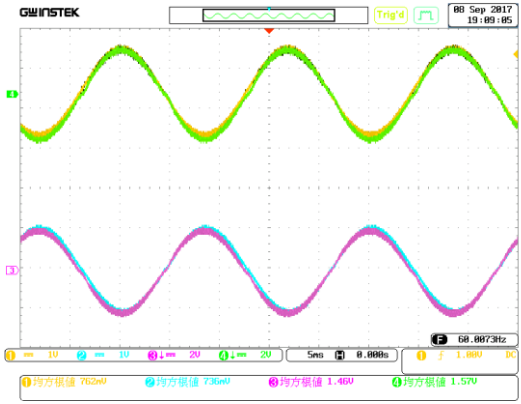


Figure 4.19 Waveforms of output voltage current and input voltage current (load 21 ohm)



As the figure 4.20 displayed, 14 ohm is available for switch and 1SS, 2SS as well as 3SS are set ON. The figure 4.21 indicates waveforms of output voltage current and input voltage current (load 14 ohm).

Figure 4.20

Settings of GPL-300A (14 ohm)

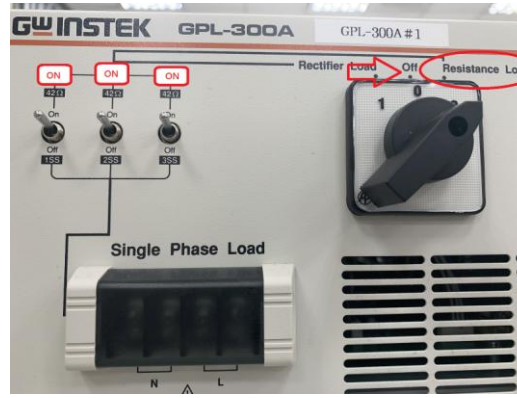
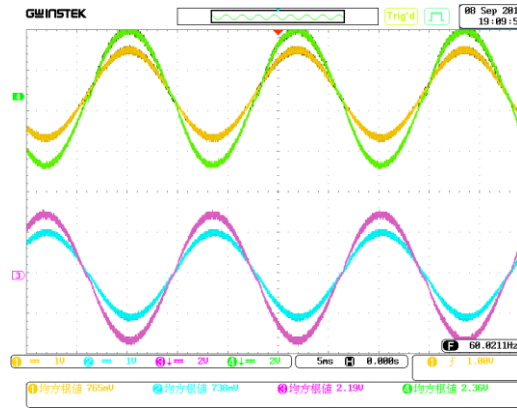


Figure 4.21

Waveforms of output voltage current and input voltage current (load 14 ohm)



When sending waveform from RS232 back to PC side, in order to simplify the process, the following waveforms observed on PC side show the data with load 14 ohm only. The figure 4.22 indicates input voltage V_{ac}, input current I_s and DC voltage V_{dc}. The figure 4.23 shows output voltage V_{out}, output current I_o and DC voltage V_{dc}. The figure 4.24 demostrates the output current command tracking of I_{oc} and I_{occ}. The figure 4.25 displays the input current current command tracking of I_{oa} and I_{oac}. The figure 4.26 indicates the output voltage command tracking of V_o and V_{oc}.

Figure 4.22

The waveforms of input voltage, input current and DC voltage sent from RS232

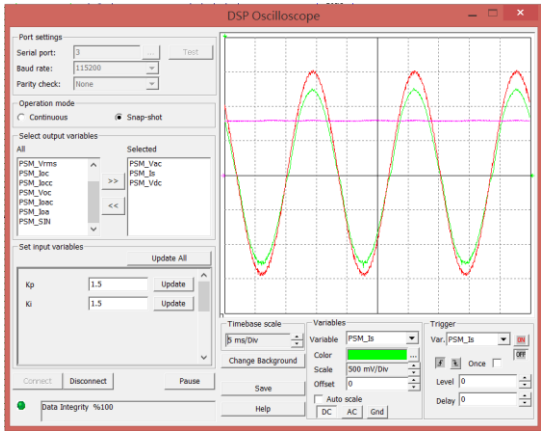


Figure 4.23

The waveforms of output voltage, output current and DC voltage sent from RS232

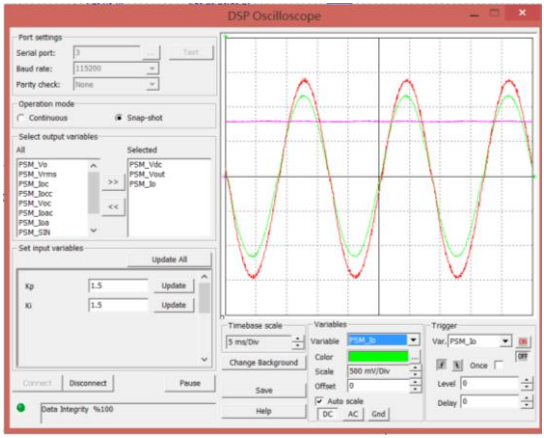


Figure 4.24

The I_{oc} and I_{occ} output current command tracking of control loop sent from RS232

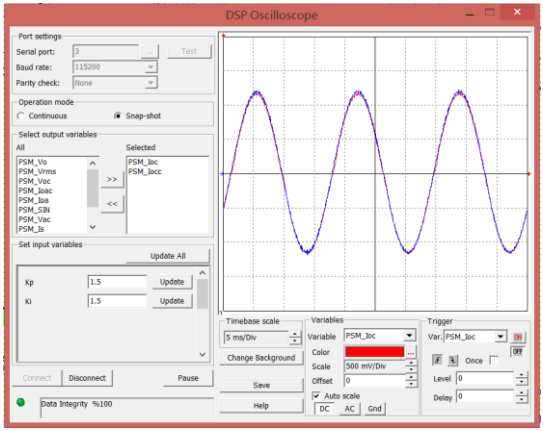


Figure 4.25

The I_{oa} and I_{oac} input current command tracking of control loop sent from RS232

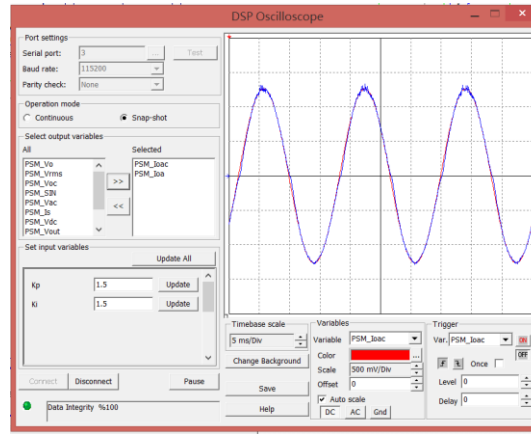
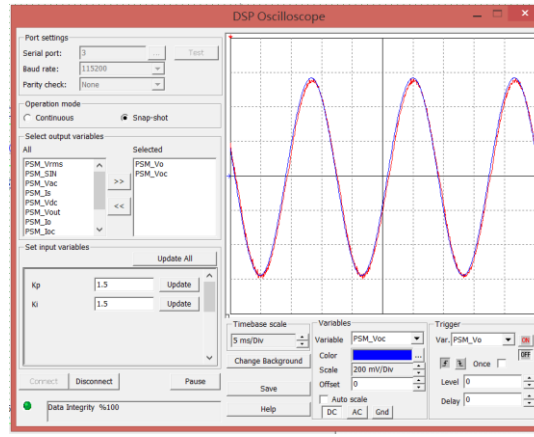


Figure 4.26

The V_o and V_{oc} output voltage command tracking of control loop sent from RS232



After the experiment, turn off the PEK-130 power button followed by turning GPL-300A to OFF state and lastly turning off APS-300.

(2) Three-arms single-phase rectifier – inverter rectified load

Repeat the experiment steps in which adjust the GPL-300A setting by setting Resistance Load and setting ON for 1SS, further setting OFF for 2SS and 3SS. The rectified load is 42ohm then as the figure 4.26 shown.

Figure 4.27

The settings of GPL-300A rectified load with 42ohm setting

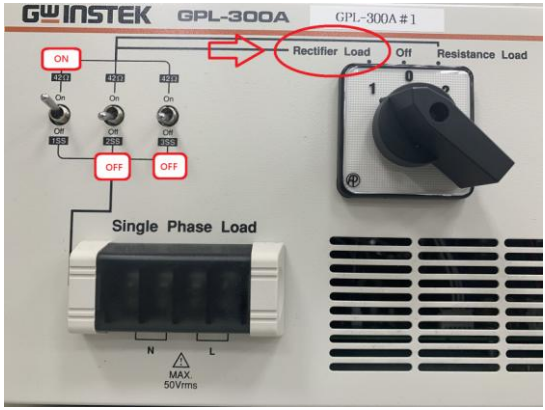
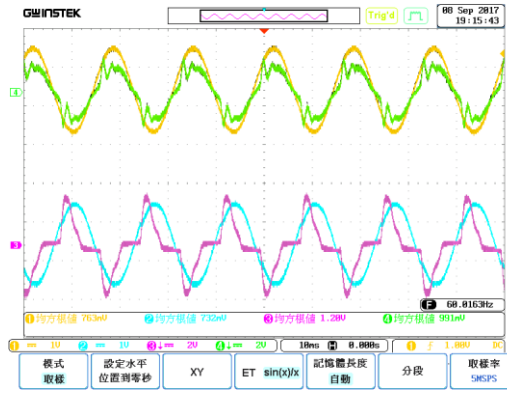


Figure 4.28 indicates the waveforms of output voltage current and input voltage current with test load 42ohm.

Figure 4.28

The waveforms of output voltage current and input voltage current of rectified load



It is available to switch to 21ohm as the figure 4.29 shown where 1SS, 2SS are set ON and 3SS is set OFF instead with the load 12ohm. The figure 4.30 indicates the waveforms of output voltage current and input voltage current (load 21ohm).

Figure 4.29

The setting of GPL-300A rectified load 21ohm

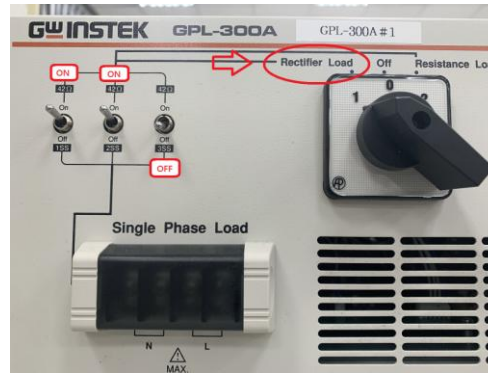
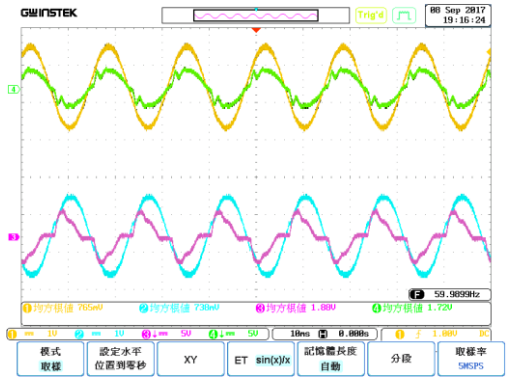


Figure 4.30

The waveforms of output voltage current and input voltage current (load 21ohm)



It is available to switch to 14ohm as the figure 4.31 shown where 1SS, 2SS as well as 3SS are set ON with the load 14ohm. The figure 4.32 indicates the waveforms of output voltage current and input voltage current (load 14ohm).

Figure 4.31

The setting of GPL-300A rectified load 14ohm

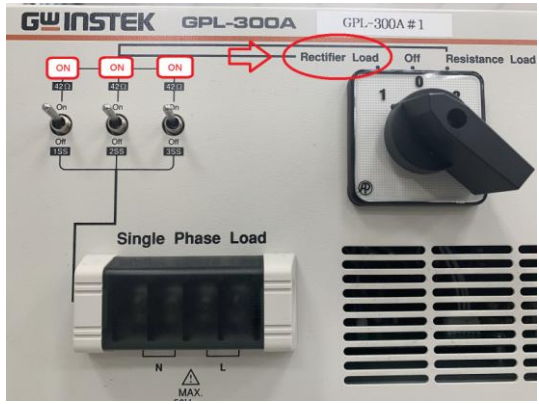
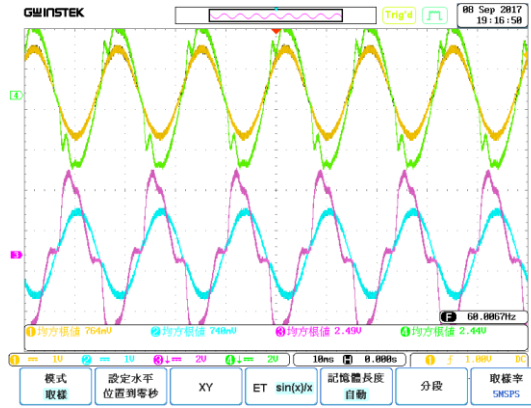


Figure 4.32

The waveforms of output voltage current and input voltage current (load 14ohm)



The result of waveforms observed in PC side sent from RS232. The figure 4.33 indicates input voltage V_{ac}, input current I_s and DC voltage V_{dc}. The figure 4.34 indicates output voltage V_{ou}, output current I_o and DC voltage V_{dc}. The figure 4.35 indicates both I_{oc} and I_{occ} output current command tracking. The figure 4.36 indicates both I_{oa} and I_{oac} input current command tracking. The figure 4.37 indicates both V_o and V_{oc} output voltage command tracking.

Figure 4.33

The diagram of input voltage, input current and DC voltage sent from RS232

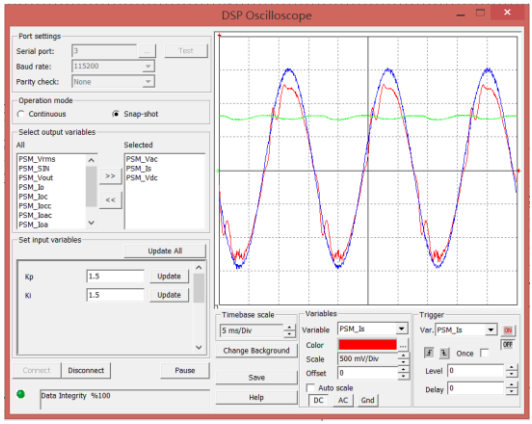


Figure 4.34

The diagram of output voltage, output current and DC voltage sent from RS232

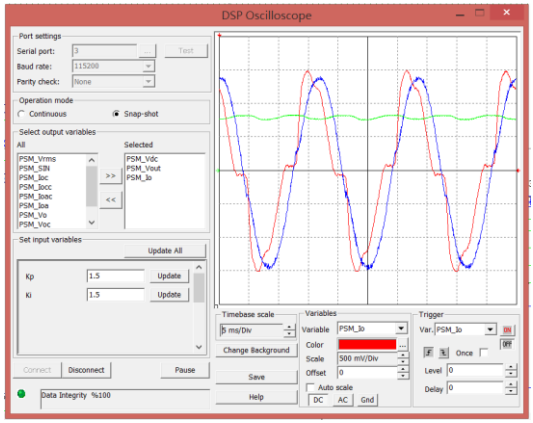


Figure 4.35

The I_{oc} and I_{occ} output current command tracking of control loop sent from RS232

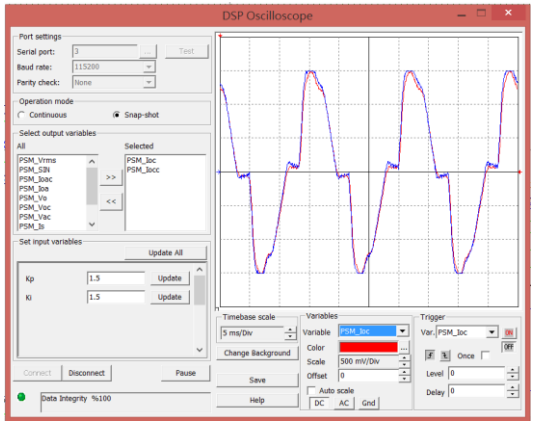


Figure 4.36

The I_{oa} and I_{oac} input current command tracking of control loop sent from RS232

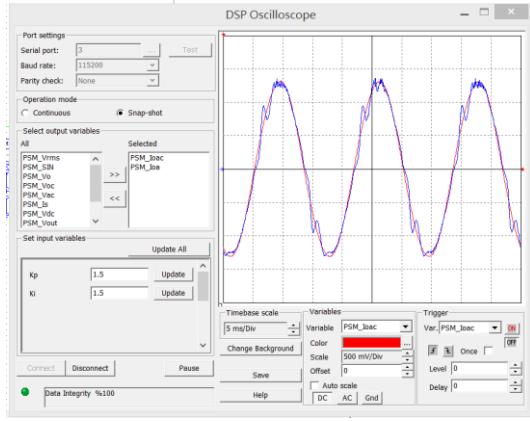
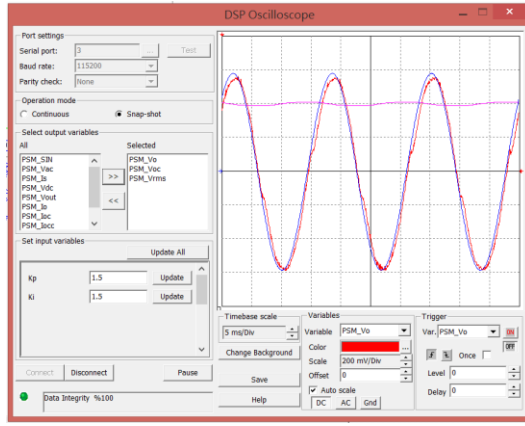


Figure 4.37

The V_o and V_{oc} output voltage command tracking of control loop sent from RS232



After completing the experiment, turn off the power key of PEK-130 followed by setting GPL-300A to OFF state and then turning off APS-300. Lastly, restore the output terminals of APS-300 and GPL-300A back to the default settings as the figure 4.38 shown.

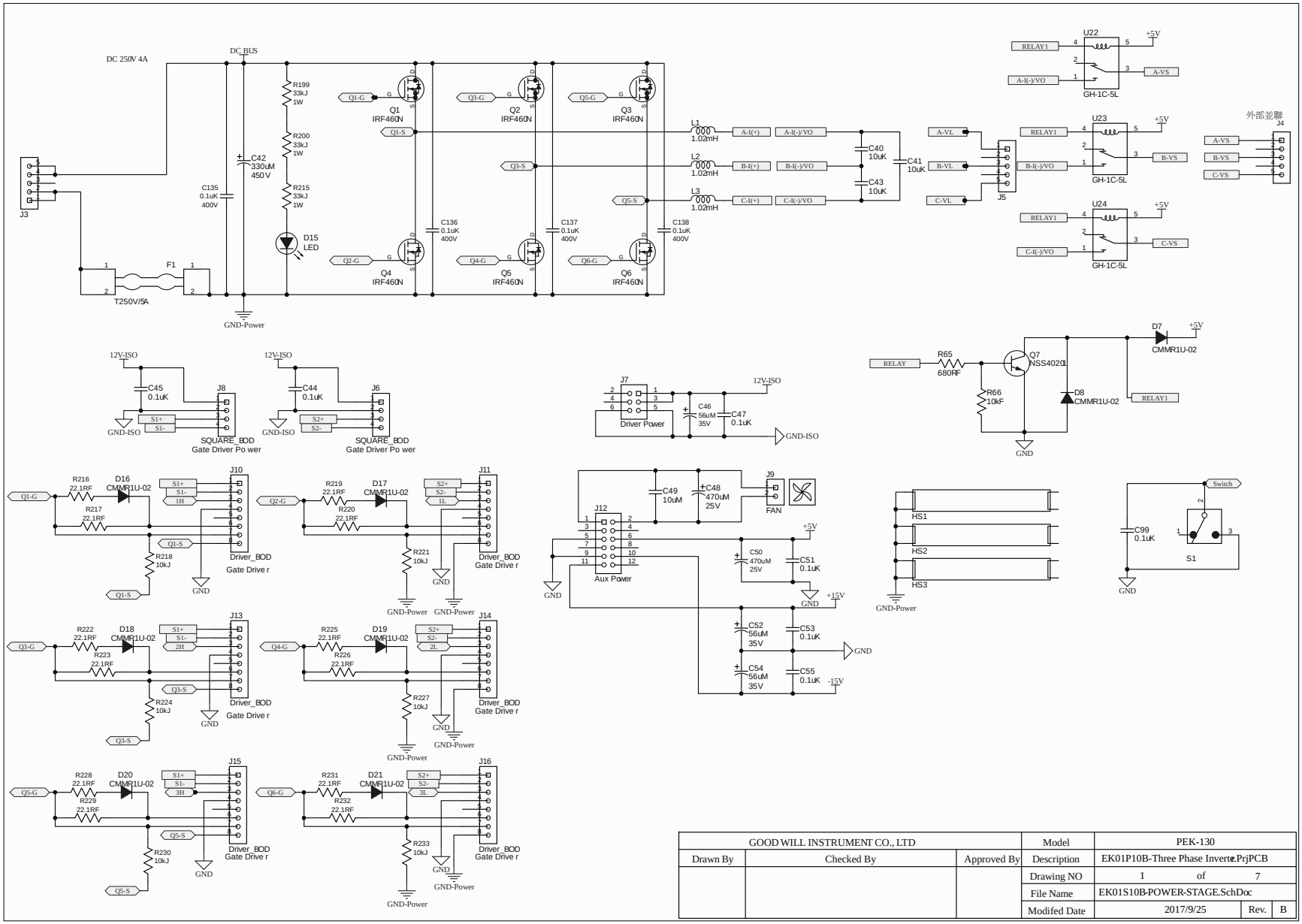
(a)

(b)

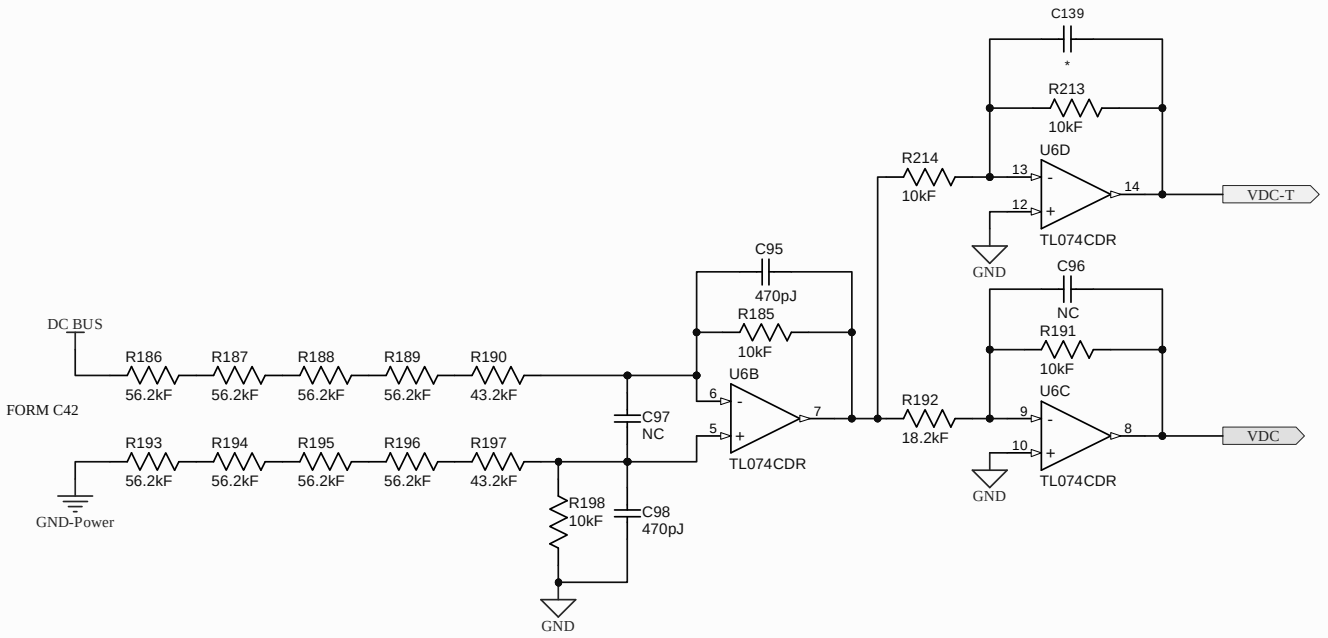
Figure 4.37 (a) APS-300 default terminal setup (b) GPL-300A default terminal setup

Appendix A – PEK-130 Circuit Diagram

Three Phase Inverter



GOOD WILL INSTRUMENT CO., LTD			Model	PEK-130	
Drawn By	Checked By	Approved By	Description	EK01P10B-Three Phase Inverter.PrjPCB	
			Drawing NO	1 of 7	
			File Name	EK01S10B-POWER-STAGE.SchDoc	
			Modifed Date	2017/9/25	Rev. B



GOOD WILL INSTRUMENT CO., LTD			Model	PEK-130		
Drawn By	Checked By	Approved By	Description	EK01P10B-Three Phase Inverter.PrjPCB		
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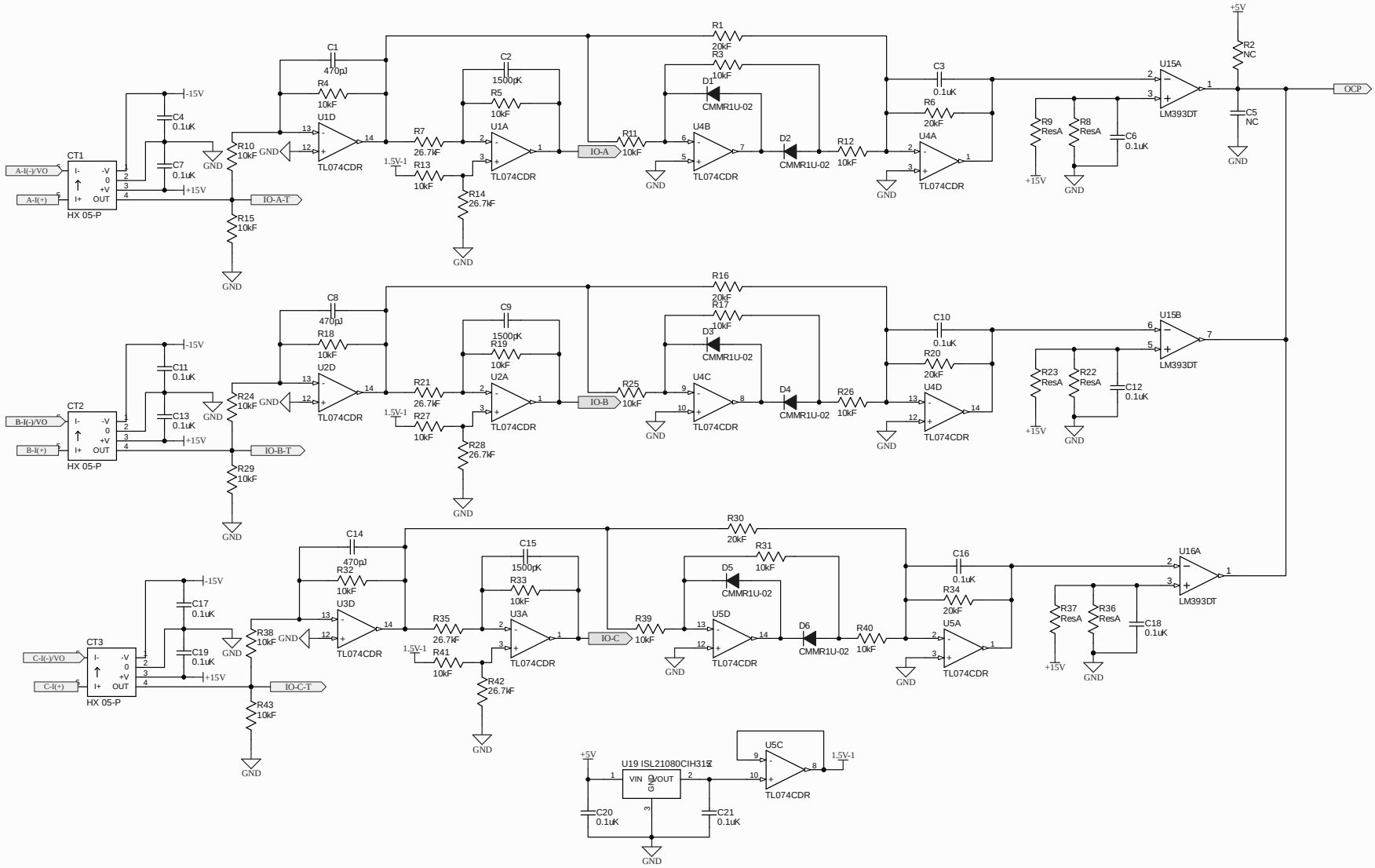
			File Name	EK01S10B-VIS.SchDoc		
			Modifed Date	2017/9/25	Rev.	B



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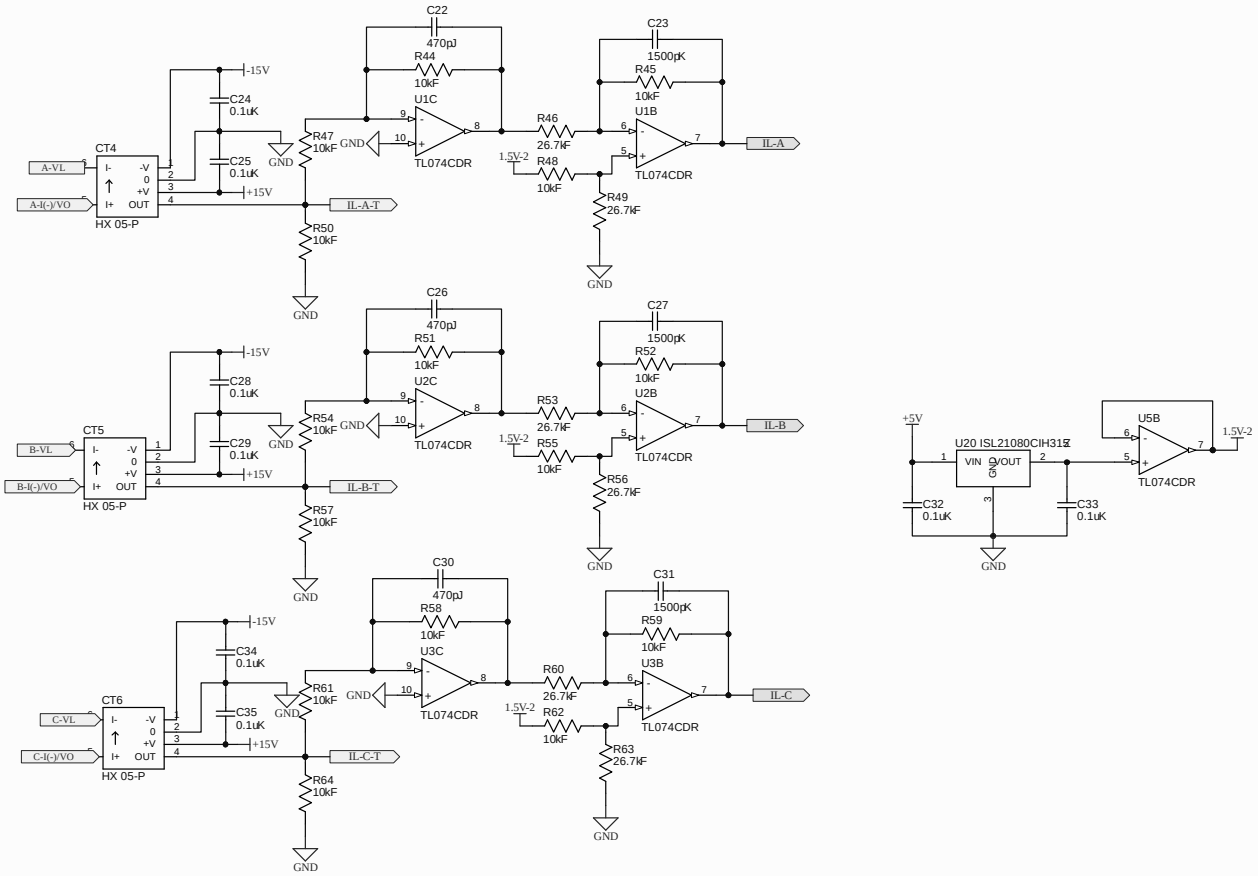

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Drawn By	Checked By	Approved By	Description	EK01P10B-Three Phase Inverter.PrjPCB		
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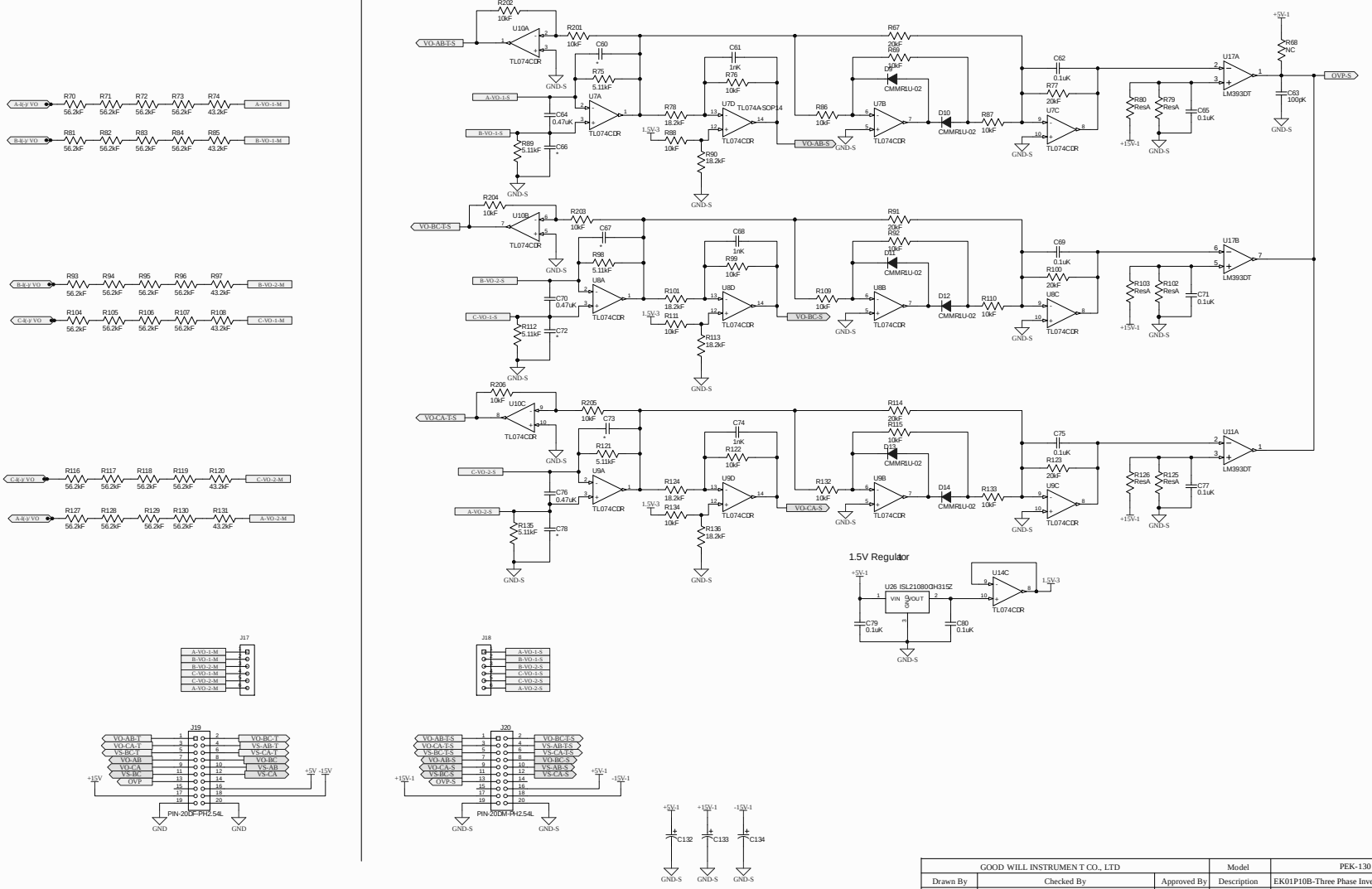
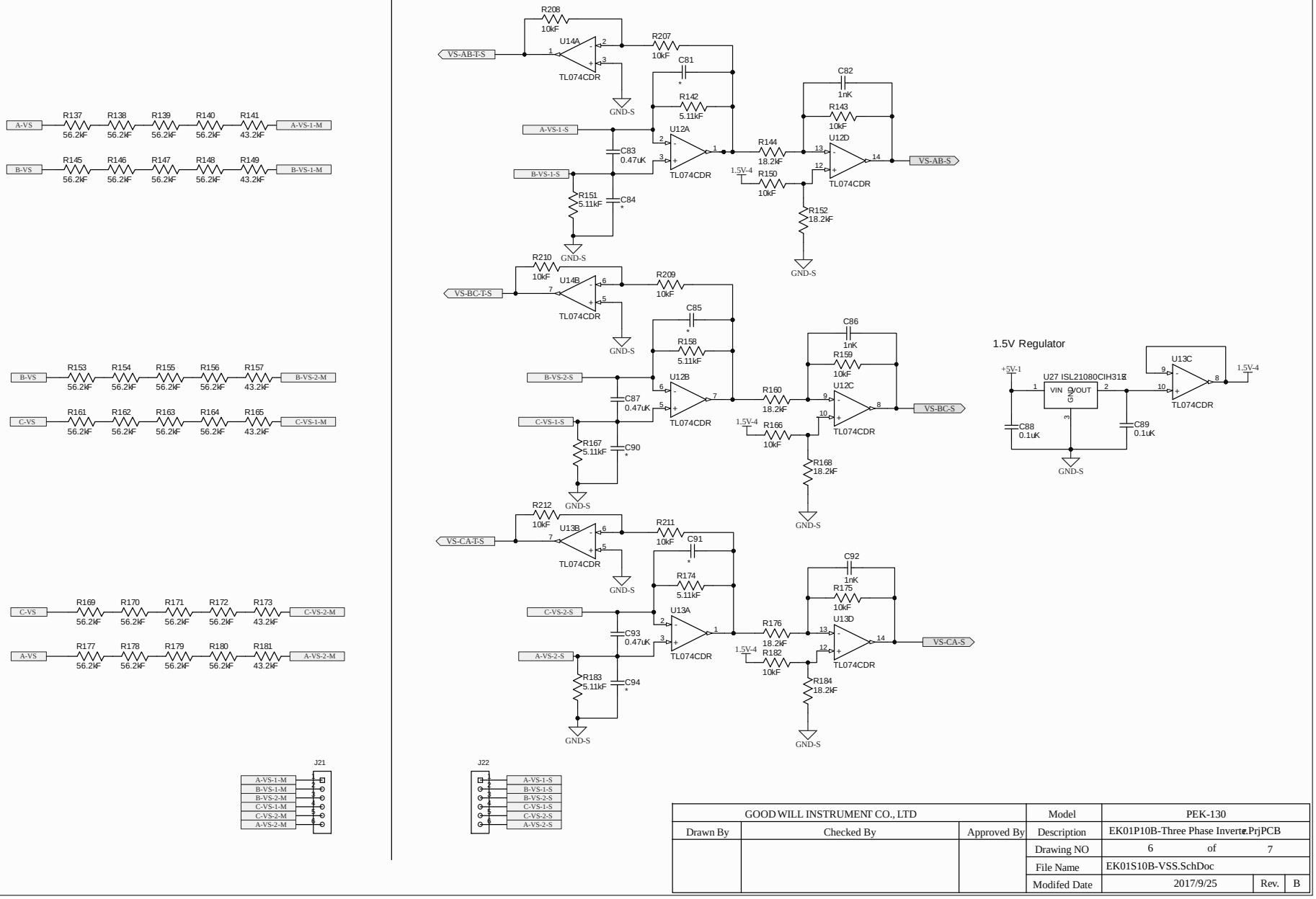
			File Name	EK01S10B-ILS.SchDoc		
			Modifed Date	2017/9/25	Rev.	B


1.5V Regulator
GOOD WILL INSTRUMEN T CO., LTD
Model
PEK-130
Drawn By
Checked By
Approved By
Description
EK01P10B-Three Phase Inverter.PrjPCB
Drawing NO
5 of 7
File Name
EK01S10B-VOS-OVP.SchDoc
Modifed Date
2017/9/25
Rev.
B



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Drawn By	Checked By	Approved By	Description	EK01P10B-Three Phase Inverter.PrjPCB	
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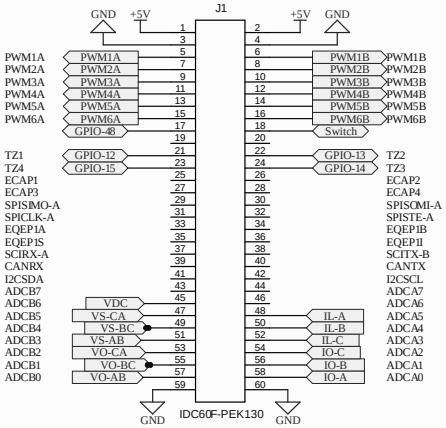
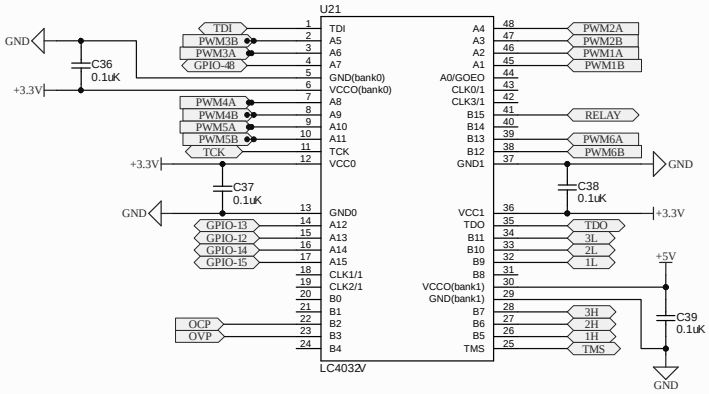
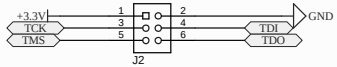
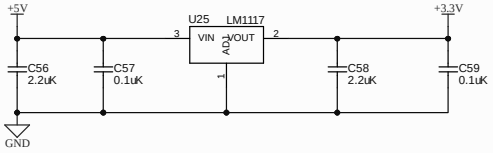
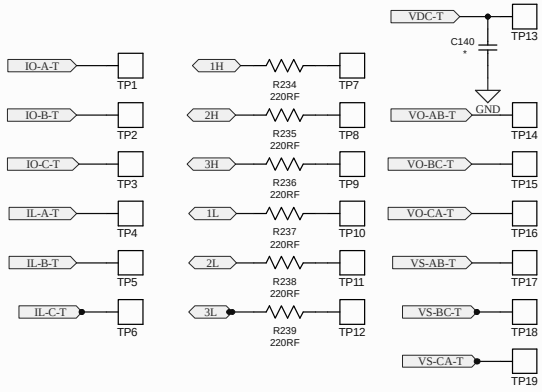
			File Name	EK01S10B-VSS.SchDoc	
			Modifed Date	2017/9/25	Rev. B

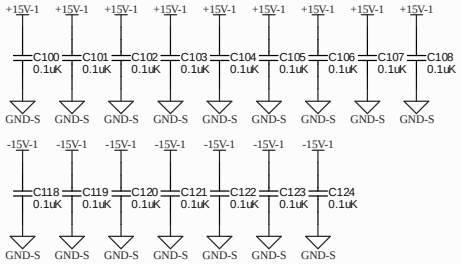


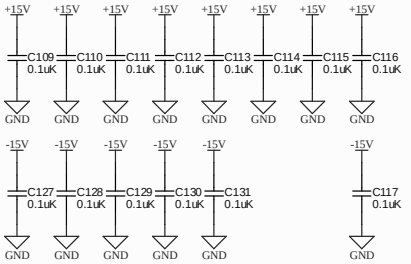


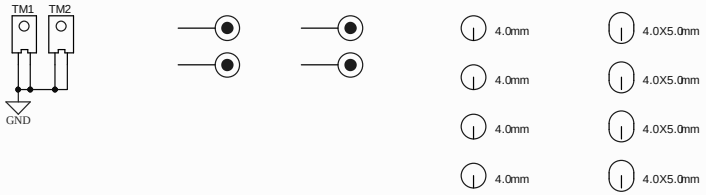












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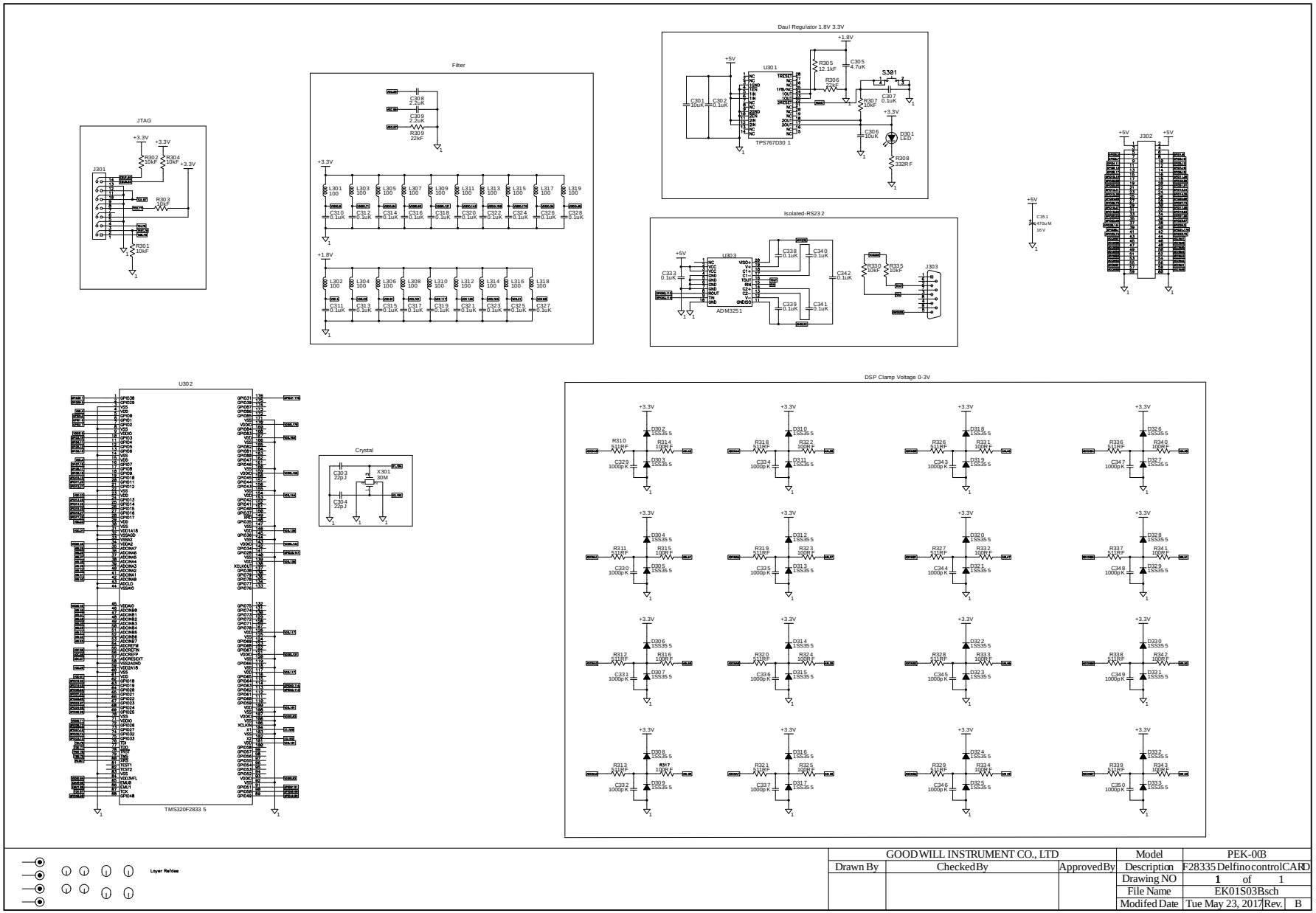
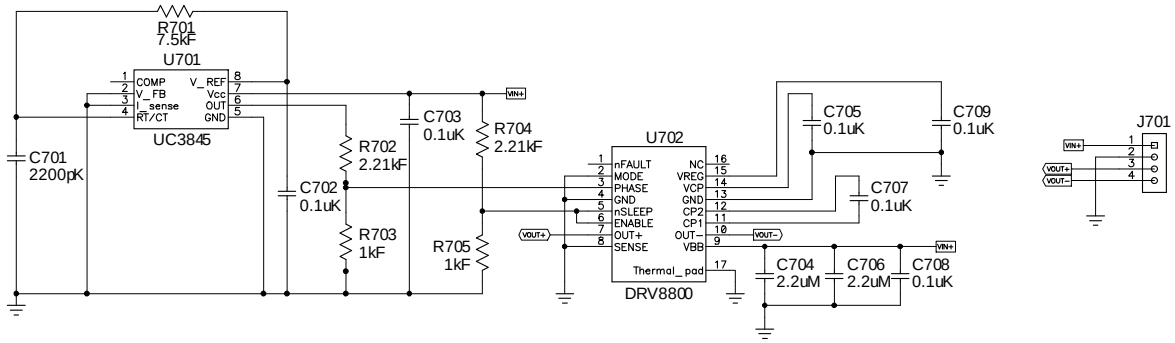
			Drawing NO	7 of 7	
			File Name	EK01S10B-INTERFACE-CPLD.SchDoc	
			Modifed Date	2017/9/25	Rev. B

F28335 Delfino control CARD



Gate Driver Power



Layer Refdes

GOOD WILL INSTRUMENT CO., LTD			Model	PEK-100	
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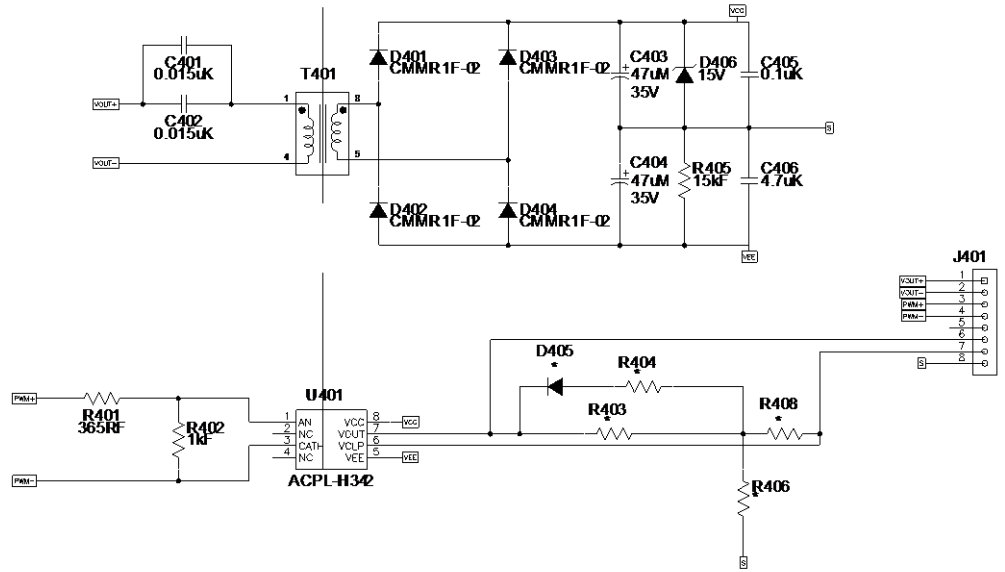
			File Name	EK01S07A.sch	
			Modifed Date	Mon Mar 09, 2015	Rev. A

Gate Driver



Layer Refdes

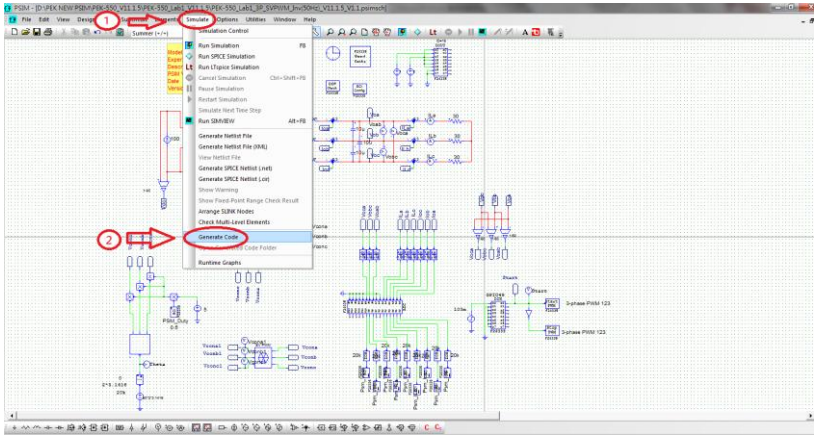
GOOD WILL INSTRUMENT CO., LTD			Model	PEK-004	
Drawn By	Checked By	Approved By	Description	Gate Driver	
			Drawing NO	1 of 1	
			File Name	EK01S04B.sch	
			Modifed Date	Fri May 19, 2017	Rev. B

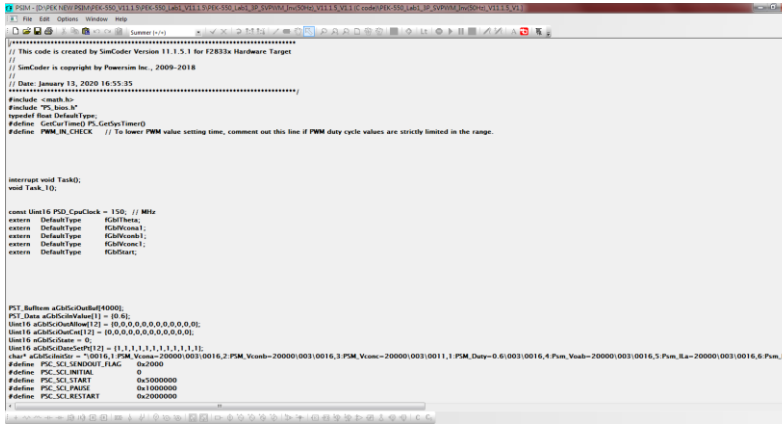
Appendix B – C Code Burning Procedure

This appendix takes "PEK-550_Lab1_3P_SVPWM_Inv(50Hz)_V11.1.5_V1.1" as an example for the instruction. See the detailed steps below.

Operating steps

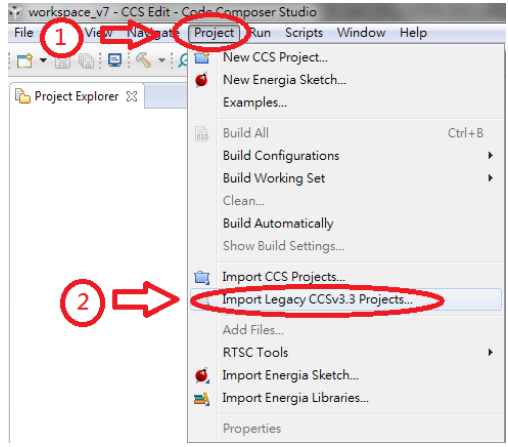
1. Open the digital circuit file "PEK-550_Lab1_3P_SVPWM_Inv(50Hz)_V11.1.5_V1.1" within the PSIM program followed by clicking "Generate Code" from "Simulate" tab. The PSIM will generate C Code automatically as shown below.



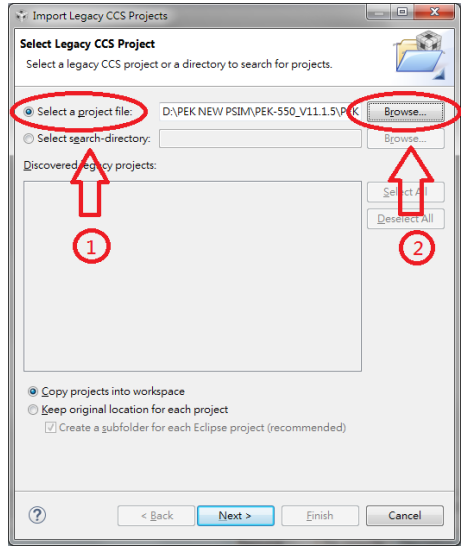


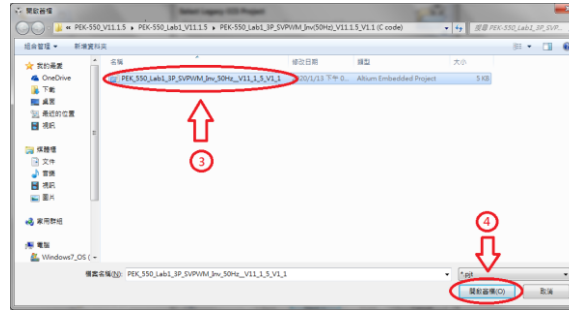
2. A folder of identical name with the PSIM circuit file in which the required files for burning and C Code are well saved will be generated in the location of PSIM circuit file by system.

3. Open CCS and select “Project” tab followed by clicking ”Import Legacy CCSv3.3 Projects” as the figure below.

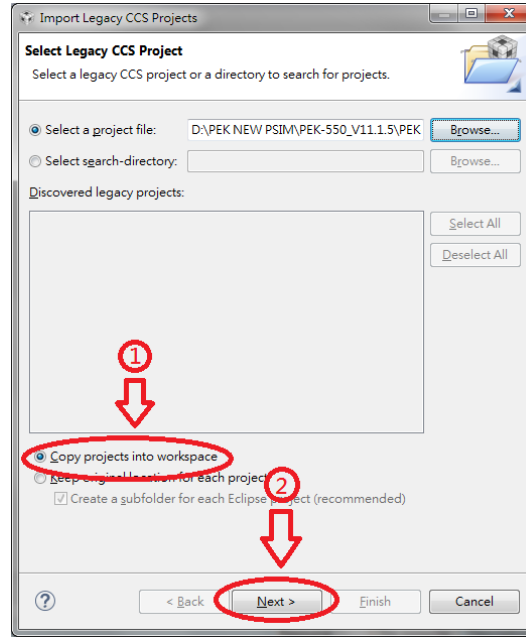


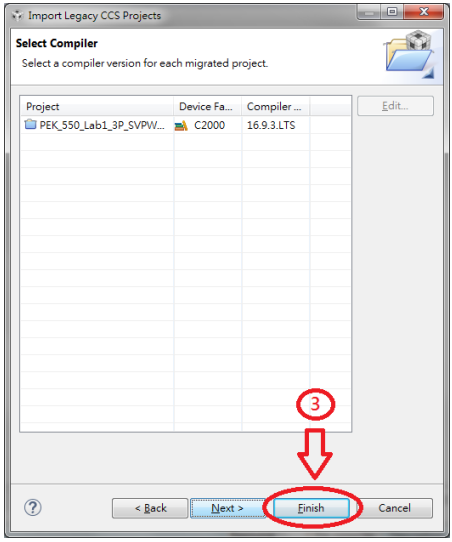
4. Go to “Select a project file” and click “Browser” followed by searching the folder where C Code is located and selecting the file with name extension “.pjt” as the following figure shown.

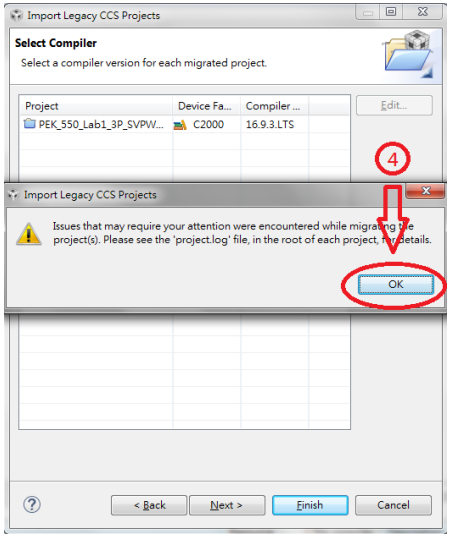




5. Select " Copy projects into workspace " followed by clicking "Next" and then "Finish" to import C Code into CCS program. See the figure below.




Import Legacy CCS Projects
Select Compiler
Select a compiler version for each migrated project.
Project
Device Fa...
Compiler ...
PEK_550_Lab1_3P_SVPW...
C2000
16.9.3.LTS
Edit...
3
< Back
Next >
Finish
Cancel


Import Legacy CCS Projects
Select Compiler
Select a compiler version for each migrated project.
Project
Device Fa...
Compiler ...
PEK_550_Lab1_3P_SVPW...
C2000
16.9.3.LTS
Edit...
4
Import Legacy CCS Projects
Issues that may require your attention were encountered while migrating the project(s). Please see the 'project.log' file, in the root of each project, for details.
OK
< Back
Next >
Finish
Cancel

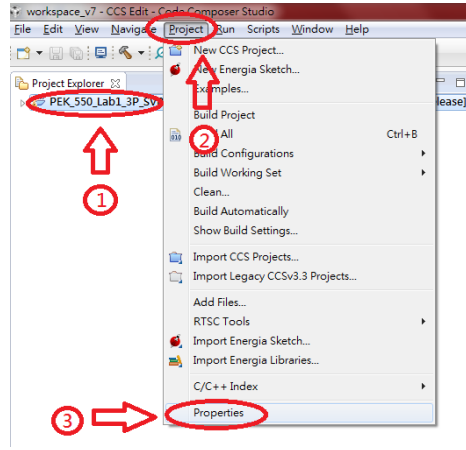
6. Select C Code file and choose “Properties” from “Project” tab. The setting steps are as follows.

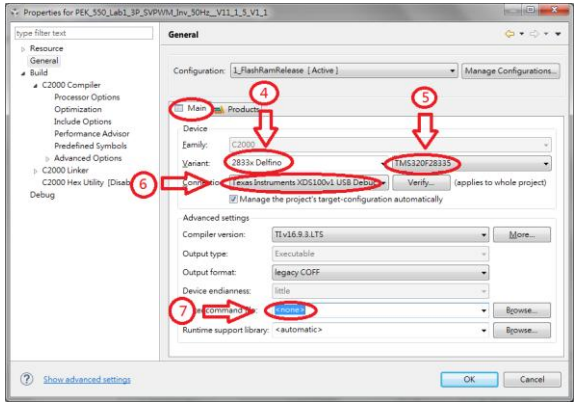
   1) Select “TMS320F28335” of “2833X Delfino” from Variant under Main tab.

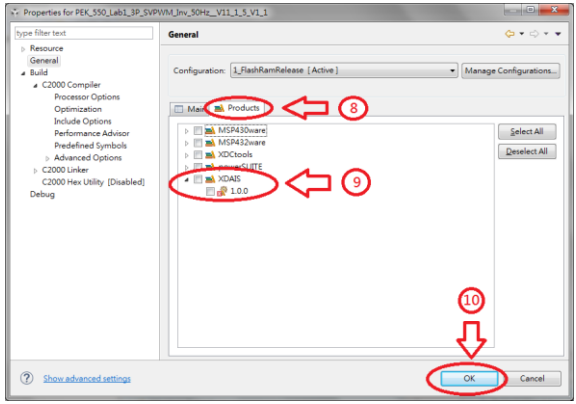
   2) Select “Texas Instruments XDS100v1 USB Debug Probe” from Connection under Main tab.

   3) Select “none” from Linker command file under Main tab.

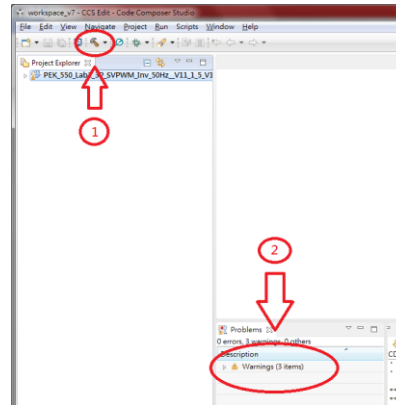
   4) Deselect “XDAIS” under Project tab. (Ignore this step if your CCS version doesn’t provide this option.



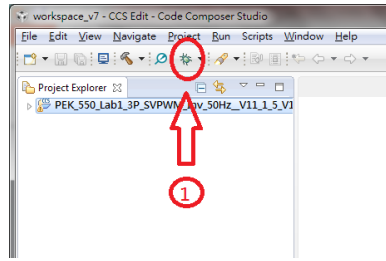




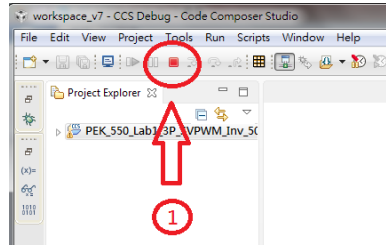
7. After the setting, click "Build" for compilation. If no errors occur after compiling, the program is eligible for burning. Simply ignore the warnings, which have no impact on burning process.



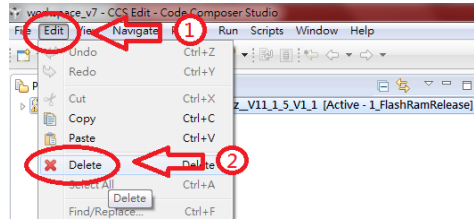
8. Connect PEK-006 to PC and PEK module respectively followed by clicking “Debug” to proceed to burning process.

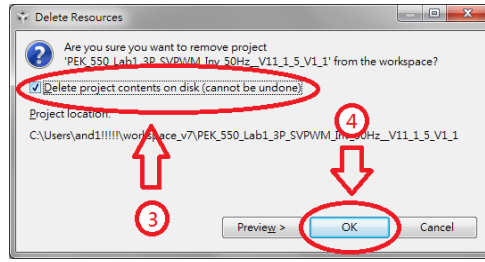


9. After the burning process, click "Terminate" and remove "PEK-006"to finish the entire procedure.



10. If it needs to delete file, select C Code file followed by selecting "Delete" under "Edit" tab and checking "Delete project contents on disk". Finally, click "OK" to complete the action.



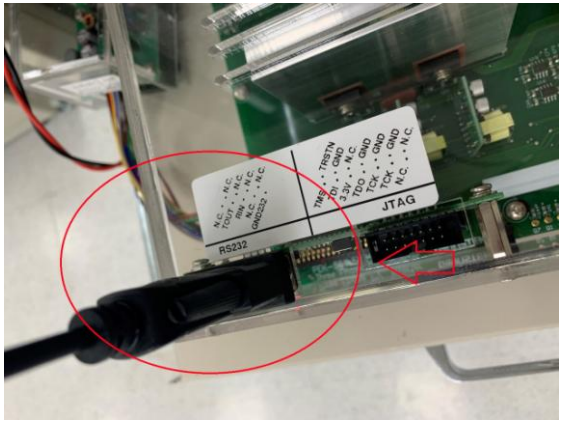


Appendix C – RS232 Connection

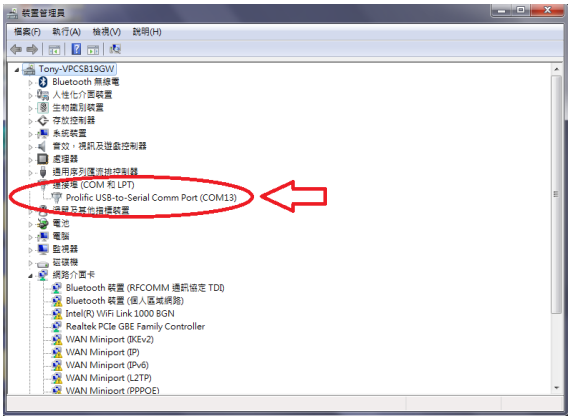
Operating steps

1. Connect PEK-005A to PEK module and make sure DSP is working normally.

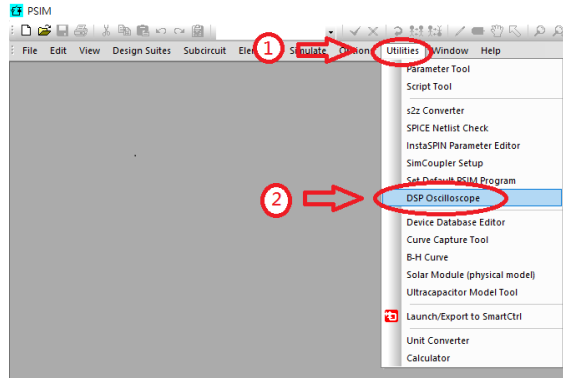
2. Connect one end of RS232 cable to PC, and the other end to the RS232 connector of PEK module.



3. Open Device Manger from PC and identify the COM port number being utilized by RS232 cable.



4. Open PSIM program and select “DSP Oscilloscope” under “Utilities” tab.

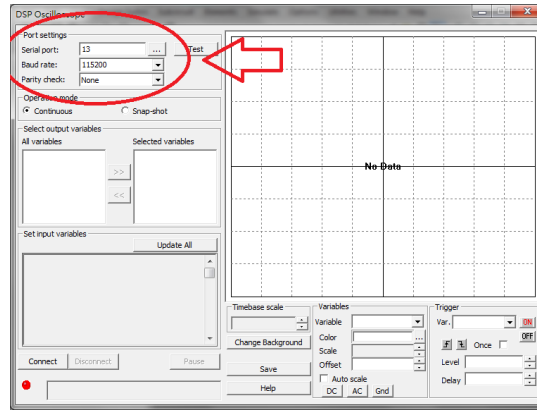


5. The Port settings are as follows.

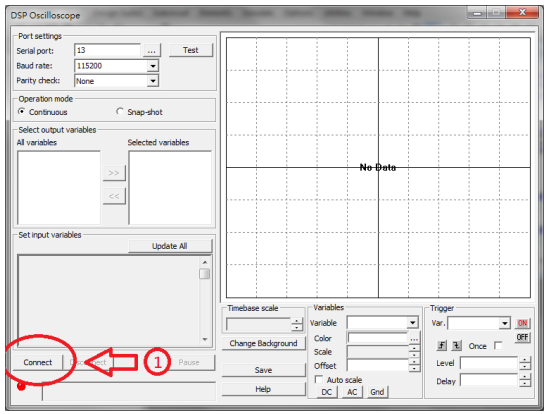
   1) Select the COM port being used by RS232.

   2) Set 115200 for Baud rate.

   3) Set None for Parity check.



6. After the settings, click "Connect" to proceed to RS232 connection.



7. Both the output and input variables schemed within PSIM circuit can be clearly observed when connection is properly established.