Single-phase DC - AC Converter Experiment Module

PEK-110

USER MANUAL

GW INSTEK PART NO. 82EK-11000M01

ISO-9001 CERTIFIED MANUFACTURER

GW INSTEK

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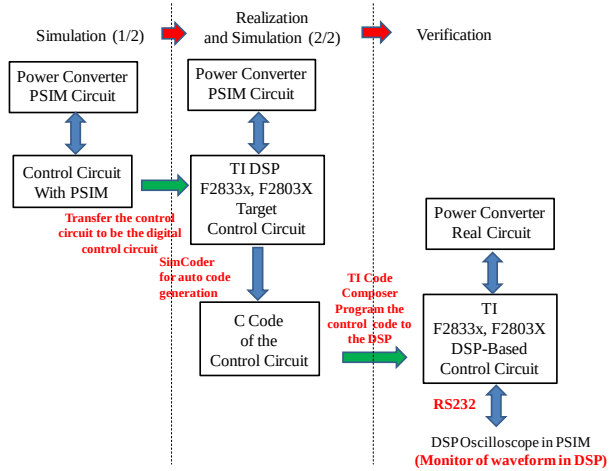
Introduction

The power converter utilizing digital control, which largely improves both functions and performances, further elevating the added values itself, is the mainstream tendency for the contemporary industrial products. It has seen more and more digital control technologies deployed in power converters nowadays. The purpose of this manual as shown in the figure 1.1 is to provide a learning platform for power converter of specifically digital control, having users, via PSIM software, to understand the principle, analysis as well as design of power converter through simulating process. More than that, it helps convert, via SimCoder tool of PSIM, control circuit into digital control and proceed to simulation with the circuit of DSP, eventually burning the control program, through simulating verification, in the DSP chip. Also, it precisely verifies the accuracy of designed circuit and controller via control and communication of DSP.

Figure 1.1 The process in details



The main features of this teaching aid are elaborated below.

1. To provide both electric and electronic analysis, design, simulation and practical verification.

2. To complete programming and burning via hardware circuit established within PSIM, facilitating new learner in DSP firmware to quickly grasp tips for programming, thus realizing the area of digital control with ease.

3. This teaching aid offers resourceful instructional materials containing SimCoder usage to set up method of hardware programming, in-depth instructions on teaching aid to each part of circuit, detailed principle and design of experiment circuit, PSIM circuit simulating file, DSP hardware layout and setting, the method of program burning, etc.

4. This teaching aid provides completely educational slides for both teachers and users' reference.

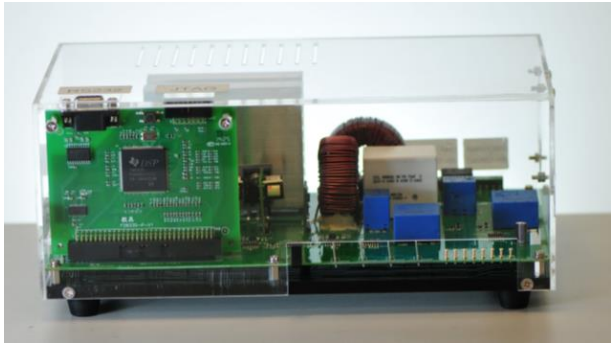
5. This teaching aid offers purchasers for free on any additional experimental items later.

Instruction on Teaching Aid of Single-phase Inverter Module

As the figure 1.2 shown, the single-phase inverter experiment module currently provides the following 5 experiments.

1. Unipolar voltage switching SPWM
2. Stand alone inverter with dual loop inductor current control
3. Grid connected single-phase inverter
4. Totem Pole Bridgeless PFC AC-DC converter
5. Full-bridge AC-DC switching rectifier

Figure 1.2 Single-phase Inverter experiment module

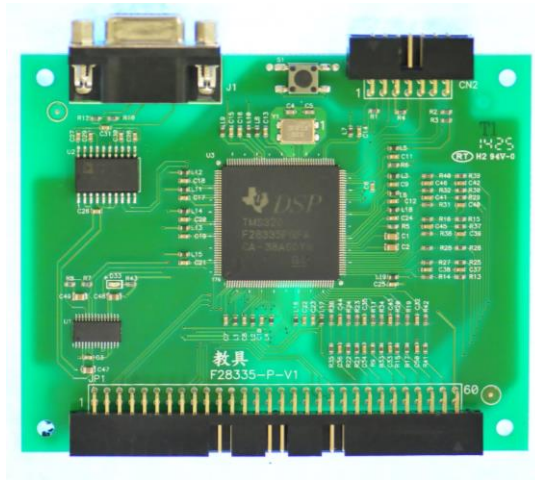


In addition to the Inverter main power circuit, the experiment module comprises the following components.

DSP Control Module

- The module TI F28335 is available.
- Each module is equipped with the isolated RS-232 interface, which allows DSP internal signal to be sent back to PSIM for observation during the process of experiment.

Figure 1.3 DSP Control Module



Auxiliary Power Module

Input voltage ranges from 100 to 250Vac with multiple isolated power outputs (+15V, -15V, 12V, 5V) and the output maximizes up to 23W. Check the table 1.1 for the specification.

Description	Symbol	Min	Typ	Max	Units
Input					
Voltage	V_{IN}	100		250	VAC
Frequency	f_{LINE}	47	50/60	63	Hz
Output					
Output Voltage 1	V_{OUT1}	11.4	12	12.6	V
Output Current 1	I_{OUT1}	0.1	0.5	0.6	A
Output Voltage 2	V_{OUT2}	11.4	12	12.6	V
Output Current 2	I_{OUT2}	0.1	0.5	0.6	A
Output Voltage 3	V_{OUT3}	14.25	15	15.75	V
Output Current 3	I_{OUT3}	0.1	0.2	0.24	A
Output Voltage 4	V_{OUT4}	-14.25	-15	-15.75	V
Output Current 4	I_{OUT4}	-0.1	-0.2	-0.24	A
Output Voltage 5	V_{OUT5}	4.75	5	5.25	V
Output Current 5	I_{OUT5}	0.5	1	1.2	A
Total Output Power	P_{OUT}	7.505	23	28.98	W

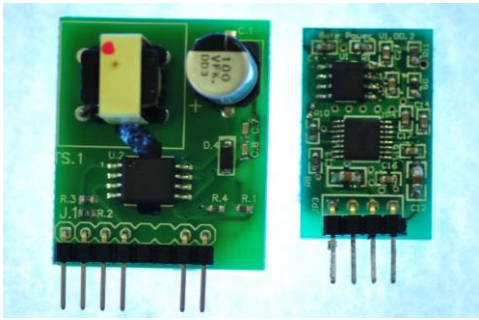
Table 1.1

Figure 1.4 Flyback Auxiliary Power Module

Motor Power and Switch Driver Modules

- With one set of 12V isolated power, this module can provides multiple groups of isolated power, addressing the issue of complicated multiple groups of isolated motor powers validly.
- Driver module offers driving power of high frequency and current (2A) with the protection circuit equipped with Miller effect to prevent from false actions by accident.

Figure 1.5 Motor Power and Switch Driver Modules



JTAG Burning Module

It offers isolated protection burning to free from computer burnout during the experimental process due to lack of proper insulation.

Figure 1.6 JTAG Burning Module

The Goal of Experiment

The teaching aid proceeds to query-oriented learning on the basis of circuit analysis, design, simulation, experiment, etc., and designs electric circuit and controller quantitatively based on the converter specification. Furthermore, it facilitates readers to have profound understanding of relevant technology of inverter, via PSIM simulation verification, SimCoder programming process, therefore developing the following capabilities for readers.

1. The capability of analysis and design on power converter.
2. PSIM circuit simulating capability.
3. The design capability for controller of power converter.
4. DSP digital control technology (programming via SimCoder).
5. The layout and integration of hardware and firmware.
6. The capability for circuit production and verification step by step.

The Descriptions on Chapters

See the chapter arrangements as follows

Brief	Briefly describes the circuit setup, experimental method and experimental purpose of the teaching aid. It also explains the contents of each chapter.
PSIM Brief	Briefly introduces the setup and functions of PSIM to help user realize the working contents of PISM that is able to assist converter to analyze and design circuit.
Introduction on hardware and equipment of teaching aid	Thoroughly introduces the working principle of each circuit and way to operate the equipment of the teaching aid.
Experiment 1 Unipolar voltage switching SPWM	Learns the switch theory of unipolar voltage SPWM, the measuring method of voltage and current for open loop of inverter module, the pin setting of TI F28335 DSP IC, the A/D and PWM module settings of DSP, the DSP internal signal monitoring by RS232, etc.
Experiment 2 Stand alone inverter with dual loop inductor current control	Learns the modularization of single-phase full bridge inverter, the controller design of current loop and voltage loop, the RMS voltage loop design, the inverter hardware layout, the SimCoder programming, etc.
Experiment 3 Grid connected single-phase inverter	Learns the method of phase-lock loop of grid connected single-phase inverter, the controller design of current loop and voltage loop, the hardware layout, the SimCoder programming, etc.

Experiment 4 Totem Pole Bridgeless PFC AC-DC converter	Learns the theory of Totem Pole Bridgeless PFC AC-DC converter, the controller design of current loop and voltage loop, the hardware layout, the SimCoder programming of PFC, etc.
Experiment 5 Full-bridge AC-DC switching rectifier	Learns the theory of Full-bridge AC-DC switching rectifier, the controller design of current loop and voltage loop, the hardware layout, the SimCoder programming, etc.

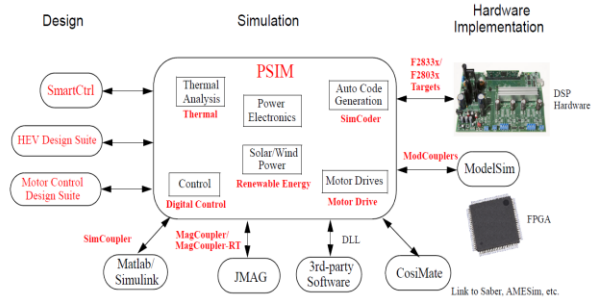
PSIM Introduction

PSIM, the simulating software specifically designed for diversified systems of electric and electronic, motor-driven as well power converter, has the following features: full functions, intact components, fast and precise simulation, user-friendly interface, etc. It is the most popular teaching and researching software in the international academic community and related industry. Therefore, this teaching aid, by adopting the software as platform, makes efforts in helping reader better sync with the international research and education.

PSIM, with abundantly all-directional features including simulation, design as well as hardware circuit realization, provides the functions as the figure 2.1 shown. In addition to the main frame that supplies simulation of electricity, electron and circuit, the following modules are included.

Figure 2.1

Simulation provided by PSIM



Motor Driver Module	It includes DC motor, brushless DC motor, squirrel-cage rotor, wound-rotor motor, permanent-magnet synchronous motor, synchronous motor, switched reluctance motor, various feedback circuit devices for speed, location and torque, different mechanical loads and drive source devices that can be utilized as various motors and generators for simulation in application systems.
Digital Control Module	It includes several discrete components like zero-order hold, z-domain transfer function, digital filter, quantization blocks, etc, all of which are components that can execute digital control and analysis.
SimCoupler Module	It can be used to be the interface of PSIM and Simulink that empowers Co-simulation for PSIM and Simulink, while allowing the user of Simulink to use the original technology. In addition, due to the advancements in simulating speed and convergence by adopting PSIM, it empowers the user of PSIM to make use of abundant Toolbox functions of Matlab via Simulink.
Thermal Module	It provides the module with actual power semiconductor component characteristics that is able to calculate the loss of power of semiconductor component for measuring temperature rise and reference on radiator mechanism design. User is able to construct power semiconductor component with Thermal in accordance with the data manual of actual component.
Renewable Energy Module	It contains Photovoltaics module, wind turbine and battery module.

SimCoder Module	It automatically converts control circuit into C program, and executes burning, via TI Composer, for DSP chip. Also, it offers a platform for interaction between hardware and firmware engineers through PSIM to build a specific field of closely tight cooperation.
F2833X Target	It contains the element database of TI DSP F2833X, which automatically generates program for burning F2833X.
F2803X Target	It contains the element database of TI DSP F2803X, which automatically generates program for burning F2803X.
MagCoupler Module	It offers the interface for PSIM and magnetic circuit analysis software JMAG and further links the above 2 for Co-simulation.
MagCoupler-RT	It provides link of data files for PSIM and magnetic circuit analysis software JMAG.
ModCoupler Module	It offers the interface of PSIM and ModelSim and further links the 2 for Co-simulation. 2 versions are available: ModCoupler-VHDL supporting VHDL program and ModCoupler-Verilog supporting Verilog program.
HEV Design Suite	It has some templates providing assistant design for power train system of HEV.
Motor Control Design Suite	It has some templates providing assistant design for induction motor, linear and non-linear permanent-magnet synchronous motor actuator.

In addition, PSIM offers user link with CosiMate, through which co-simulation can be realized with various software including Matlab/Simulink, ModelSim, Saber (from Synopsys), Easy5 and Adams (from MSCSoftware), Inventor (from Autodesk), AMESim (from LMS), GT-Power (from Gamma Technologies), etc. For more details, refer to the website link www.chiastek.com.

Teaching Aid Hardware & Equipment Introduction

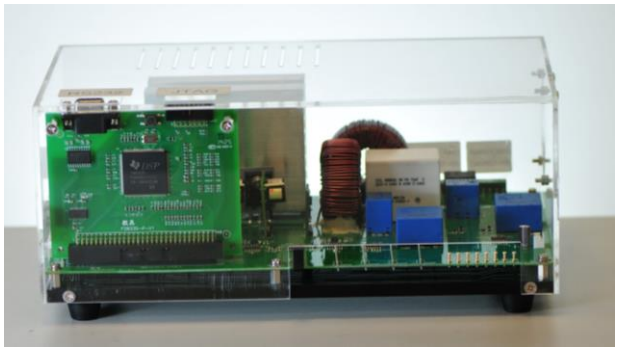
The teaching aid is a single-phase inverter and the input device is GW PSW 250-4.5 360W with the input voltage ranging from 60V to 200V. The output device is GW GPL-100 available for rectified load or resistive load. GW GPM-8212 is responsible for measuring output power, and GW GDS-2304A is the main oscilloscope. Also, we utilize GW APS-7050 to simulate grid connected electricity in the parallel experiment.

Power Circuit

The physical appearance of teaching aid is shown as the figure 3.1, and the circuit is shown as the figure 3.2. For safety concern, the input voltage is limited at 70V in case of critical issue from users unfamiliar with the circuit operation. There is a 5A fuse in the forefront of input terminal of inverter followed by a 330uF/450V input electrolytic capacitor, and a full-bridge inverter consisting of 4 MOS follows behind, for which the later part will further elaborate. Also, a second order low-pass filter composed of L-C (inductance: 661.5uH, capacitance: 10uF/400V) switches output, in accord with high frequency of attenuator inverter, to generate low frequency sine wave for output voltage with the RMS value 40V.

Figure 3.1

Single-phase Inverter Experiment Module



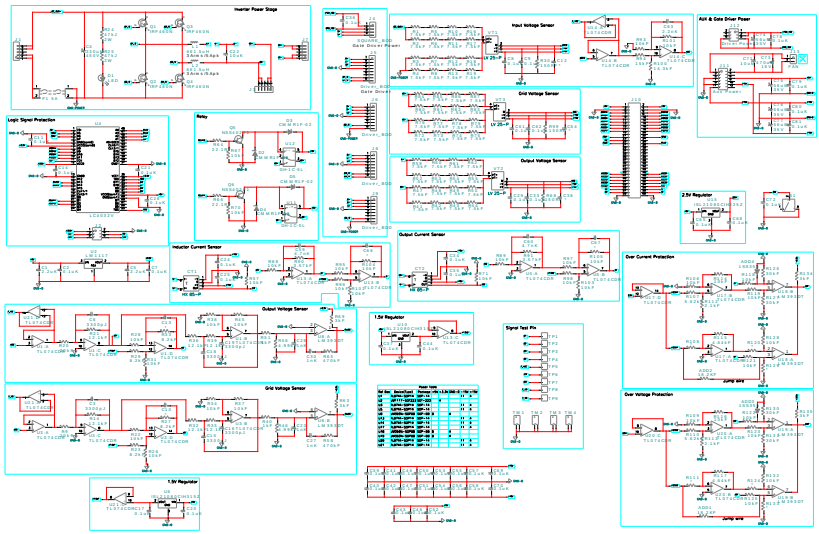


Figure 3.2 Single-phase Inverter Circuit Diagram

In the control and feedback circuit, the five parameters (input voltage (V_{DC}), output voltage (V_0), output current (I_0), inductor current (I_L) and grid connected electricity voltage (V_S)) will be sampled before sent to DSP. The sample process before sent to DSP will be further illustrated in-depth in the following section.

1. The sample process of input voltage is excerpted as the figure 3.2 shown. Refer to the figure 3.3, the input voltage, after routing 16 resistors and attenuating by 1/30k times, is sent to the sampled IC with model name LEM LV 25-P. The IC magnifies the voltage by 2.5 times followed by timing 150Ω to produce the VDCS signal. It will be then sent to DSP after passing through the OP magnifier with the amplification of 0.976 times. The sampled attenuated ratio is shown as the figure 3.1.

$$Gain = \frac{1}{30k} \times 2.5 \times 150 \times 0.976 = 1.22 \times 10^{-2} \qquad (3.1)$$

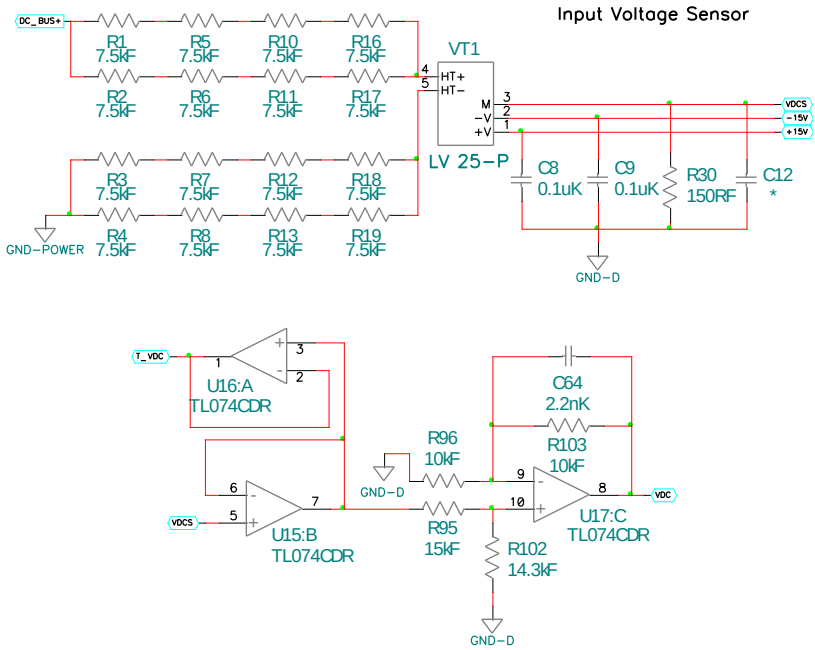


Figure 3.3 Input voltage sampled circuit

The sample process of output voltage is excerpted as the figure 3.2 shown. Refer to the figure 3.4, the output voltage, after routing 16 resistors and attenuating by 1/30k times, is sent to the sampled IC with model name LEM LV 25-P. The IC magnifies the voltage by 2.5 times followed by timing 150Ω. It will be then sent to DSP after passing through the OP magnifier with the amplification of 0.496 times. The sampled attenuated ratio is shown as the figure 3.2. Due to the fact that the output voltage is alternative signal, and the signal to sent to DSP must be within 0 ~ 3V, it is necessary to add a 1.5V level to comply with the requirement, which happens to the pin 12 of U1.

$$Gain = \frac{1}{30k} \times 2.5 \times 150 \times 0.496 = 6.2 \times 10^{-3} \qquad (3.2)$$

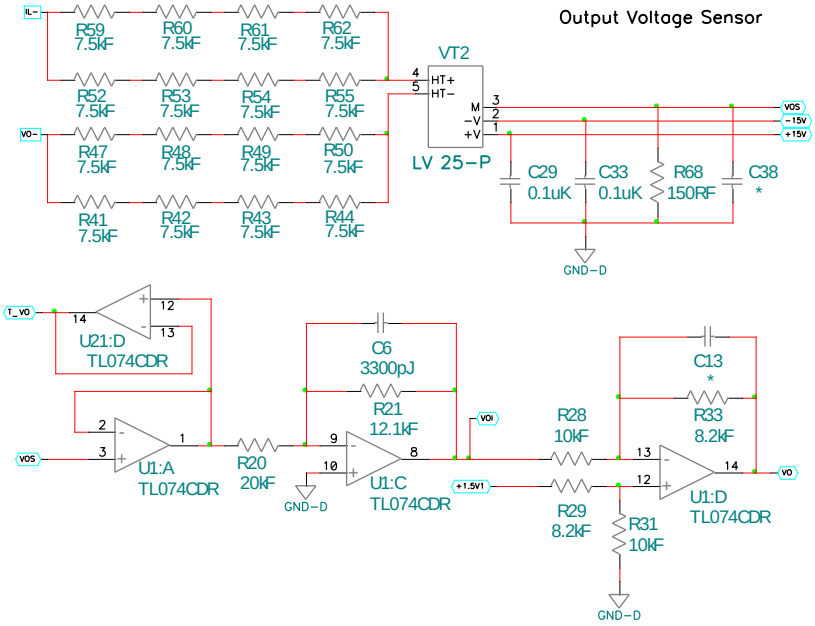


Figure 3.4 output voltage sampled circuit

2. The sample process of output current is excerpted as the figure 3.2 shown. Refer to the figure 3.5, the output current passes through the current sensor IC LEM HX 05-P with the conversion ratio 8×10^{-5} times. It will be then multiplied by 10kΩ followed by routing through the OP magnifier with 0.357 amplification to be sent to DSP. The sampled attenuated ratio is shown as the figure 3.3. Due to the fact that the output current is alternative signal, and the signal to sent to DSP must be within 0 ~ 3V, it is necessary to add a 1.5V level to comply with the requirement, which happens to the pin 5 of U5. $Gain = (8\times10^{-5})\times10k\times0.357 = 0.286$ (3.3)

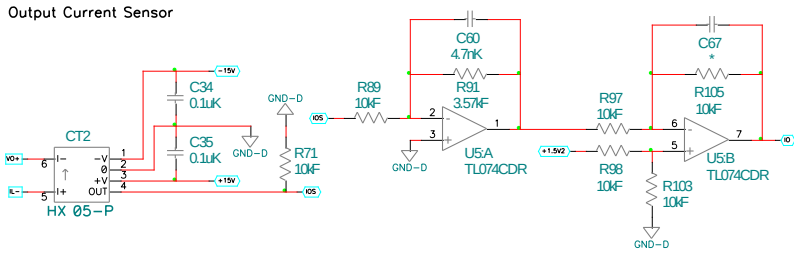


Figure 3.5 output current sampled circuit

The sample process of inductor current is excerpted as the figure 3.2 shown. Refer to the figure 3.6, the inductance capacitance passes through the current sensor IC LEM HX 05-P with the conversion ratio 8×10-5 times. It will be then multiplied by 10kΩ followed by routing through the OP magnifier with the amplification of 0.36 to be sent to DSP. The sampled attenuated ratio is shown as the figure 3.4. Due to the fact that the inductor current is alternative signal, and the signal to sent to DSP must be within 0 ~ 3V, it is necessary to add a 1.5V level to comply with the requirement, which happens to the pin 5 of U13.

$$Gain = (8 \times 10^{-5}) \times 10k \times 0.36 = 0.288 \qquad (3.4)$$

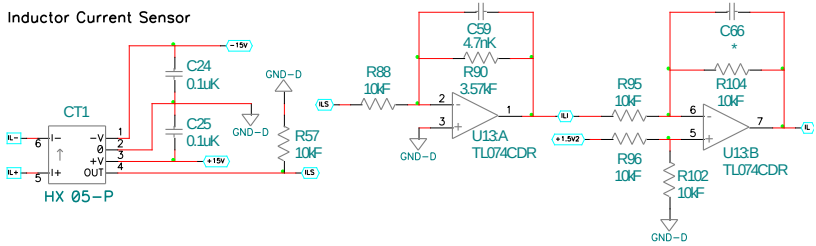


Figure 3.6 Inductor current sampled circuit

The sample process of grid connected electricity voltage is excerpted as the figure 3.2 shown. Refer to the figure 3.7, the grid connected electricity voltage, after routing 16 resistors and attenuating by 1/30k times, is sent to the sampled IC with model name LEM LV 25-P. The IC magnifies the voltage by 2.5 times followed by timing 150Ω. It will be then sent to DSP after passing through the OP magnifier with 0.496 amplification. The sampled attenuated ratio is shown as the figure 3.5. Due to the fact that the grid connected electricity voltage is alternative signal, and the signal to sent to DSP must be within 0 ~ 3V, it is necessary to add a 1.5V level to comply with the requirement, which happens to the pin 12 of U3.

$$Gain = \frac{1}{30k} \times 2.5 \times 150 \times 0.496 = 6.2 \times 10^{-3} \qquad (3.5)$$

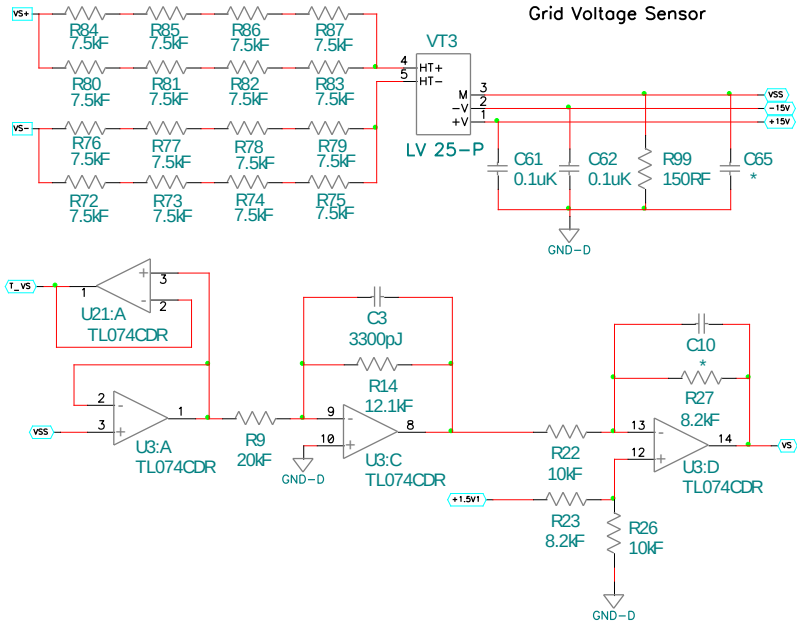


Figure 3.7 Grid connected electricity voltage sampled circuit

In general, hardware circuit has the built-in OV (Over Voltage) and OC (Over Current) Protection design with the normality of high level. Once either voltage or current is beyond the limit, output will switch to low level to trigger the protection mechanism which forces inverter to stop operation at once in case of damage. Refer to the figure 3.8 for the circuit.

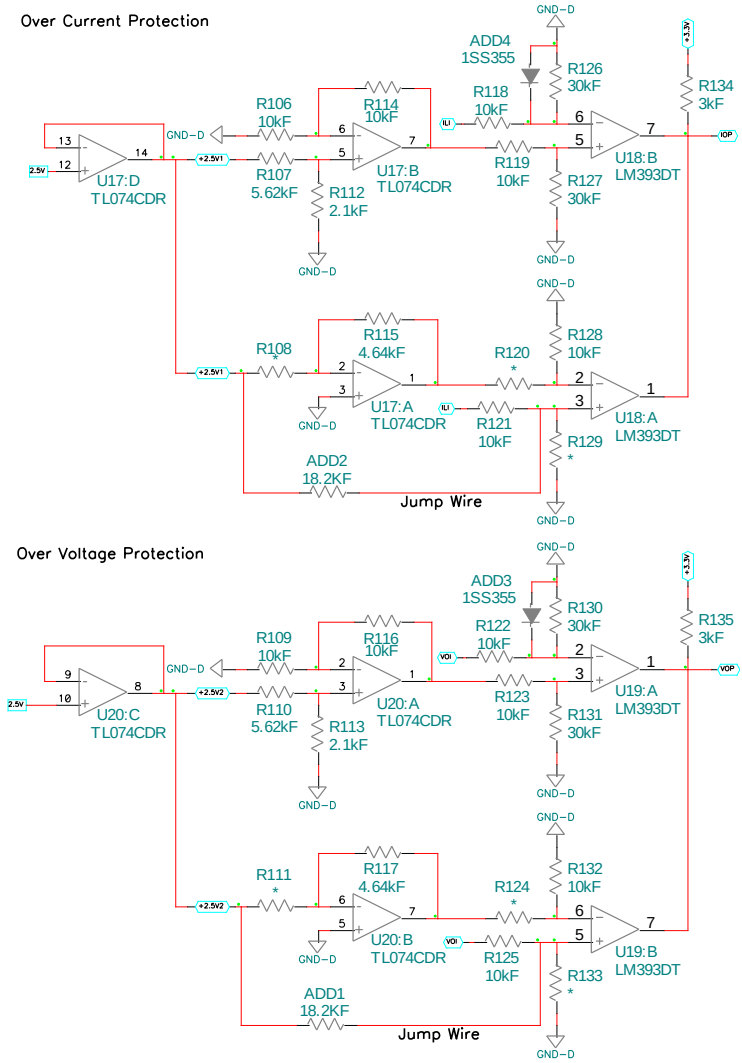


Figure 3.8 Over voltage and over current protection circuit

Single-phased inverter teaching aid provides the following test points for users to measure:

1. DSP sends PWM1 ~ PWM4 to CPLD LC4032V before obtaining signal Q1 ~ Q4. It will then pass through the drive circuit to drive MOS, and the signal Q1 ~ Q4 can be measured from the measuring point.

2. Input voltage (VDC), after routing 16 resistors and attenuating by 1/30k times, is sent to the sampled IC. The IC magnifies the voltage by 2.5 times followed by timing 150Ω to generate the exactly measuring value of measuring point. The attenuated ratio is shown as the figure 3.6.

$$Gain = \frac{1}{30k} \times 2.5 \times 150 = 0.0125 \quad (3.6)$$

3. Inductor current (IL) passes through the current sensor with the conversion ratio 8×10^{-5} times. It will be then multiplied by 10kΩ to generate the exactly measuring value of measuring point. The attenuated ratio is shown as the figure 3.7. $Gain = (8\times10^{-5}) \times 10k = 0.8$ (3.7)

4. Output current (I0) passes through the current sensor with the conversion ratio 8×10^{-5} times. It will be then multiplied by 10kΩ to generate the exactly measuring value of measuring point. The attenuated ratio is shown as the figure 3.8.

$$Gain = (8\times10^{-5}) \times 10k = 0.8 \quad (3.8)$$

5. Output voltage (V_0), after routing 16 resistors and attenuating by 1/30k times, is sent to the sampled IC. The IC magnifies the voltage by 2.5 times followed by timing 150Ω to generate the exactly measuring value of measuring point. The attenuated ratio is shown as the figure 3.9.

$$Gain = \frac{1}{30k} \times 2.5 \times 150 = 0.0125 \quad (3.9)$$

6. Grid connected electricity voltage (Vs), after routing 16 resistors and attenuating by 1/30k times, is sent to the sampled IC. The IC magnifies the voltage by 2.5 times followed by timing 150Ω to generate the exactly measuring value of measuring point. The attenuated ratio is shown as the figure 3.10.

$$Gain = \frac{1}{30k} \times 2.5 \times 150 = 0.0125 \quad (3.10)$$

DSP Control Circuit

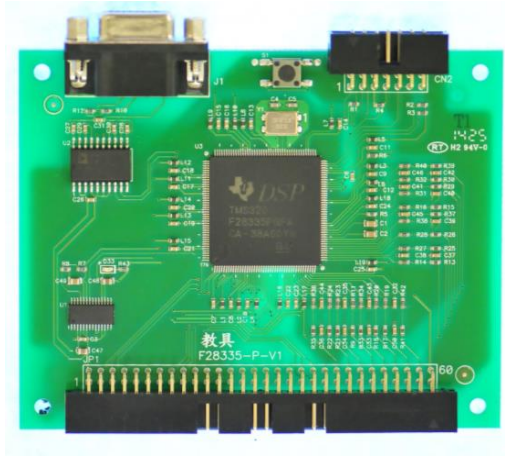
DSP control circuit is the hardware based on the TI TMS320F28335 (check figure 3.9 and 3.10 for the circuit diagram) to supply, via dual output regulator IC, 3.3V, the 28335 IC working power, and 1.8V. Before sent into DSP, the signal passes through the diode clamp circuit to ensure the voltage sent to IC is within 0 ~ 3V in case of damage to DSP. Through the isolated RS232 interface, it is available to sent DSP internal signal back to the oscilloscope of PSIM for observation. The output definition of each pin on control panel is well explained in the table below.

	Pin		
+5V in	1	2	+5V in
GND	3	4	GND
GPIO-00 / EPWM-1A	5	6	GPIO-01 / EPWM-1B / MFSR-B
GPIO-02 / EPWM-2A	7	8	GPIO-03 / EPWM-2B / MCLKR-B
GPIO-04 / EPWM-3A	9	10	GPIO-05 / EPWM-3B / MFSR-A / ECAP-1
GPIO-06 / EPWM-4A / SYNCI / SYNCO	11	12	GPIO-07 / EPWM-4B / MCLKR-A / ECAP-2
GPIO-08 / EPWM-5A / CANTX-B / ADCSOC-A	13	14	GPIO-09 / EPWM-5B / SCITX-B / ECAP-3
GPIO-10 / EPWM-6A / CANRX-B / ADCSOC-B	15	16	GPIO-11 / EPWM-6B / SCIRX-B / ECAP-4
GPIO-48 / ECAP5 / XD31 (EMIF)	17	18	GPIO-49 / ECAP6 / XD30 (EMIF)
GPIO-50	19	20	GPIO-51
GPIO-12 / TZ1n / CANTX-B / MDX-B	21	22	GPIO-13 / TZ2n / CANRX-B / MDR-B
GPIO-15 / TZ4n / SCIRX-B / MFSX-B	23	24	GPIO-14 / TZ3n / SCITX-B / MCLKX-B
GPIO-24 / ECAP1 / EQEPA-2 / MDX-B	25	26	GPIO-25 / ECAP2 / EQEPB-2 / MDR-B
GPIO-26 / ECAP3 / EQEPI-2 / MCLKX-B	27	28	GPIO-27 / ECAP4 / EQEPS-2 / MFSX-B
GPIO-16 / SPISIMO-A /	29	30	GPIO-17 / SPISOMI-A / CANRX-

CANTX-B / TZ-5			B / TZ-6
GPIO-18 / SPICLK-A / SCITX-B	31	32	GPIO-19 / SPISTE-A / SCIRX-B
GPIO-20 / EQEP1A / MDX-A / CANTX-B	33	34	GPIO-21/ EQEP1B/ MDR-A/ CANRX-B
GPIO-22 / EQEP1S / MCLKX-A / SCITX-B	35	36	GPIO-23/ EQEP1I/ MFSX-A / SCIRX-B
GPIO-28 / SCIRX-A / -- / TZ5	37	38	GPIO-29 / SCITX-A / -- / TZ6
GPIO-30 / CANRX-A	39	40	GPIO-31 / CANTX-A
GPIO-32 / I2CSDA / SYNCI / ADCSOCA	41	42	GPIO-33 / I2CSCL / SYNCO / ADCSOCB
ADCIN-B7	43	44	ADCIN-A7
ADCIN-B6	45	46	ADCIN-A6
ADCIN-B5	47	48	ADCIN-A5
ADCIN-B4	49	50	ADCIN-A4
ADCIN-B3	51	52	ADCIN-A3
ADCIN-B2	53	54	ADCIN-A2
ADCIN-B1	55	56	ADCIN-A1
ADCIN-B0	57	58	ADCIN-A0
GND	59	60	GND

Figure 3.9

DSP control circuit



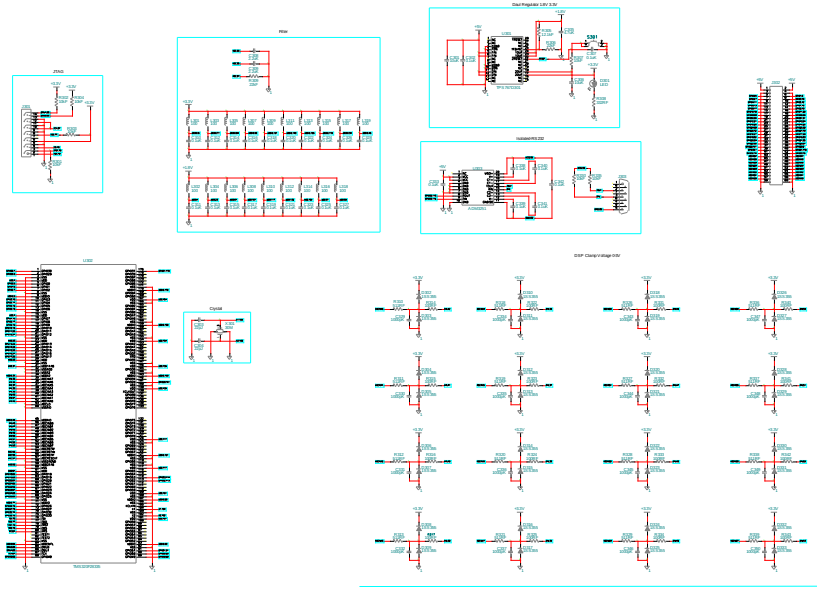


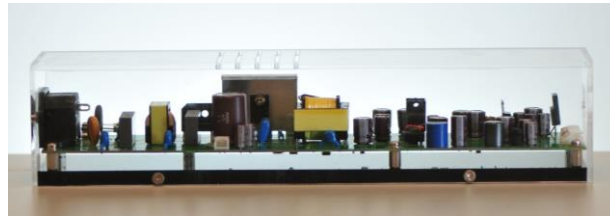
Figure 3.10 F28335 circuit diagram

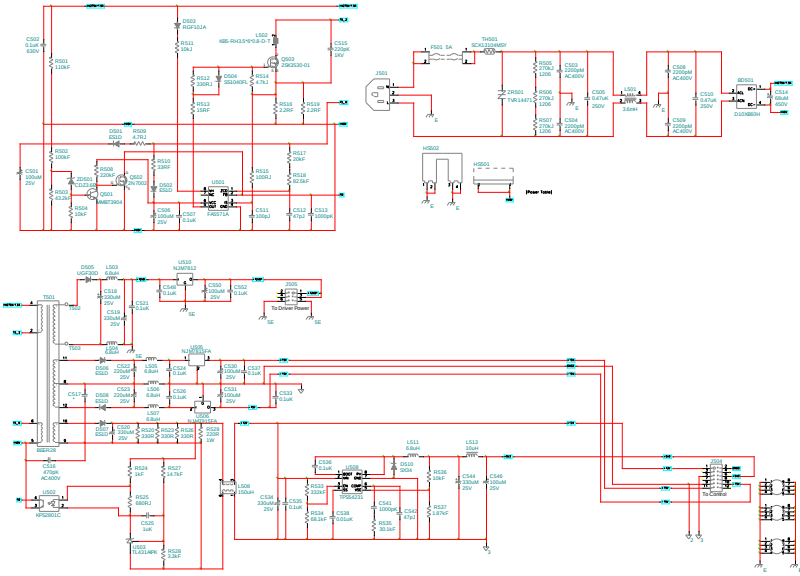
Auxiliary Power

Based on the layout design of Flyback, this module has input voltage from 100 ~ 250V, and 3 groups of isolated power, which is (1)12V, (2)12V, 5V (3)15V, -15V respectively. Refer to the figure 3.11 for physical appearance and figure 3.12 for circuit diagram.

Figure 3.11

Auxiliary power





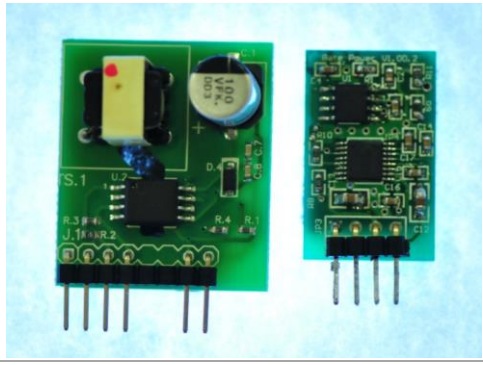
3.12 Auxiliary power circuit

Drive Circuit

Drive power module, which consists of Gate Driver board and Gate Driver Power board, provides multiple isolated powers. Refer to the figure 3.13 for Gate Driver (left) and Gate Driver Power (right). Also refer to the figures 3.14 and 3.15 for circuit diagrams. Inputting the 12V voltage to Gate Driver Power generates the output of ±12V square wave. The ±12V square wave along with the PWM signal generated by DSP, via the input of Gate Driver, will output the signal of drive MOS. Gate Driver meets the objective of isolation through inverter and optical coupling driver IC.

Figure 3.13

Circuit drive circuit module



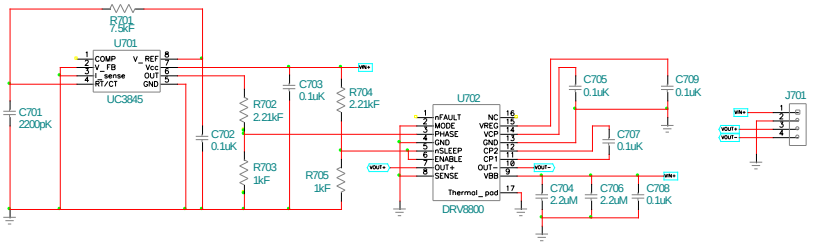


Figure 3.14 Gate Drive Power circuit diagram

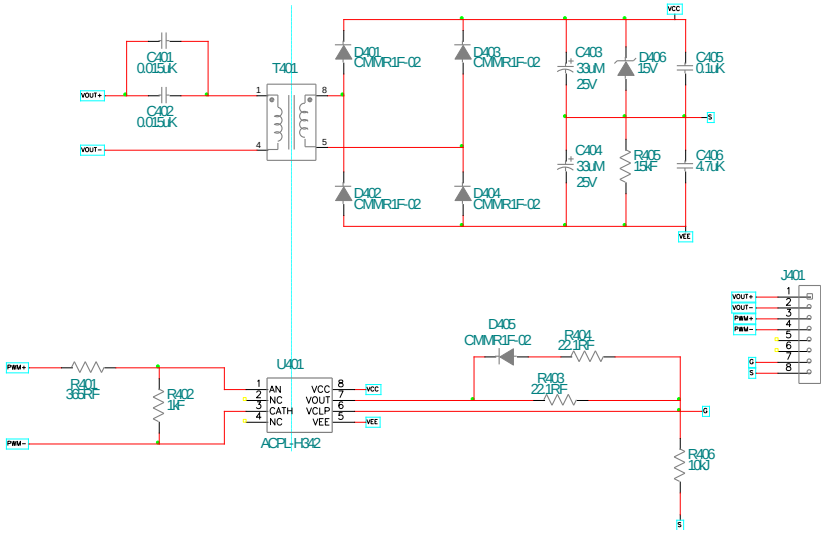


Figure 3.15 Gate Drive circuit diagram

JTAG Burning Circuit

The module helps burning program from PC to DSP chip. Refer to the figure 3.16 for hardware circuit and 3.17 for the circuit diagram. Connect USB to PC, and JTAG to DSP port individually.

Figure 3.16

USB_JTAG burning circuit

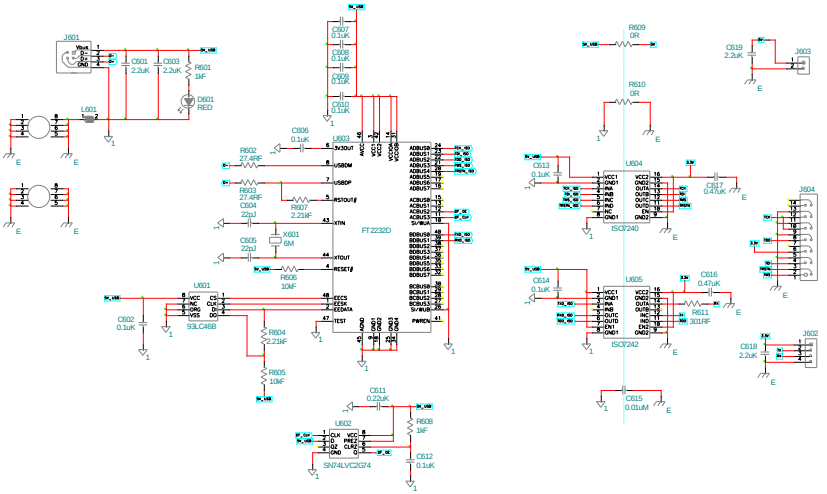


Figure 3.17 USB_JTAG circuit

Experiment 1: Unipolar voltage switching PWM

The purpose of experiment

- Learn the principle of switch for Sinusoidal PWM (SPWM)
- The voltage and current measuring method for open loop of inverter module
- The pin setting of TI F28335 DSP IC
- The setting of PWM and A/D module for DSP
- The method of monitoring DSP internal signal by RS232
- Get familiar with the hardware circuit operation from this experiment

The principle of experiment

The principle of Sinusoidal PWM (SPWM) inverter

As the figure 4.1 shown, the single-phase full bridge inverter has the switch control that is based on trigger signal of switch, known as sinusoidal PWM (SPWM), from comparison between a low-frequency sine wave ($V_{control}$) and a high-frequency triangle wave (V_{tri}). L-C forms a 2-level low pass filter, which is used to attenuate high-frequency switch item from inverter output, to turn the output voltage into low-frequency sine wave. AC load can be divided into 2 parts: linear and non-linear load, in which linear load includes resistive (voltage and current same-phase), inductive (current phase lagging voltage) and capacitive (current phase leading voltage), while non-linear load contains rectified load of current distortion.

To provide the aforementioned loads, inverter output is supposed to be with the functionality of 4 quadrants; the classic load is the output voltage and current wave form (figure 4.2 (a)) of inductive inverter which passes through 4-quadrants operation simultaneously within an alternative cycle.

With the 4-quadrants operability, bridge converter is the most popular circuit architecture for inverter. The definition of power flow direction of single-phase full bridge inverter is highlighted as the arrow within figure 4.1; the power of 1st and 3rd quadrants is P_o>0, known as inverter mode, whilst the power of 2nd and 4th quadrants is P_o< 0, known as rectifier mode. Although 4 quadrants have been passed through within a single cycle in terms of the instantaneous power, power keeps in and out constantly. On the basis of average power, however, the inverter mode (figure 4.2(a)) is active when current lags behind voltage by the angle < 90 degree, whilst rectifier mode is active when current lags behind voltage by the angle > 90 degree.

The switch of full bridge inverter (figure 4.2(b)) has up to 8 conduction modes. For instance, P_o>0 is in operation under the I quadrant of v_o-i_o plane where output voltage and current are positive when the switch of diagonal (T_{A+}, T_{B-}) is conducted; P_o<0 is

in operation under the IV quadrant where output voltage is positive but negative for current when the diode of diagonal (D_{A+}, D_{B-}) is conducted; P_o >0 is in operation under the III quadrant where output voltage and current are negative when the switch of diagonal (T_{A-}, T_{B+}) is conducted; P_o <0 is in operation under the II quadrant where output voltage is negative but positive for current when the diode of diagonal (D_{A-}, D_{B+})is conducted. In addition, the flyback conduction mode of the 4 output short-circuit (v_o = 0) is the so-called 4 conduction modes indicated within the i_o axis including the (T_{A+}, D_{B+}) and (D_{A-}, T_{B-}) when i_o current is positive and the (T_{A-}, D_{B-}) and (D_{A+}, T_{B+}) when i_o current is negative.

In respect to single-phase inverter, SPWM can be separated into 2 ways: Bipolar-voltage switching and Unipolar-voltage switching. The details are explained below.

A. Bipolar-voltage switching

The comparison method of bipolar-voltage switching is illustrated as the figure 4.3(a). The switch of diagonal of full bridge circuit is paired trigger. The trigger signal of switch within same arm is complementary but requires a Dead-time to add in case of simultaneous conduction at the time of instantaneous switch changing.

Duty cycle of switch is determined by the comparison between control voltage $v_{control}$ and periodic sawtooth wave v_{tri}. When $v_{control}$ > v_{tri}, (T_{A+}, T_{B-}) is triggered; non i_o direction forces A arm connected to high level (i_o >0 through T_{A+}, v_o <0 through D_{A+}), and B arm is connected to low level (i_o >0 through T_{B-}, i_o <0 through D_{B-}); therefore v_o = V_d. On the contrary, (T_{A-}, T_{B+}) is triggered when $v_{control}$ < v_{tri},; regardless of direction of i_o, A arm is connected to low level, whilst B arm is connected to high level; therefore i_o =-V_d. The figure 4.3(b) indicates the output waveform of inverter where v_o switches between 2 levels: +V_d and -V_d, and thus it is called Bipolar-voltage switching.

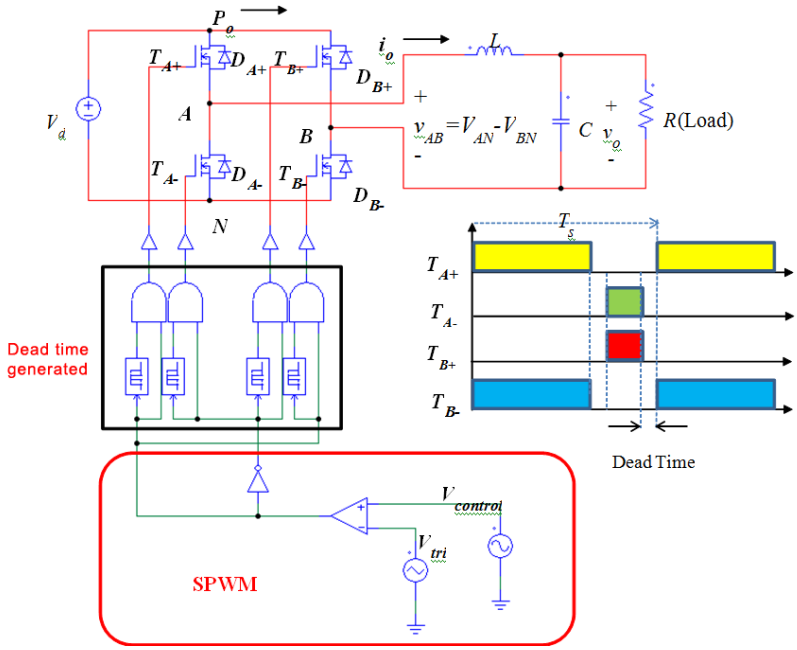
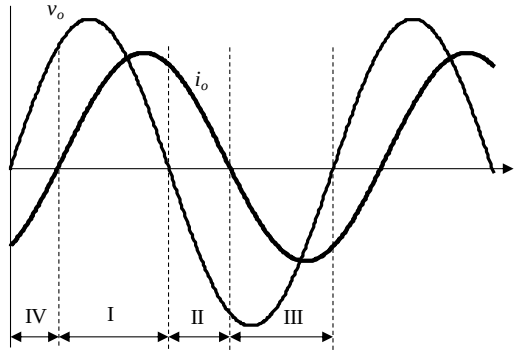


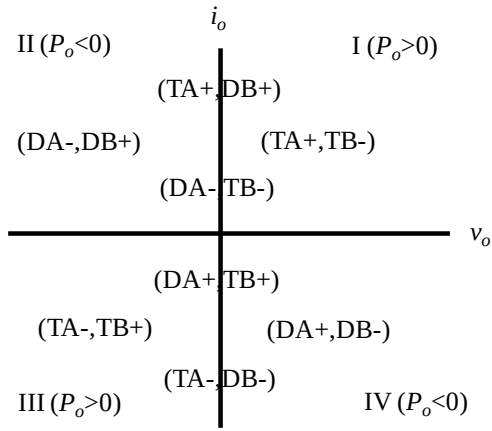
Figure 4.1 Single-phase full bridge inverter with bipolar-voltage switching

Figure 4.2

The output waveform and component conduction of full bridge converter



(a) The output voltage and current waveform of inductive load



(b) The 8 conduction modes of full bridge inverter

2 parameters can be defined by SPWM:

Amplitude modulation index

$$m_a = \frac{\hat{v}_{control}}{\hat{v}_{tri}} \tag{4.1}$$

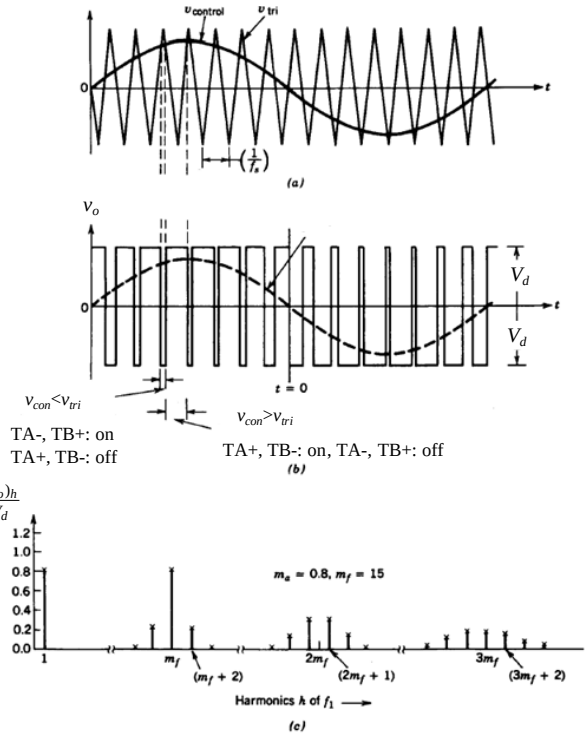
Frequency modulation index

$$m_f = \frac{f_s}{f_1} \tag{4.2}$$

From the abovementioned, $\hat{v}_{control}$ and $\hat{v}_{tri}$ are control voltage and amplitude of triangle wave individually, while f_1 and f_s are control voltage and frequency of triangular wave respectively. The spectrum of output voltage v_o is shown as the figure 4.3(c) where the size of basic wave is directly proportional to ma, whilst the rest harmonic waves appear right in or close to the integral multiples to mf .

Figure 4.3

Bipolar-voltage switching



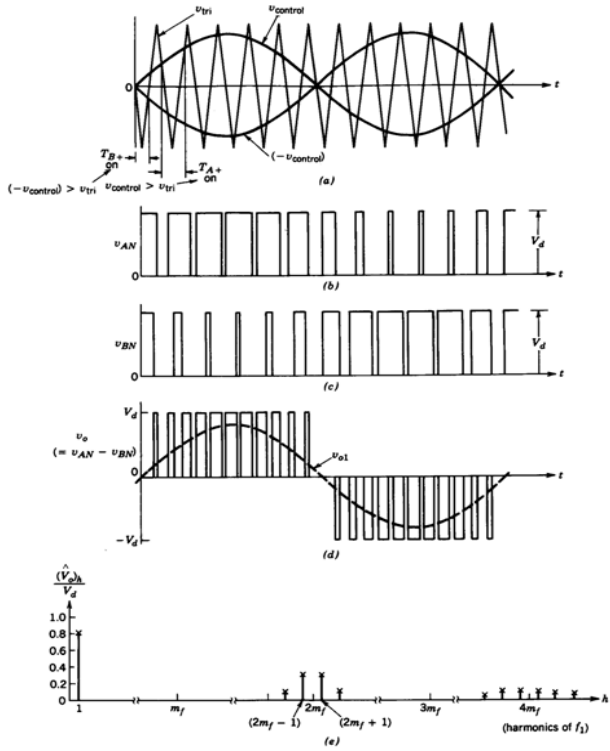
B. Unipolar voltage switching

The comparison method of unipolar-voltage switching is illustrated as the figure 4.4(a) where the control voltage of A and B arms individually compare with triangle wave, and trigger signal of switch within same arm is complementary. The 2 control voltages are inverting: $v_{controlA} = +v_{control}$, $v_{controlB} = -v_{control}$. The output waveform of inverter from the previous comparison is illustrated as the figure 4.4(b) where Vo switches between $+V_d$ and 0 or $-V_d$ and 0 level and thus being called unipolar voltage switching which utilizes 8 conduction modes with flyback mode included as the figure 4.2 shown. The spectrum of output voltage v_o is shown as the figure 4.4(c) where the size of basic wave is directly proportional to ma, whilst the rest harmonic waves appear right in $2m_f$ or close to the integral multiples to $2m_f$. Compared with output of bipolar voltage switching, the size of basic wave is identical but with equivalently twice switching frequency and lower voltage

fluctuation. More compact LC filter component is acceptable and therefore unipolar voltage switching is easily adoptable for most of the cases.

Figure 4.4

Unipolar voltage switching



The relation between output voltage basic wave of single-phase SPWM inverter and m_a is illustrated as the figure 4.5 where m_a <1 is called linear zone and output voltage basic wave is directly proportional to ma.

1< m_a <3.24 is called over-modulation area where the amplitude of output voltage basic wave ($\frac{(\hat{v}_o)_1}{V_d}$) is beyond 1.

m_a >3.24 is called square wave area in that output voltage results in square waveform with the amplitude of basic wave as $\frac{(\hat{v}_o)_1}{V_d} = 4/\pi$.

As the figure 4.6 shown, output voltage under over-modulation area (1< m_a <3.24) will be low-frequency harmonic wave, which is

forbidden for inverter of general sine wave output because it will cause critical distortion for output voltage. Nevertheless, for motor drives, over-modulation and operation of square wave area are highly adopted due to higher torque garnered from higher basic wave, which is helpful for momentarily heavy load and startup for motor. For pulsating torque resulted from low-frequency harmonic wave, the characteristics of mechanically low-frequency filter can greatly overcome by reducing vibrations and noises.

Figure 4.5

The relation between output voltage basic wave of single-phase SPWM inverter and ma

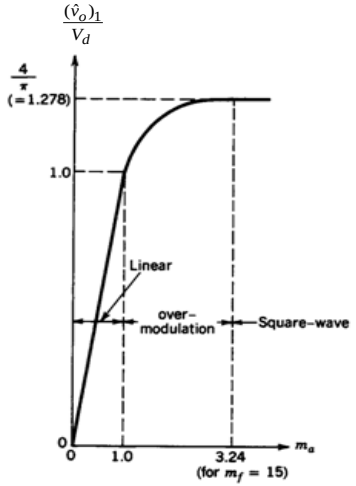
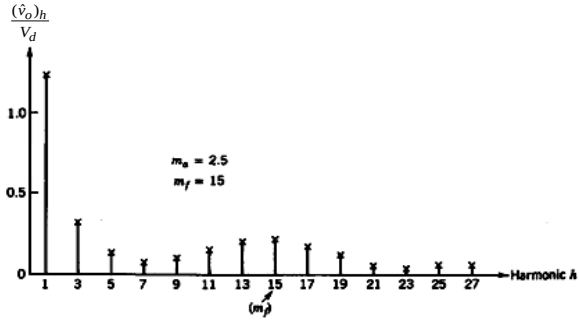


Figure 4.6

The spectrum of output voltage harmonic wave of single-phase SPWM inverter ma>1



Circuit Simulation

The circuit parameters of inverter are as follows:

V_d =70V, V_{tri} =5Vpp/18kHz, L=661.5mH*2, C=10μF, R=14Ω

V_{conA}, V_{conB} =2.4Vp/60Hz

The simulating circuit utilizing unipolar voltage switching is illustrated as the figure 4.7, and the result of simulation is shown as the figure 4.8.

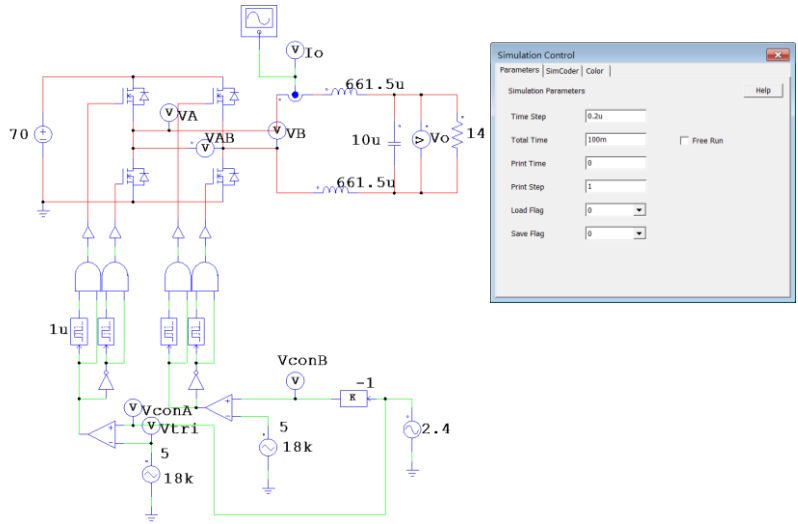


Figure 4.7 The simulating circuit utilizing unipolar voltage switching

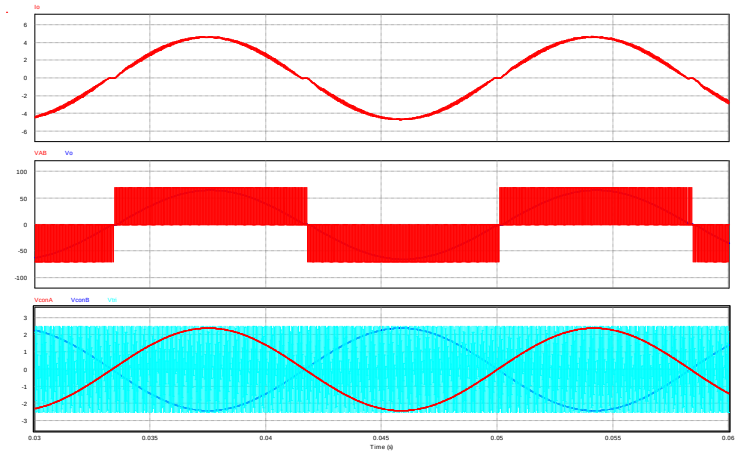


Figure 4.8 The result of simulation by utilizing unipolar voltage switching from the figure 4.7

SimCoder Program Layout

Based on the simulating circuit of analog unipolar voltage switching indicated in the figure 4.7, the SimCoder circuit layout of control circuit (figure 4.9) is realized by TI F28335, and the gain hardware setting of sense circuit is as follows:

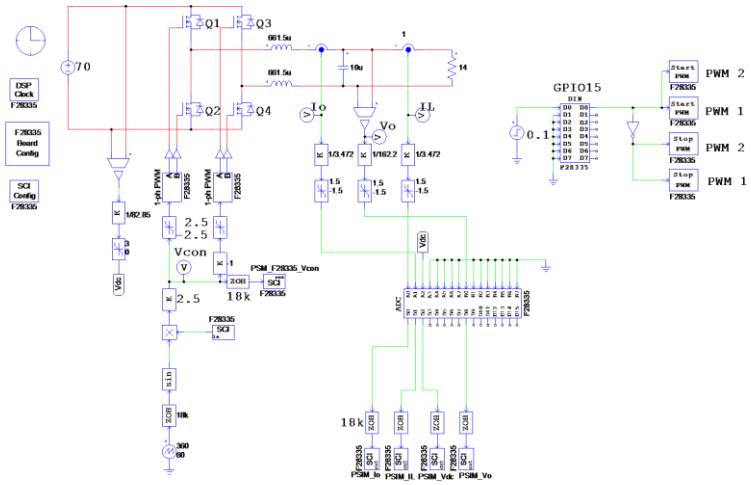
Current sense gain K_s =1/3.472

Voltage sense gain K_v =1/162.2

Sense signal of voltage/current has to pass through a limiter, which forces input voltage clamped at ±1.5V, before entering the DSP A/D pin.

The above hardware circuit is merely for SimCoder simulation. Due to the fact that DSP of actual circuit only accepts 0~3V signal, the AC signal will be risen to 1.5V followed by 3V clamp to enter the A/D pin, which means DSP, originally 1.5V, will be regarded 0 to AC signal.

The setting of each component of SimCoder is as follows.



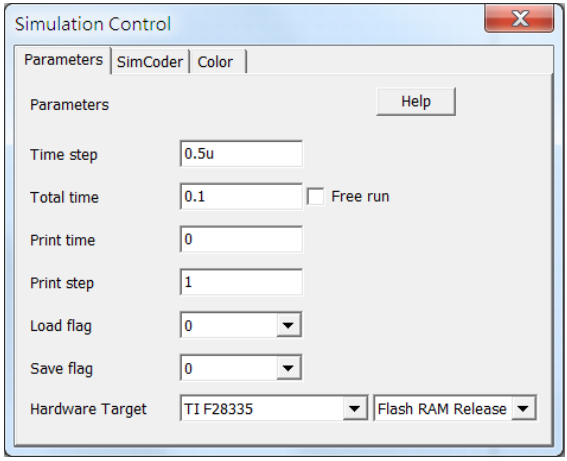
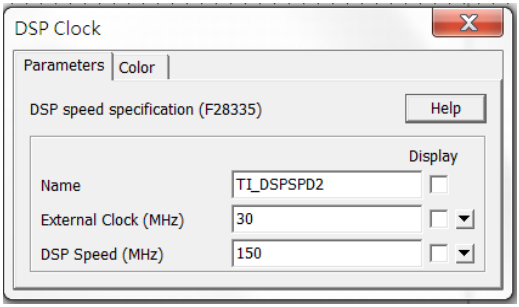


Figure 4.9 The SimCoder simulating circuit utilizing unipolar voltage switching

DSP Clock Setting

DSP Clock is available for external or built-in setting; external setting asks user to manually modify parameters of External Clock (default=30MHz), whilst built-in setting requests DSP speed 150MHz. The experiment adopts the built-in setting.



28335 Hardware Config

The hardware setting of this experiment DSP F28335 requires tick for each cell within the following table.

- 2 sets of PWM; A arm adopts PWM1(GPIO 0, GPIO 1), while B arm utilizes PWM2(GPIO 2, GPIO 3).
- Use a set of DI (Digital Input，GPIO 15), and PWM can be activated via external circuit.
- When circuit is active, use a set of serial communication (SCI C, GPIO62, 63) to send signal to computer through RS232-USB to monitor system status.

GPIO 0	Digital Input	Digital Output	V PWM		
GPIO 1	Digital Input	Digital Output	V PWM	Capture	
GPIO 2	Digital Input	Digital Output	V PWM		
GPIO 3	Digital Input	Digital Output	V PWM	Capture	
GPIO 4	Digital Input	Digital Output	PWM		
GPIO 5	Digital Input	Digital Output	PWM	Capture	
GPIO 6	Digital Input	Digital Output	PWM		
GPIO 7	Digital Input	Digital Output	PWM	Capture	
GPIO 8	Digital Input	Digital Output	PWM		
GPIO 9	Digital Input	Digital Output	PWM	Capture	Serial Port

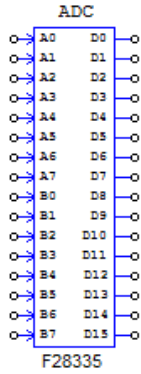
GPIO 10		Digital Input	Digital Output	PWM		
GPIO 11		Digital Input	Digital Output	PWM	Capture	Serial Port
GPIO 12		Digital Input	Digital Output	Trip-Zone		
GPIO 13		Digital Input	Digital Output	Trip-Zone		
GPIO 14		Digital Input	Digital Output	Trip-Zone	Serial Port	
GPIO 15	V	Digital Input	Digital Output	Trip-Zone	Serial Port	
GPIO 16		Digital Input	Digital Output	Trip-Zone	SPI	
GPIO 17		Digital Input	Digital Output	Trip-Zone	SPI	
GPIO 18		Digital Input	Digital Output	Serial Port	SPI	
GPIO 19		Digital Input	Digital Output	Serial Port	SPI	
GPIO 20		Digital Input	Digital Output	Encoder		
GPIO 21		Digital Input	Digital Output	Encoder		
GPIO 22		Digital Input	Digital Output	Encoder	Serial Port	
GPIO 23		Digital Input	Digital Output	Encoder	Serial Port	
GPIO 24		Digital Input	Digital Output	PWM	Capture	Encoder
GPIO 25		Digital Input	Digital Output	PWM	Capture	Encoder
GPIO 26		Digital Input	Digital Output	PWM	Capture	Encoder
GPIO 27		Digital Input	Digital Output	PWM	Capture	Encoder
GPIO 28		Digital Input	Digital Output	Serial Port		
GPIO 29		Digital Input	Digital Output	Serial Port		

GPIO 30	Digital Input	Digital Output		
GPIO 31	Digital Input	Digital Output		
GPIO 32	Digital Input	Digital Output		
GPIO 33	Digital Input	Digital Output		
GPIO 34	Digital Input	Digital Output	PWM	Capture
GPIO 35	Digital Input	Digital Output	Serial Port	
GPIO 36	Digital Input	Digital Output	Serial Port	
GPIO 37	Digital Input	Digital Output	PWM	Capture
GPIO 38	Digital Input	Digital Output		
GPIO 39	Digital Input	Digital Output		
GPIO 40	Digital Input	Digital Output		
GPIO 41	Digital Input	Digital Output		
GPIO 42	Digital Input	Digital Output		
GPIO 43	Digital Input	Digital Output		
GPIO 44	Digital Input	Digital Output		
GPIO 45	Digital Input	Digital Output		
GPIO 46	Digital Input	Digital Output		
GPIO 47	Digital Input	Digital Output		
GPIO 48	Digital Input	Digital Output	PWM	Capture
GPIO 49	Digital Input	Digital Output	PWM	Capture

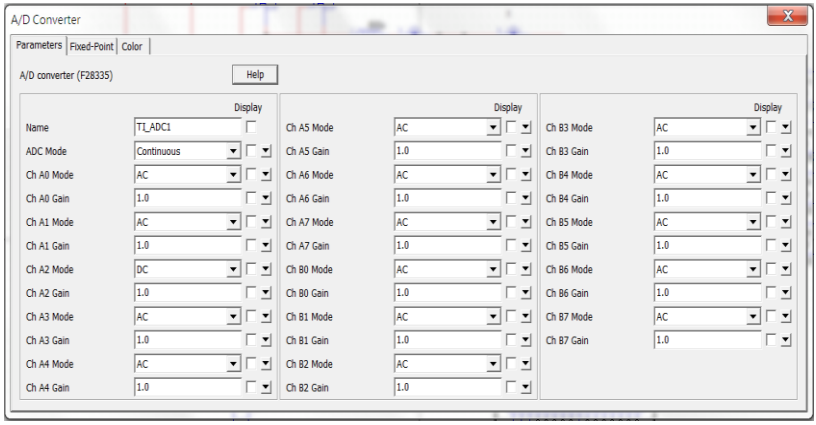
GPIO 50	Digital Input	Digital Output		Encoder	
GPIO 51	Digital Input	Digital Output		Encoder	
GPIO 52	Digital Input	Digital Output		Encoder	
GPIO 53	Digital Input	Digital Output		Encoder	
GPIO 54	Digital Input	Digital Output		SPI	
GPIO 55	Digital Input	Digital Output		SPI	
GPIO 56	Digital Input	Digital Output		SPI	
GPIO 57	Digital Input	Digital Output		SPI	
GPIO 58	Digital Input	Digital Output			
GPIO 59	Digital Input	Digital Output			
GPIO 60	Digital Input	Digital Output			
GPIO 61	Digital Input	Digital Output			
GPIO 62	Digital Input	Digital Output	V	Serial Port	
GPIO 63	Digital Input	Digital Output	V	Serial Port	
GPIO 64	Digital Input	Digital Output			
GPIO 65	Digital Input	Digital Output			
GPIO 66	Digital Input	Digital Output			
GPIO 67	Digital Input	Digital Output			
GPIO 68	Digital Input	Digital Output			
GPIO 69	Digital Input	Digital Output			

GPIO 70	Digital Input	Digital Output		
GPIO 71	Digital Input	Digital Output		
GPIO 72	Digital Input	Digital Output		
GPIO 73	Digital Input	Digital Output		
GPIO 74	Digital Input	Digital Output		
GPIO 75	Digital Input	Digital Output		
GPIO 76	Digital Input	Digital Output		
GPIO 77	Digital Input	Digital Output		
GPIO78	Digital Input	Digital Output		
GPIO 79	Digital Input	Digital Output		
GPIO 80	Digital Input	Digital Output		
GPIO 81	Digital Input	Digital Output		
GPIO 82	Digital Input	Digital Output		
GPIO 83	Digital Input	Digital Output		
GPIO 84	Digital Input	Digital Output		
GPIO 85	Digital Input	Digital Output		
GPIO 86	Digital Input	Digital Output		
GPIO 87	Digital Input	Digital Output		

AD Converter (ADC) Setting

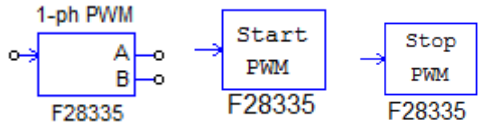


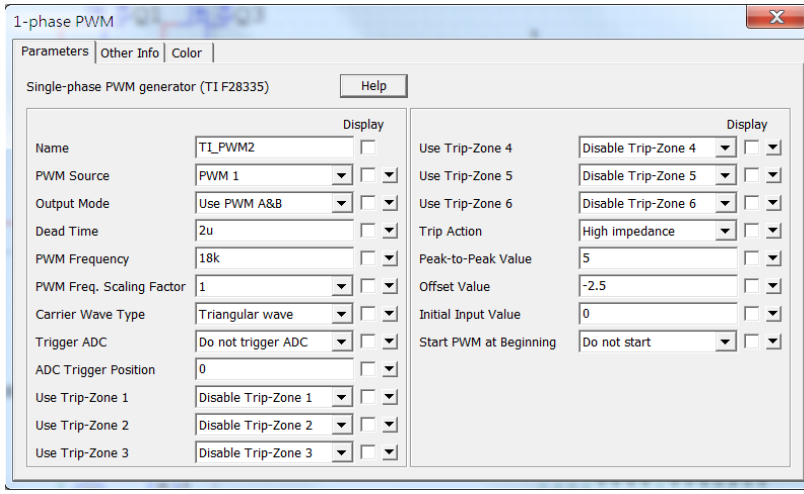
F28335 contains 16 groups of ADC, which can be divided into A0~A7 and B0~B7 channels, respectively. ADC module requires setting ADC sampling mode where Continuous sampling mode, input mode and Gain mode of each channel are necessary for setting. The experiment feedbacks 4 signals in total, which are load current (I_L, A0)), inductor current (I_0, A1)), input voltage (V_d, A2) and output voltage (V_0, B0), where only input voltage is defined as DC mode, whilst the rest 3 are AC mode. The gain of each ADC is set 1.



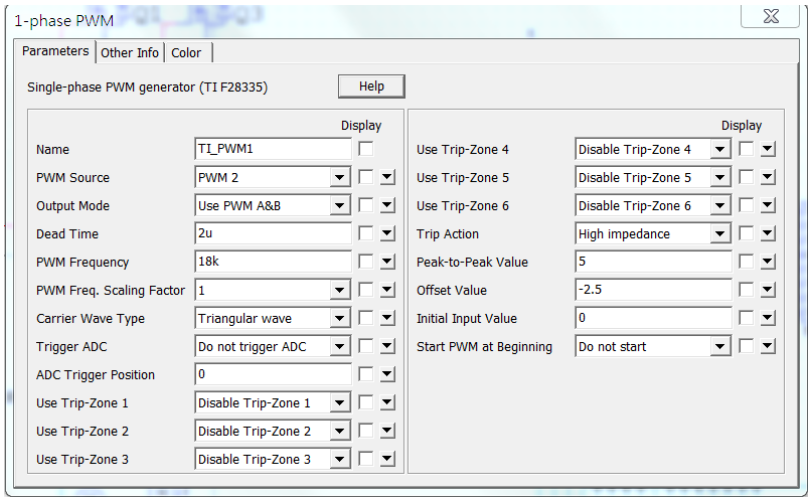
PWM Setting

The single-phase PWM, with A arm for PWM1 and B arm for PWM2, adopts 18kHz triangular wave with dead time 2μs and amplitude setting: Vp=10V, offset=-5V, i.e., the triangle wave between -5V~+5V. The initial status of PWM is not auto-activation; instead, it activates and stops via control of 2 modules: Start PWM and Stop PWM. Either PWM1 or PWM2 has its own Start PWM and Stop PWM modules.





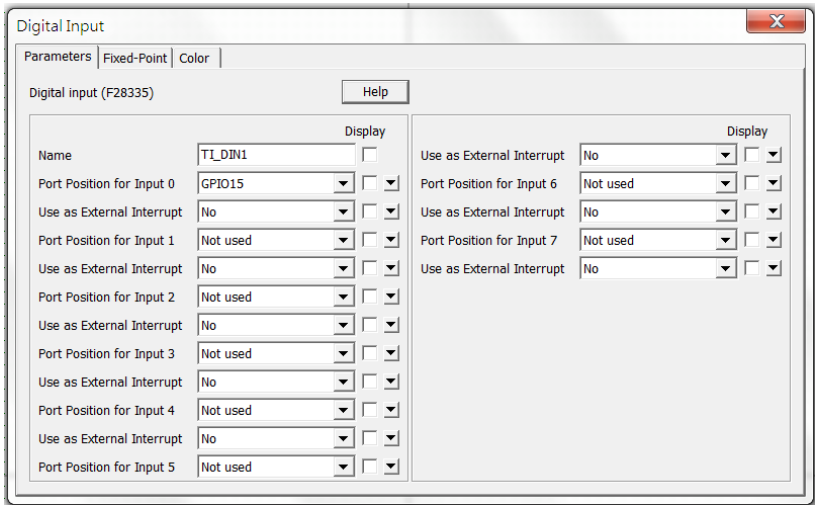
PWM 1



PWM 2

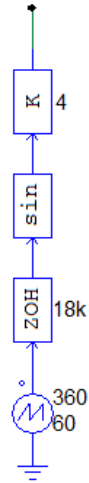
Digital Input (DI) Setting

The experiment enables or disables PWM1 and PWM2 via DI (by GPIO 15). DI input signal is generated from DSP external signal.



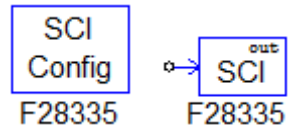
Sinusoidal Signal Generator

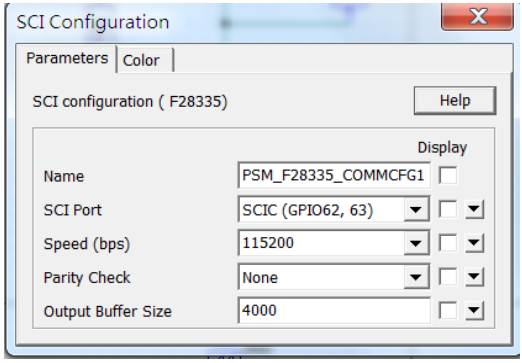
A signal of 60Hz amplitude representing angle with 360V is produced by the PSIM sawtooth generator. It passes through sampling process of 18kHz ZOH (zero-order-hold) and Sin function followed by multiplied by gain K to generate control voltage of PWM. It is available to make use of K value to define the amplitude modulation exponent of PWM.

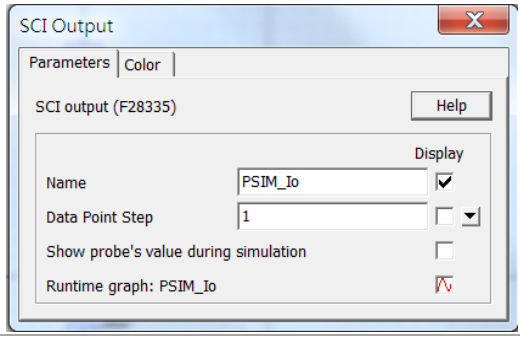


SCI Setting

The experiment send signal back to computer via SCI. The settings of 2 modules, SCI Config and SCI out, are as the following. The SCI communication speed is 115200(bps) without parity check and its buffer size is defined as 4000 points. SCI output, on the other hand, is set to send signal in every single point.

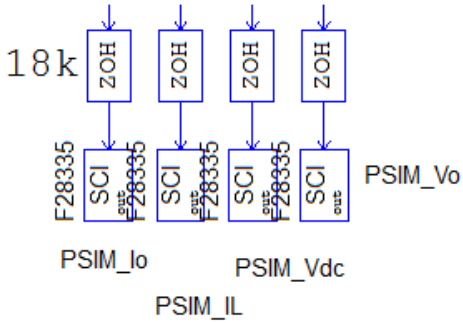






Note

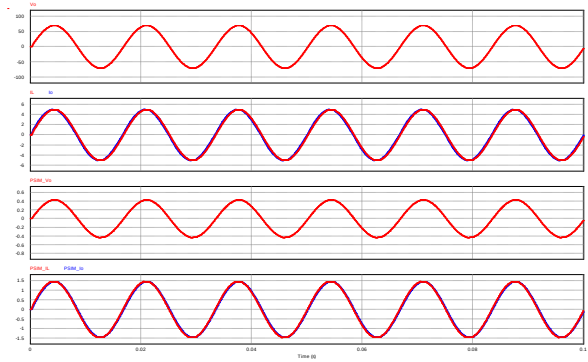
SCI out module must work with ZOH module, which is used to define breaking interval of SCI.



Simulating result of SimCoder circuit

Figure 4.10

The simulating result of SimCoder circuit



Code Autogeneration

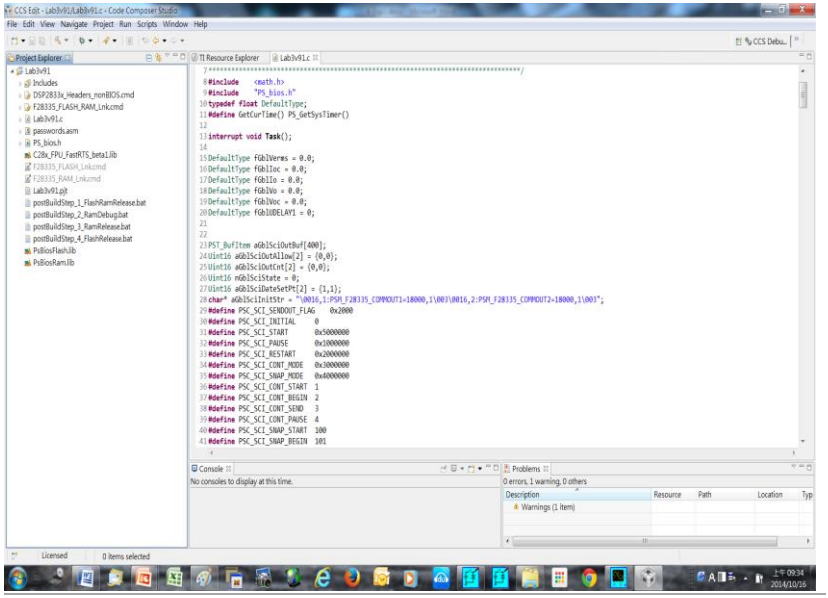
Convert the SimCoder control circuit of the above inverter circuit into the C Code via Simulate => Generate Code under PSIM. PSIM will generate a subdirectory named by the simulating file in the same directory with the simulating circuit. The auto-generated Code along with the related files for next project of TI Code Composer will be collectively saved into the subdirectory. For example, Lab1.psimsch generates a subdirectory named “Lab1”.

Compile and burn via TI Code Composer

Enter the TI Code Composer Studio

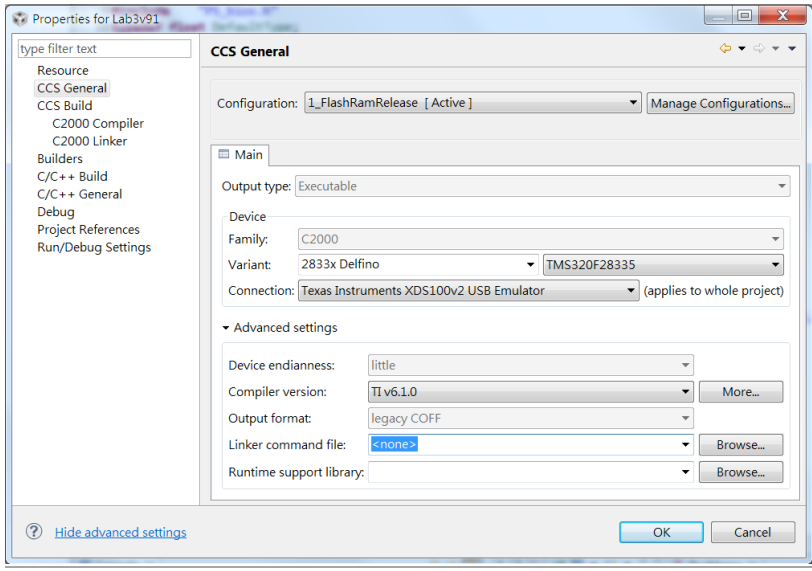
1. Bring up project: Lab1.pjt of the previous subdirectory (Lab1) by the following steps: Project => Import Legacy CCSv3.3 Project => Lab1.pjt under the subdirectory => Next => Finish.

   The following screen will therefore appear where clicking Lab1.c is able to check the C file generated from SimCoder.



2. Click Lab1[Active, FlashRamRelease] => Build all to check if any error occurred. Warnings can be simply omitted.

3. Click Lab1[Active, FlashRamRelease]=> Right click button => Set as follows



4. RUN => Debug => Burn program to DSPIC => Remove JTAG => Execute Experiment

Experiment Measurement

The experimental devices and teaching aid layout are illustrated as the figure 4.11. DC power supply, PSW 160-7.2, connects to the input terminal J1 of PEK-110. The output terminal J3 first passes through AC power meter GPM-8213 followed by connecting to passive load GPL-100. The switch trigger signal waveforms are indicated in the figure 4.12 and 4.13. The waveforms of output voltage/current and inductor current are indicated in the figure 4.14 and 4.15.

Figure 4.11

Experiment devices layout

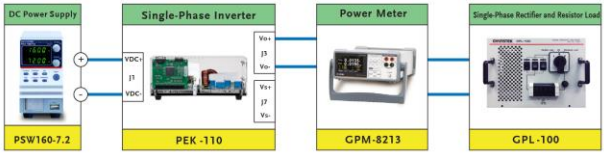


Figure 4.12

The waveforms (1/2) of unipolar voltage switching trigger signal

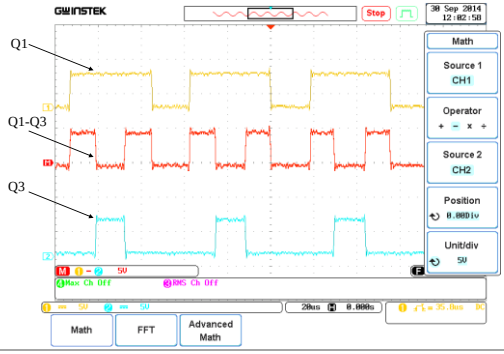


Figure 4.13

The measured waveforms (2/2) of unipolar voltage switching trigger signal

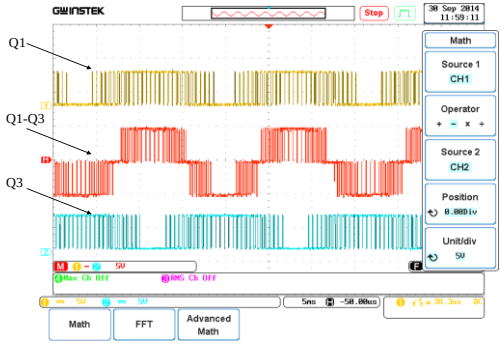


Figure 4.14

The measured waveforms of inverter output voltage and inductor current

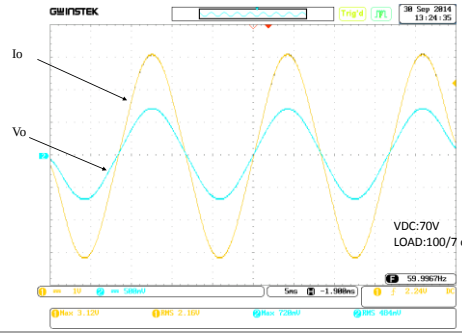
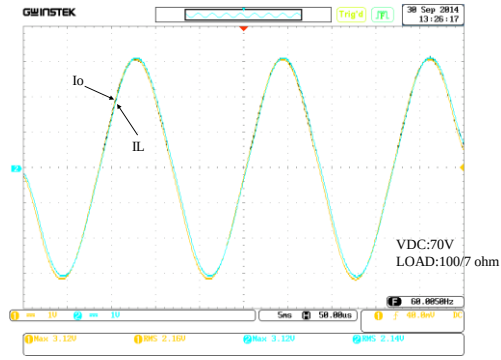


Figure 4.15

The measured waveforms of inverter inductor current and load current



It is allowed to turn on DSP Oscilloscope under PSIM when hardware circuit is active so that the signal feed backed from RS232-USB will be shown on computer.

Method to open DSP oscilloscope:

Utilities => DSP Oscilloscope => Refer to figure 4.16 for setting Serial port, which can be retrieved from the Device Manager under Control Panel, Baud rate, which requires to integrate with SCI Configuration, Parity check, which requires to integrate with SCI Configuration => Press Connect once completing setting. The screen shows as figure 4.17, 4.18 and 4.19 in which green light and signal feed backed screen show when connecting successfully. If it needs to access to DSP Oscilloscope result, refer to the instructions as figure 4.20 by clicking Save to select a location for file storage followed by observing and processing to these signals via SIMVIEW.

Figure 4.16

DSP Oscilloscope setting

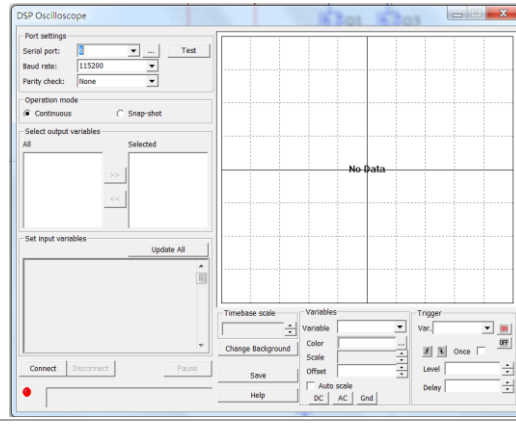


Figure 4.17

The inverter output voltage and inductive current waveforms from DSP Oscilloscope

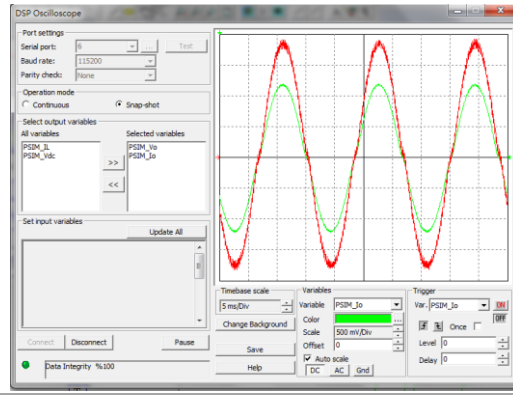


Figure 4.18

The inverter inductor current and load current waveforms from DSP Oscilloscope

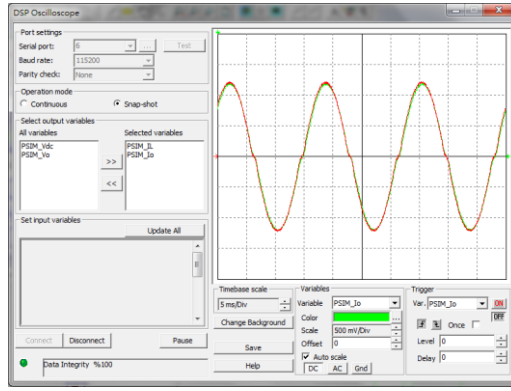


Figure 4.19

The input voltage waveforms from DSP Oscilloscope

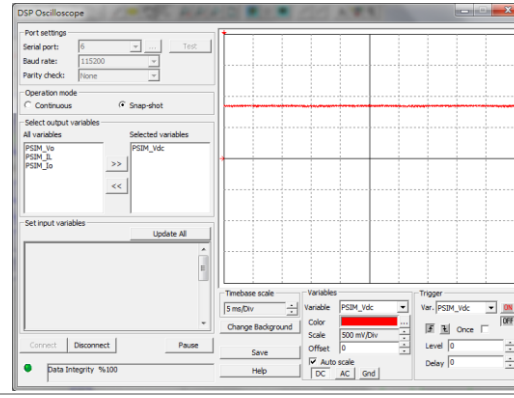
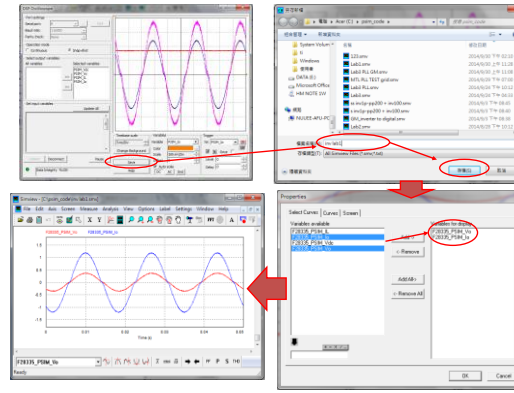


Figure 4.20

The method of converting DSP Oscilloscope waveforms to SIMVIEW



Experiment 2 – Individual Inverter of Dual-loop Inductor Current Control

The purpose of experiment

- Learn the way to modularization of single-phased full bridge inverter
- The control design of current loop and voltage loop
- RSM voltage loop design
- Hardware layout of inverter and programming of SimCoder

The principle of experiment

The working principle and model derivation of inverter circuit

As the figure 5.1 shown, the circuit architecture of full bridge converter utilizes dual-loop design in which outer loop is voltage loop whose deviation used to generate inductive current command for inner loop, and inner loop is inductor current loop whose deviation used to generate control voltage for PWM.

PWM adopts the sinusoidal PWM switch to generate trigger signal of switch, whilst L-C forms a 2-level low pass filter, which is used to attenuate high-frequency switch item from inverter output, to turn the output voltage into low-frequency sine wave.

From the figure 5.1, we may infer as follows:

$$C\frac{dV_c}{dt} = I_{cap} = I_o - I_L \tag{5.1}$$

$$L\frac{dI_o}{dt} = V_{AN} - V_{BN} - V_c = S_A V_d - S_B V_d - V_c \tag{5.2}$$

S_A and S_B are switch functions for A arm and B arm switch individually:

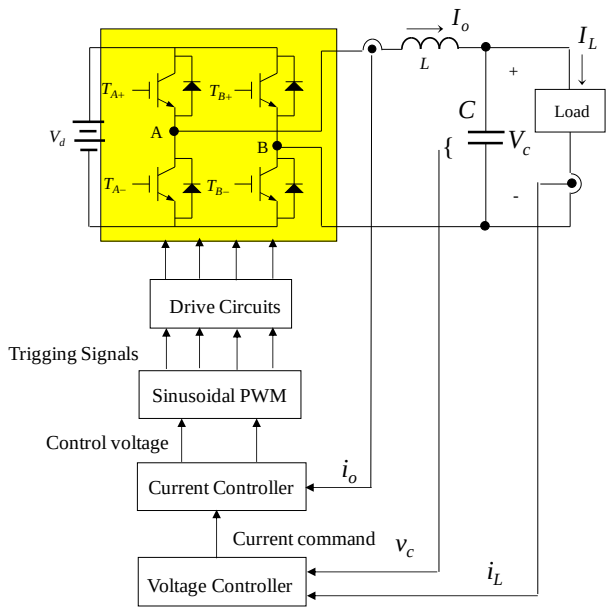
$$S_i = \frac{1}{2} + \frac{v_{coni}}{2v_{tm}} \quad (i = A, B) \tag{5.3}$$

v_{conA} and v_{conB} are PWM control voltage for A arm and B arm individually. If switch utilizes unipolar voltage switching, it becomes as follows:

$$v_{conB} = -v_{conA} \tag{5.4}$$

Figure 5.1

The circuit architecture of single-phased full bridge inverter



We may infer as follows from the (5.3):

$$S_A = \frac{1}{2} + \frac{v_{coni}}{2v_{tm}} \quad S_B = \frac{1}{2} + \frac{-v_{coni}}{2v_{tm}} \tag{5.5}$$

Where v_{tm} is the amplitude of PWM triangle wave. We get as follows by substituting (5.5) into (5.2):

$$L\frac{dI_o}{dt} = \frac{v_{con}}{v_{tm}}V_d - V_c \tag{5.6}$$

To make

$$k_{pwm} = \frac{V_d}{v_{tm}} \tag{5.7}$$

We get as follows:

$$L\frac{dI_o}{dt} = k_{pwm}v_{con} - V_c \tag{5.8}$$

The aforementioned (5.6) and (5.8) can be applied to voltage loop and current loop respectively as the figure 5.1 shown.

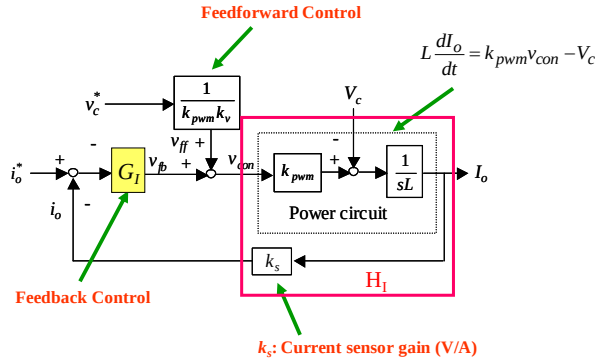
Controller Design

A. The Design of Current Loop Controller

As the figure 5.2 shown, the current loop design where power circuit block is illustrated in accord with (5.8) and k_v and k_s are voltage sense gain and current sense gain, respectively. The adopted feedforward control makes voltage command v_c^* be multiplied by gain $1/k_{pwm}k_v$ to directly offset the disturbance in current loop from output voltage V_c.

Figure 5.2

Current control loop design



Current control G_I can be designed by the controllers including P, PI and Type 2. When P controller is under operation, $G_I = k_1$ and we can infer as follows from the figure 5.2:

$$\frac{i_o}{i_o^*} = \frac{\frac{k_1 k_s k_{pwm}}{L}}{s + \frac{k_1 k_s k_{pwm}}{L}} = \frac{u_i}{s + u_i} \tag{5.9}$$

The pinnacle u_I here is equal to bandwidth of current loop, from which we can infer as follows:

$$k_1 = \frac{u_i L}{k_s k_{pwm}} \tag{5.10}$$

When Type2 is being utilized, it becomes as follows:

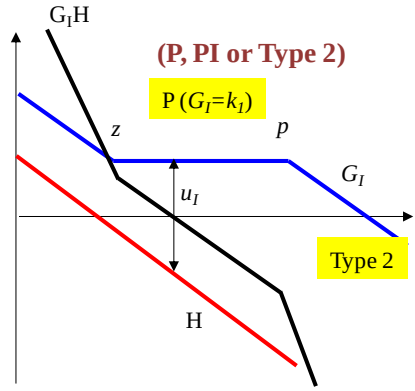
$$G_I(s) = \frac{K_1(s+z)}{s(s+p)} \quad (5.11)$$

The design of current loop bode plot is illustrated as figure 5.3 with the following details:

1. Set u_I 1/10~1/8 of the switch frequency. k_1 can be directly retrieved when adopting P controller. If Type2 is adopted, jump to the step 2 instantly.
2. Set $z = \frac{u_I}{3}$
3. Set $p = 3u_I$
4. Get k_1 by utilizing $G_I(u_I)H_I(u_I)$=1.

Figure 5.3

The bode plot of current control loop response



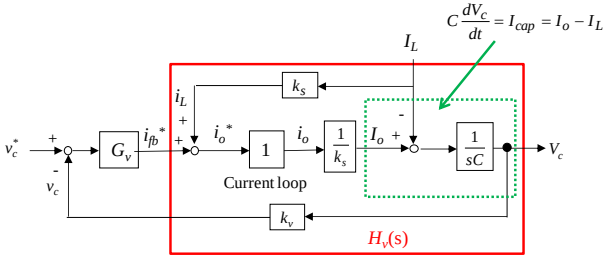
B. The design of voltage loop control

As the figure 5.4 shown, the block diagram of voltage loop control where power circuit is illustrated based on (5.1).

If the bandwidth (u_I) corresponding to current loop is higher than the bandwidth of voltage loop by 4 times above, analysis of the corresponding current loop to the corresponding voltage loop is regarded as 1. Voltage loop controller adopts both feedforward control and feedback control. Due to the sense load current, voltage controller adds the sense load current (i_L) into current command as feedforward control to directly offset the disturbance in voltage loop from load current.

Figure 5.4

The block diagram of voltage control loop



Voltage controller (G_v) can design via Proportional (P) or Proportional integral (PI) controller; when P controller is under operation, $G_v = k_2$ and we may get as follows from the figure 5.4.

$$\frac{v_o}{v_o^*} = \frac{\frac{k_2 k_v}{C}}{s + \frac{k_2 k_v}{k_s C}} = \frac{u_v}{s + u_v} \tag{5.12}$$

When PI controller is under operation, it becomes as follows:

$$G_v = \frac{K_2(s+z)}{s} \tag{5.13}$$

The design of voltage loop bode plot is illustrated as figure 5.5. The voltage loop bandwidth uv designed by P or PI controller can be defined 1/4, i.e., $u_v = u_I / 4$, of current loop bandwidth (u_I). When P controller is under operation, it becomes as follows:

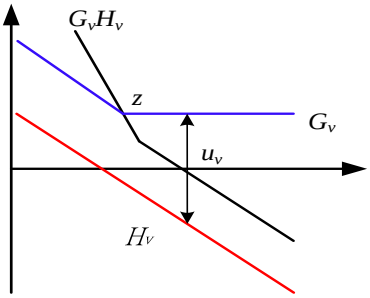
$$k_2 = \frac{u_v C}{k_v} \tag{5.14}$$

When P controller is in operation, the way to design is as follows:

1. Set u_v is $\frac{u_I}{4}$
2. Set $z = \frac{u_v}{3}$
3. $Get\, k_2\, via\, G_v(u_v)H_v(u_v)$=1

Figure 5.5

The bode plot of voltage control loop response



C. To enhance voltage adjustment rate by adding voltage RMS value loop

To make inverter output be equipped with better voltage adjustment rate, it is recommended to add a RMS (Root Mean Square) value loop outside of voltage loop (figure 5.6(a)), which compares output voltage RMS value v_{cm} calculated from H_{rms} with the command of RMS value v_{cm}^* followed by G_m adjustment to generate an amplitude corrected signal A_{mr} that is used to correct the original amplitude command A_{m0}. The ultimate amplitude command A_m is acquired, which will be further multiplied by unit sinusoidal wave sinωt to obtain the transient voltage command v_c^*. In order to acquire precise RMS value, it is required to utilize H_{rms} to calculate RMS value with the necessary definition of RMS value as the following equation.

$$v_{cm} = \sqrt{\int v_c^2 d\omega t / 2\pi} \qquad (5.11)$$

The calculation result from (5.11) is generally processed by a low-pass filter, which can be represented as follows:

$$H_{LPF} = \frac{a}{(s+a)} \tag{5.12}$$

The cutoff frequency a, in general, is set below 20Hz, and G_m generally adopts the proportional integral control to obtain the accurate voltage adjustment rate.

The calculation of RMS value, however, is energy-consuming in memory, the generic calculation utilizes the simpler block diagram (figure 5.6(b)) for design, which makes use of rectification (ABS block) and low-pass filter (H_{LPF}) to calculate the average of sinusoidal wave followed by multiplied by $\frac{\pi}{2\sqrt{2}}$ (=1.11) to acquire RMS value. Considering the filter signal in connection with the 2nd ripple, it is suggested to add a band-pass filter (H_{BPF}) to calculate the 2nd ripple, which will be subtracted from the original signal to obtain a mild-prone RMS value.

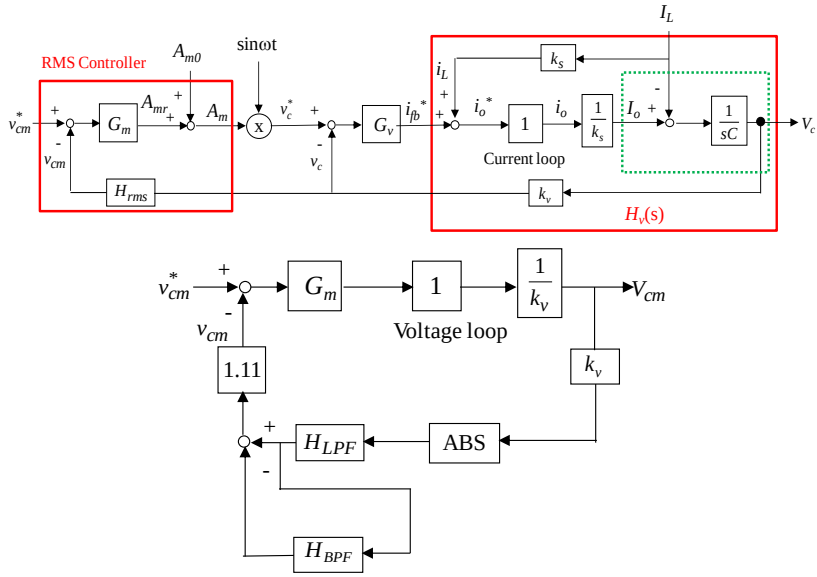


Figure 5.6 (a) Voltage RMS value control loop block diagram; (b) Simpler block diagram

Circuit Simulation

Inverter Specification

- P_o=115W, V_o=40Vac/60Hz,
- V_d = 70V, v_{tri}=18kHz/5Vpp, k_s = 1/3.472V/A, k_v = 1/162.2,
- Utilize unipolar voltage switching with blank time 2μs
- L = 1.323mH, C= 10μF

Controller Design

- u_1 = 18kHz/10=1.8kHz = 11310 rad/s => k_1 = 1.68
- u_v = 1.8kHz/4=450Hz = 2827 rad/s => k_2 = 4.6

Based on the simulating circuit constructed by the above parameters (figure 5.7), the simulating result under linear load is illustrated as the figure 5.8. Change the calculation of RMS value of the above control circuit to the method described as the figure 5.6(b), and the simulating circuit is illustrated as the figure 5.9.

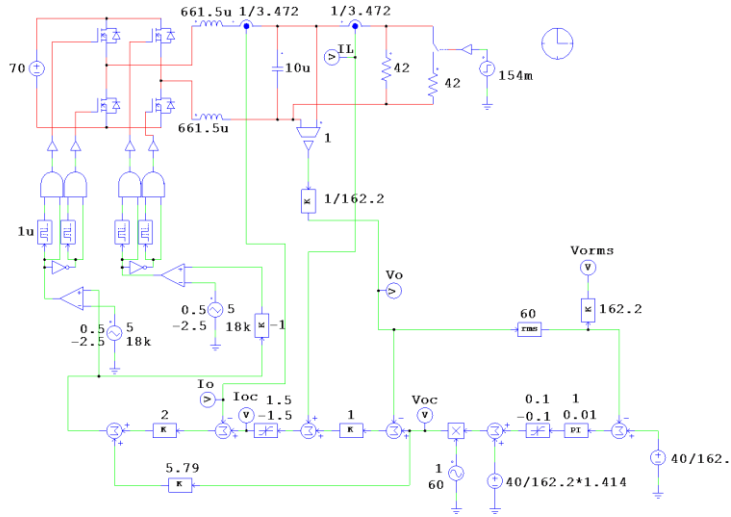


Figure 5.7 The simulating circuit of dual-loop control inverter

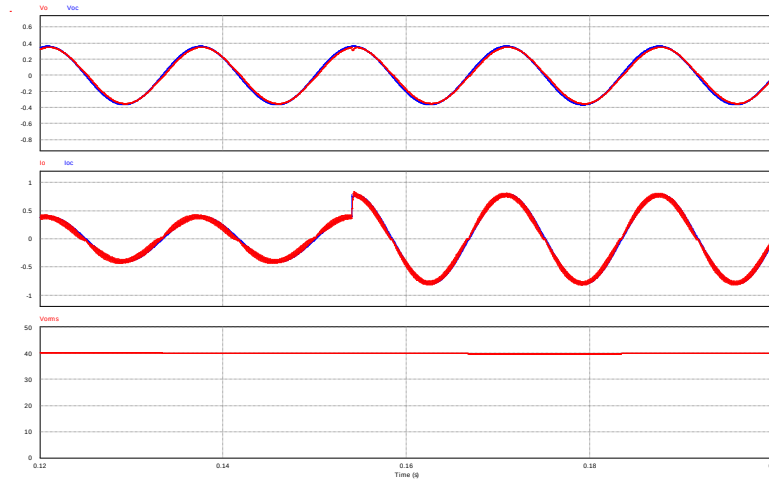


Figure 5.8 The simulating result of dual-loop control inverter

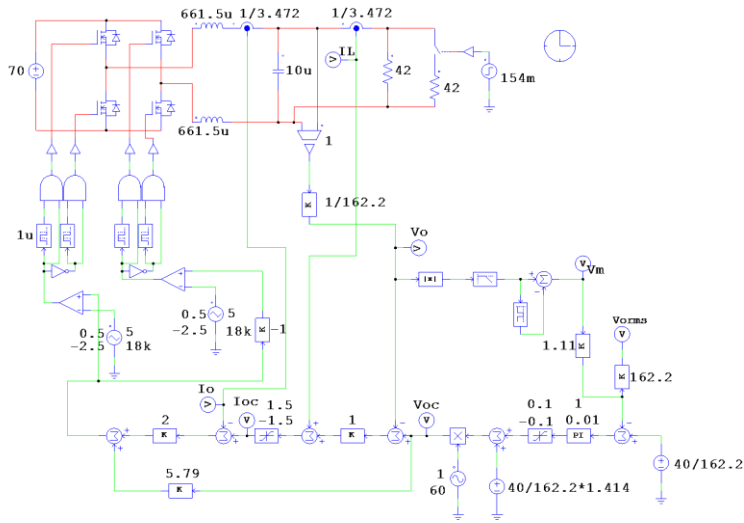


Figure 5.9 The simulating circuit of linear load from the RMS calculation of figure 5.6 (b)

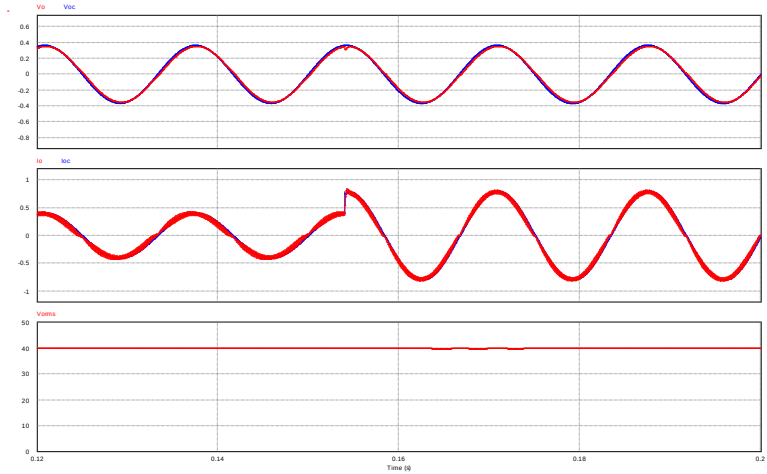


Figure 5.10 The simulating result of linear load from the RMS calculation of figure 5.6 (b)

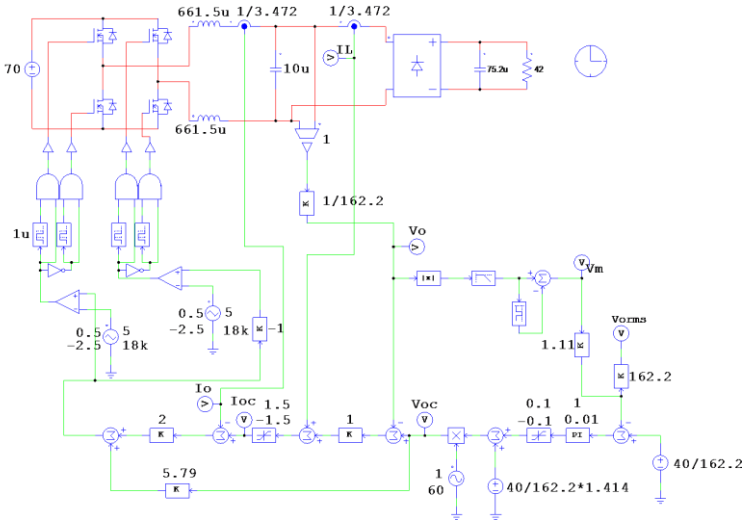


Figure 5.11 The simulating circuit of non-linear load from the RMS calculation of figure 5.6 (b)

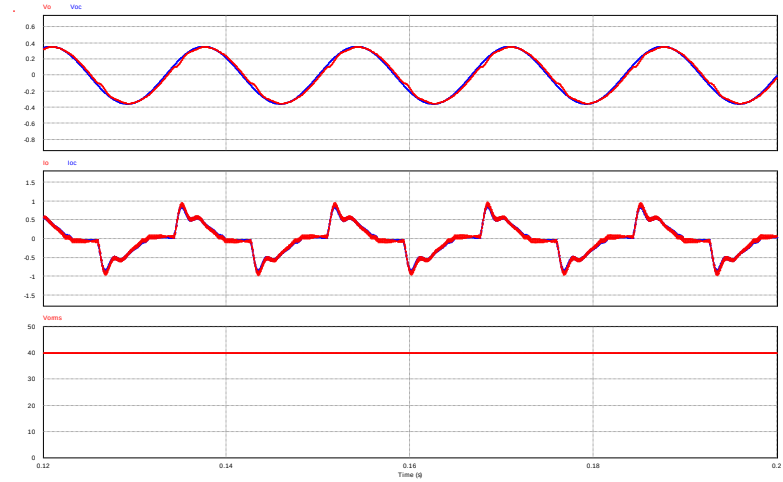


Figure 5.12 The simulating result of non-linear load from the RMS calculation of figure 5.6 (b)

SimCoder Program Layout and Circuit Simulation

Based on the inverter simulating circuit of figure 5.9, change to the SimCoder circuit layout of control circuit (figure 5.13) realized by TI F28335 in which AD sampling is continuous, while each sense signal has to pass through a 18kHz ZOH. To calculate low-pass and high-pass digital filters of RMS, utilize the s2z Converter under PSIM Utilities to digitize the analog filter (figure 5.9) to obtain. The sample frequency is 18kHz, and the way to digitization is Back Euler. The simulating results of linear R load (0.95A=>1.9A) and non-linear (RCD, C=75.2μF, R=42Ω) are illustrated as the figure 5.14 and 5.15, respectively, both of which are almost identical with the analog simulating result.

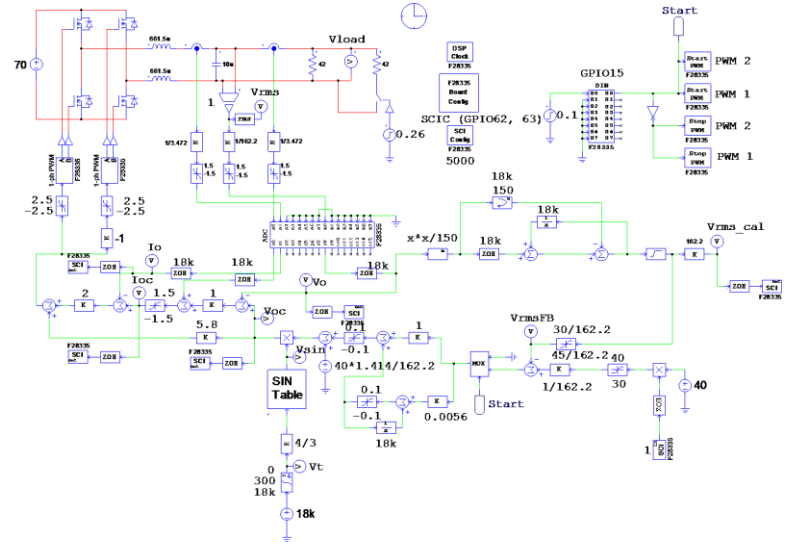


Figure 5.13 The inverter simulating circuit constructed by the method of SimCoder

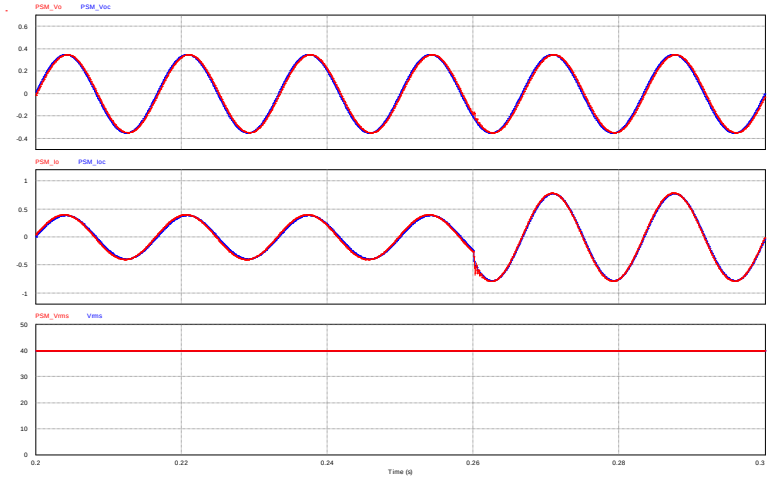


Figure 5.14 The simulating result of linear load

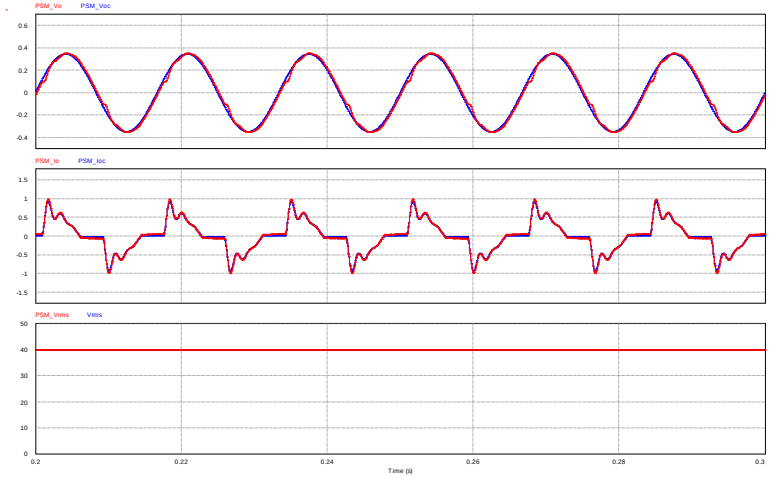


Figure 5.15 The simulating result of non-linear load

Experiment Measurement

Refer to the figure 5.16 for the layout of experimental devices and teaching aid. DC power supply, PSW 160-7.2, connects to the input terminal J1 of PEK-110. The output terminal J3 first passes through AC power meter GPM-8213 followed by connecting to passive load GPL-100. The figure 5.17 indicates measured waveforms of linear load. The figure 5.18 indicates measured result sent from RS232. The figure 5.19 indicates measured waveforms of non-linear load. The figure 5.20 indicates measured result sent from RS232.

Figure 5.16

Experiment device layout

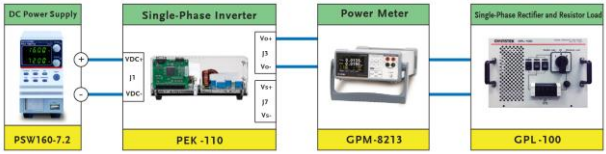


Figure 5.17

The measuring result of linear load

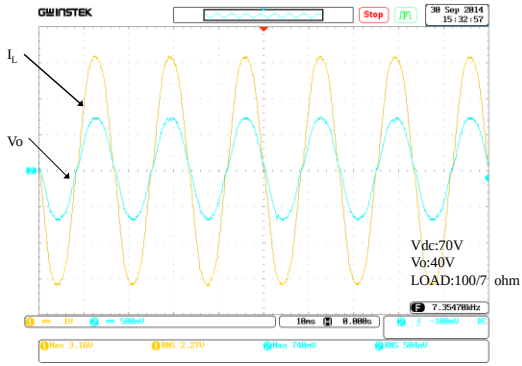


Figure 5.18

The measuring result (a) sent from RS232 under linear load

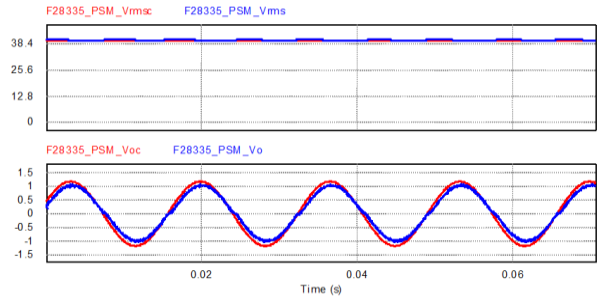


Figure 5.18

The measuring result (b) sent from RS232 under linear load

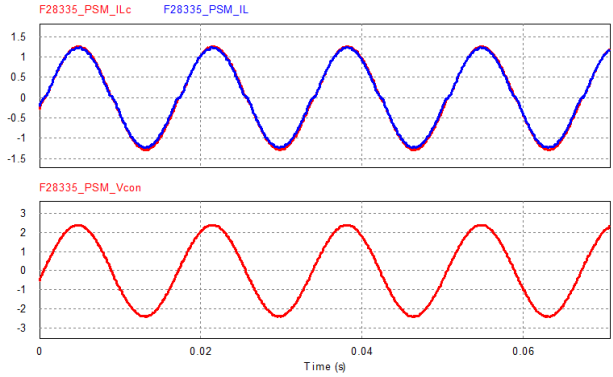


Figure 5.19

The measuring result under non-linear load

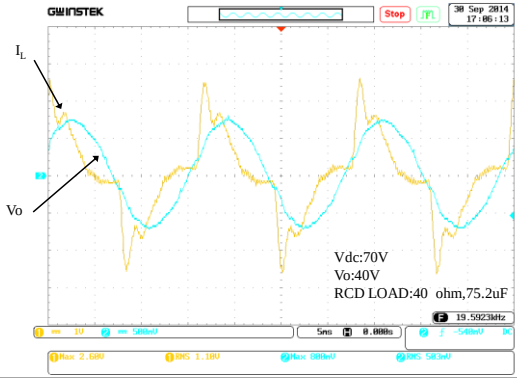


Figure 5.20

The measuring result (a) sent from RS232 under non-linear load

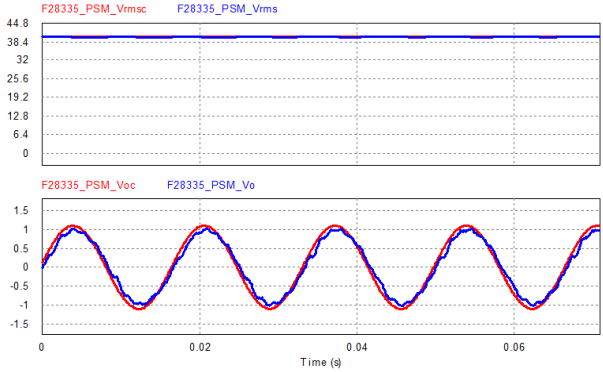
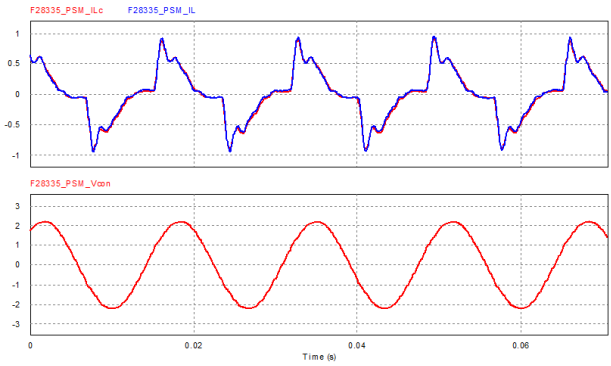


Figure 5.20

The measuring result (b) sent from RS232 under non-linear load



Experiment 3 – Single-phased Grid-connected Electricity Parallel Inverter

The purpose of experiment

To learn the phase-locked loop, current/voltage loop control design and hardware layout of grid-connected electricity parallel inverter. Also, it is to learn the SimCoder program composing of grid-connected electricity.

The principle of experiment

The working principle and control design of grid-connected parallel inverter circuit.

As the figure 6.1 shown, the control architecture of single-phased parallel inverter adopts dual-loop design in which outer loop is DC voltage control used to maintain DC-link voltage (V_d), and inner loop is inductor current control used to regulate grid-connected input current, turning input power factor into 1. Refer to the figure 6.2 for current loop control block diagram design. Similar to the inverter of the experiment 2, by utilizing both feedback and feedforward controls, if input current meets the identical unit power factor with input voltage, feedforward control signal vo* will be used to erase disturbance in current loop from Vs. Therefore, current loop can be feedback loop to acquire as follows:

$$\frac{i_o}{i_o^*} = \frac{\frac{k_s k_1 k_{pwm}}{L}}{s + \frac{k_s k_1 k_{pwm}}{L}} = \frac{u_R}{s + u_R} \quad , u_R = \frac{k_s k_1 k_{pwm}}{L} \tag{6.1}$$

u_R is equivalent to bandwidth of input current loop, which can be set by gain k_1. As the figure 6.3 shown, the inverter current command (i_o^*) is generated by DC voltage control G_v of outer loop, which results from deviation of voltage adjustment multiplied by an unit sinusoidal wave (sinwt) that syncs with input voltage.

G_v design must be derived from the module of DC voltage loop. Refer to the figure 6.4(a) for the circuit under equivalent unit power factor to infer design. The module of DC side can be only DC capacitor in that DC-link connects to other converter which receives/supplies electricity provided/absorbed by grid-connected electricity. The input power of AC side is as follows.

$$\begin{aligned} P_{ac} &= V_{s(p)} \sin \omega t \cdot I_m \sin \omega t = \frac{V_{s(p)} I_m}{2} - \frac{V_{s(p)} I_m}{2} \cos 2\omega t \\ &= \overline{P}_{ac} + \tilde{P}_{ac2} \end{aligned} \tag{6.2}$$

In addition to a DC item, a twice harmonic wave item is also included, which will cause twice ripples in DC voltage. The average power of DC side is equal to DC item of AC side power

$$\overline{P}_{ac} = P_{dc} \tag{6.3}$$

The equivalent circuit as the figure 6.4 (b) shown is acquired by AC current source responding to DC side. We further obtain the following based on the (6.3).

$$\frac{V_{s(p)} I_m}{2} = V_d I_d \tag{6.4}$$

$$I_d = \frac{V_{s(p)} I_m}{2V_d} = k_{dc} I_m \tag{6.5}$$

Cd capacitor charged by DC current source Id leads to the module of voltage loop as follows:

$$\frac{V_d}{I_m} = \frac{k_{dc}}{sC_d} \text{ , } k_{dc} = \frac{V_{s(p)}}{2V_d} \tag{6.6}$$

Voltage control G_v can be designed in accordance with the figure 6.5 where the current loop response (6.1) is simplified to be equal to 1 due to the fact that current loop bandwidth is much wider than voltage loop bandwidth. Therefore, the gain of current amplitude I_m from I_m^* to actual I_o is the reciprocal of current sense ratio k_s. With bode plot of voltage loop H_{dc}, it is able to draw the contents shown in the figure 6.6.

Considering the DC voltage in connection with the 2-times ripple, it is suggested to lower down the bandwidth of voltage loop by large scale below 120Hz in order to attenuate the 2-times ripple of voltage in that it needs to make grid-connected electricity current command to low distortion. Therefore, G_v adopts the design method of type II compensator, that is, PI + Low-Pass). The bode plot is illustrated as the figure 6.6. The closed-loop gain and the response utilizing only PI controller are supposed to being drawn collectively within the figure 6.6 for further comparison.

Figure 6.1

Control architecture of single-phased grid-connected parallel inverter

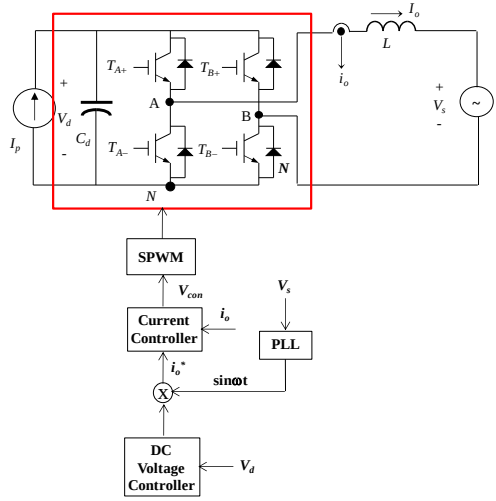


Figure 6.2

Current control loop

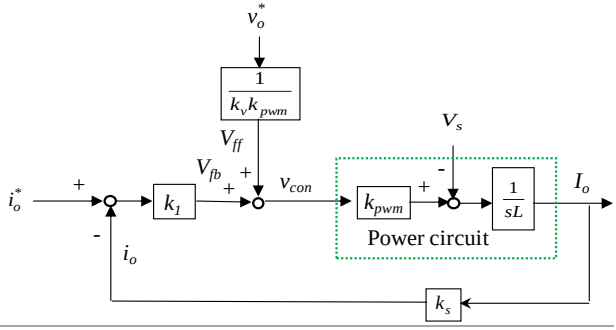


Figure 6.3

Voltage control loop

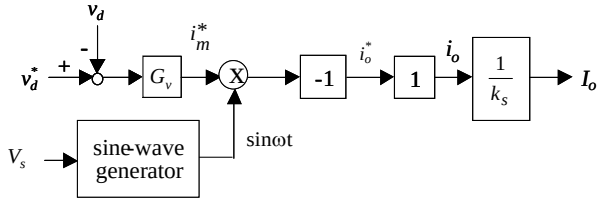


Figure 6.4

Equivalent circuit under unit power factor of inverter

(a) Equivalent circuit

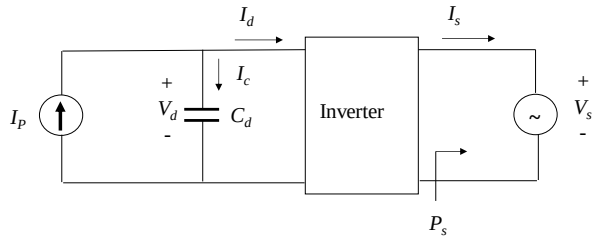


Figure 6.4

Equivalent circuit under unit power factor of inverter

(b) Equivalent circuit of small signal in DC side

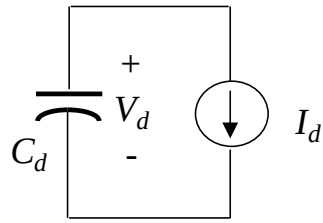


Figure 6.5

Voltage loop control design

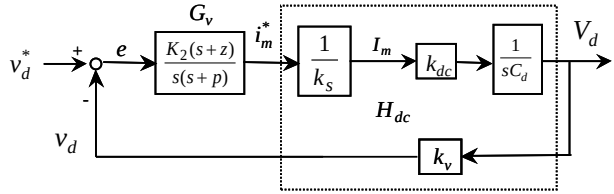
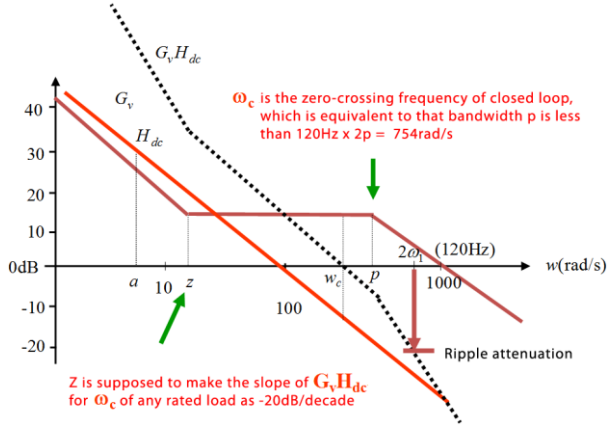


Figure 6.6

Bode plot of voltage loop control



Phase-locked Loop Design

As the figure 6.7 shown, phase-locked loop utilizes grid-connected electricity voltage (V_s) sampling (S/H) and obtains a signal $V_m sin(wt)$ followed by a delay of ¼ cycle grid-connected electricity to acquire the other signal $V_m cos(wt)$. The above 2 signals will be individually multiplied by the synchronizing signals $cos(\omega_1 t)$and $sin(\omega_1 t)$ to result in as follows:

$$e = V_m\{\sin(\omega t)\cos(\omega_1 t) - \cos(\omega t)\sin(\omega_1 t)\} \quad (6.7)$$

The signal e passes through a proportional integrator (PI) to obtain a frequency corrected signal $\Delta\omega$ which plus the original set frequency ω_0(=377) is equal to frequencyω_1. $\omega_1$further experiences integral to acquire an angle signal θ, which again passes through a limiter between 0~2π followed by referring to both Sine table and Cosine table to finally obtain $cos(\omega_1 t)$ and $sin(\omega_1 t)$ signals. Through proportional integral adjustment to decrease deviation e down to zero so that the phase-locked, also known as $\omega = \omega_1$, is properly achieved.

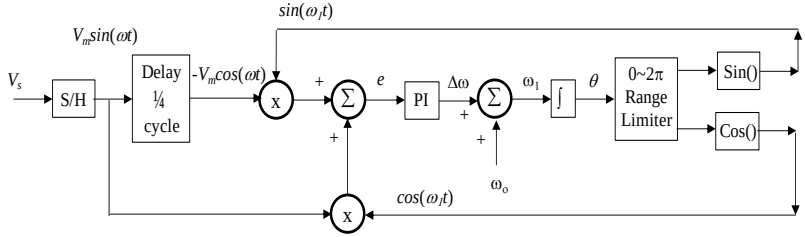


Figure 6.7 Phase-locked Loop

Circuit Simulation

Rectifier specification

- P_o=115W, V_o=40Vac/60Hz,
- V_d = 70V, v_{tri}=18kHz/5V_{pp}, k_s = 1/3.472V/A, k_v = 1/162.2,
- Adopts unipolar voltage switching with blank time 2μs
- L = 1.323mH, C_d= 330μF, Co=10μF

Current loop design

$$k_{pwm} = 70/2.5 = 28$$
$$f_{ci} = 18k/10 = 1.8kHz$$
$$u_R = 1.8k \times 2\pi = 11310rad/s$$

- $k_1 = 1.68$

Voltage loop design

- $H_{dc}(s) = \frac{26.21}{s}$
- Sets $f_c = 20Hz, \omega_c = 125rad/s$
- When G_v of p=180rad/s, z=30rad/s is selected, it turns out $G_v(s) = \frac{1024(s+30)}{s(s+180)}$

PSIM Simulation

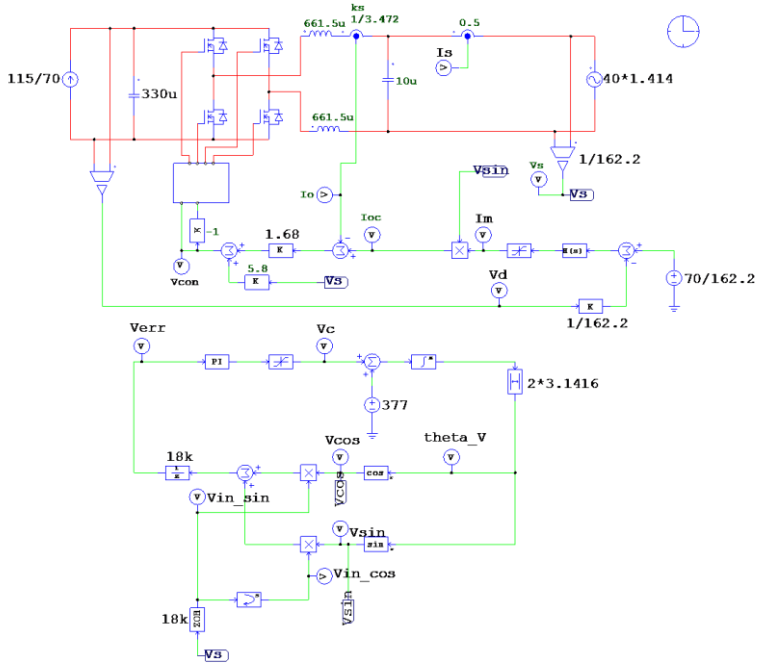


Figure 6.8 Grid-connected electricity parallel inverter PSIM simulating circuit

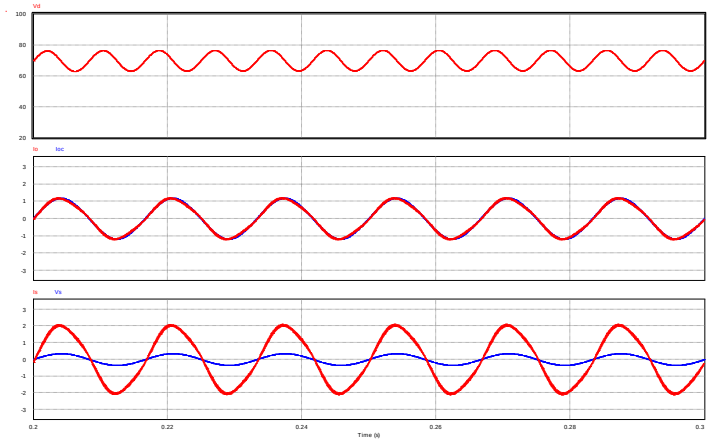


Figure 6.9 Grid-connected electricity parallel inverter PSIM simulating result

SimCoder Program Layout and Circuit Simulation

Refer to the figure 6.10 for the grid-connected electricity parallel inverter circuit. In addition to the aforementioned voltage and current controls, phase-locked circuit, it also covers the following items: 1. A relay control which detects if input voltage (V_d) and grid-connected electricity voltage are normal to activate relay with turning on grid-connected electricity. 2. A PWM startup circuit, which not only detects grid-connected electricity voltage apart from relay, but also inspects inverter voltage following relay in parallel; when both voltages are normal, PWM is allowed to start triggering and voltage integral is permitted to operate. Refer to the figure 6.11 for the simulating result.

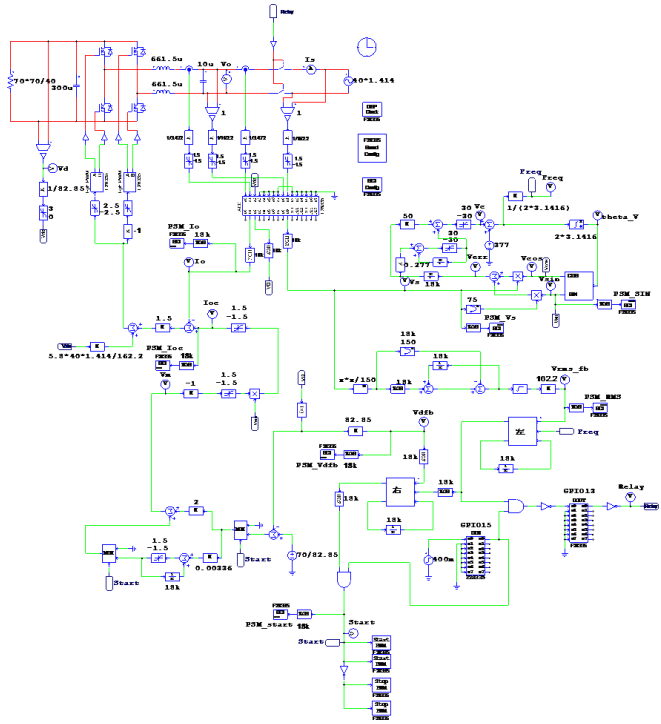


Figure 6.10 Grid-connected parallel inverter circuit built by SimCoder

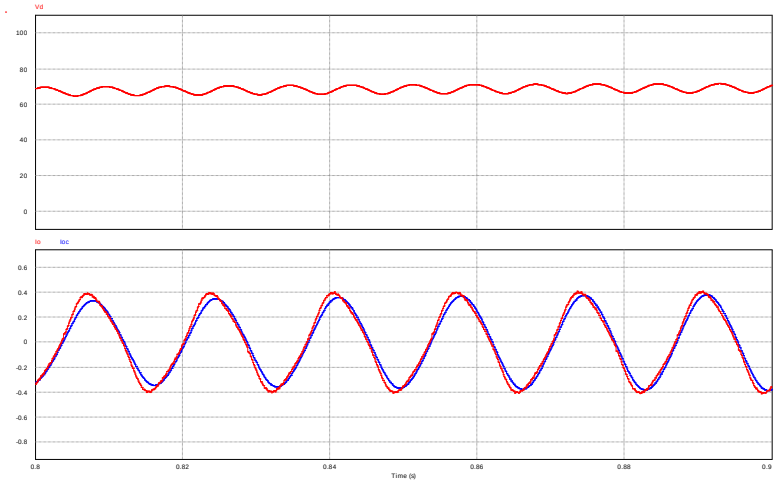


Figure 6.11 Grid-connected parallel inverter circuit simulating result built by SimCoder

Experiment Measurement

Refer to the figure 6.12 for the layout of experimental devices and teaching aid. DC power supply, PSW 160-7.2 (75V with CC level in 1A), connects to the terminal J1. The terminal J3 first passes through AC power meter GPM-8213 followed by connecting to passive AC load GPL-100. The terminal J7 connects with AC power supply, APS-7050 (40Vac with CC in limited setting 4A) to simulate grid-connected electricity. The passive AC load GPL-100 connects to the AC side in order to make the power by inverter consumed properly in AC load, of which set the 3-level resistor ON (below 40Vac, 150W above).

Make sure the power button of inverter is OFF before startup followed by opening the DC and AC power and then turn on the inverter.

The power diagram of AC and DC (figure 6.13) shows waveforms of output voltage and grid-connected electricity voltage measured by DSP oscilloscope in phase-locked loop. Refer to the figure 6.14 for actual waveforms of grid-connected electricity voltage and inductor current. Refer to the 6.15 for the waveforms shown on the DSP oscilloscope.

The current feeding into grid-connected electricity can be adjusted through CC level of DC power.

Figure 6.12

Experiment devices layout

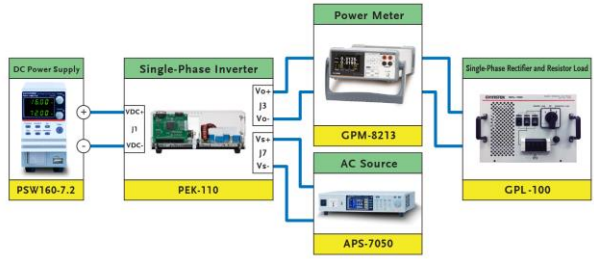


Figure 6.13

Measured waveforms by phase-locked loop DSP oscilloscope

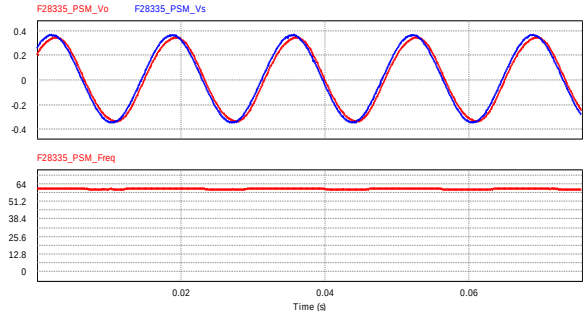


Figure 6.14

Grid-connected electricity voltage and inductor current measured waveforms

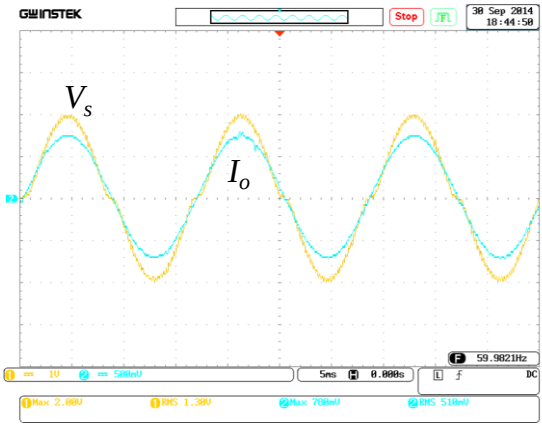
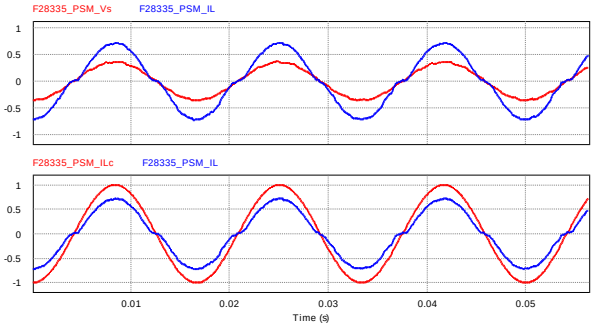


Figure 6.15

Measured voltage and current waveforms by DSP oscilloscope



Experiment 4 – Bridgeless PFC AC-DC Converter

The purpose of experiment

To realize the principle of CCM PFC, the control design of current and voltage loop, the design of Totem pole bridgeless PFC converter, hardware layout and PDC SimCoder programming.

The principle of experiment

The control method of single-phased CCM step-up PFC converter

CCM step-up PFC converter mostly adopts the dual-loop average current control architecture (figure 7.1), in which K_v and K_s represent voltage sense ratio and current sense ratio, respectively. The comparison result between feedback output voltage (V_{df}) and reference voltage (V_d^*) passes through voltage deviation amplifier (G_v) to acquire signal V_{ea}, which will be further multiplied by sensed input voltage signal $K_v V_{in}$ to obtain inductor current command I_s^*. The I_s^* will be compared with feed backed inductive current signal Is followed by experiencing the adjustment of current deviation amplifier (G_{CA}) to further acquire PWM control voltage V_{con}, which will be then compared with sawtooth wave (V_t) to forwardly obtain the duty cycle of switch. The input voltage is illustrated as follows:

$$V_{in}=V_m sin\omega t \tag{7.1}$$

From the figure 7.1, we may acquire as follows

$$I_s^* = K_v V_{in} V_{ea} \tag{7.2}$$

If current loop can force current to follow the command, $I_s=I_s^*$ and input inductor current can be illustrated as follows:

$$I_{in} = I_s / K_s = I_s^* / K_s = K_v V_{in} V_{ea} / K_s \tag{7.3}$$

We may obtain as follows from power balance:

$$\begin{aligned} P_{chg} &= V_d I_o = P_{in} = I_{in} V_{in} = K_v V_{in}^2 V_{ea} / K_s \\ &= K_v \frac{V_m^2}{2}(1-\cos 2\omega t) V_{ea} / K_s \\ &= P_o + P_{o2} \end{aligned} \tag{7.4}$$

From the (7.4), omit two-times reactive power to obtain as follows:

$$I_o = \frac{K_v V_m^2}{2 K_s V_d} V_{ea} \tag{7.5}$$

Based on (7.5), the gain of (I_o/V_{ea}) is directly proportional to the square of input voltage. Due to the fluctuation of grid-connected electricity is up to 3 times (90~264V_{ac}) under universal electric voltage, the gain variation reaches the maximum 9 times, which causes adverse effect in design of voltage loop deviation amplifier.

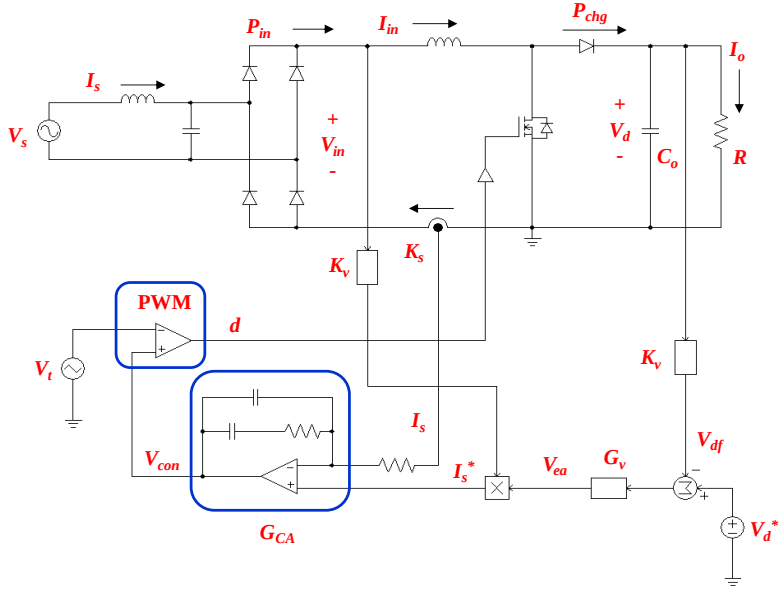


Figure 7.1 CCM step-up PFC converter adopting dual-loop average current control architecture

To improve the abovementioned influence to voltage loop gain from input voltage fluctuation, the voltage feedforward control is added as the figure 7.2 where V_{ea} signal is multiplied by $K_v V_{in}$ and then divided by the square of input voltage to obtain the inductor current command Is as the following:

$$I_s^* = \frac{K_v V_{in} V_{ea}}{K(K_v V_{in})^2} \tag{7.6}$$

We may acquire as follows via the deployment:

$$\begin{aligned} P_{chg} &= P_{in} = I_{in}V_{in} = V_d I_o \\ &= V_{in} I_s^* / K_s \\ &= K_v V_{in}^2 V_{ea} / (K_s K (K_v V_{in})^2) \\ &= V_{ea} / (K_s K_v K) \end{aligned} \tag{7.7}$$

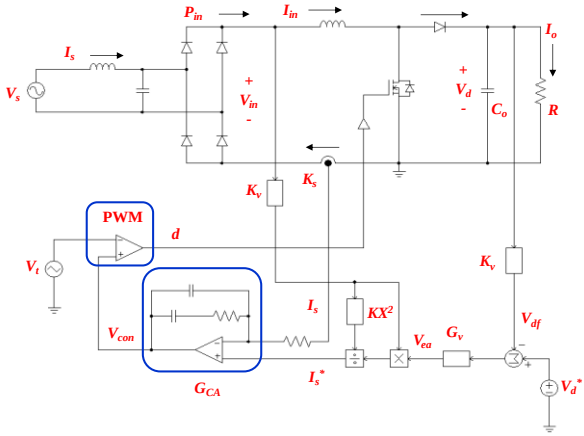
Therefore, it turns out as follows:

$$I_o = \frac{1}{K_s K_v K} V_{ea} \tag{7.8}$$

In the (7.8), it indicates the gain of (I_o / V_{ea}) is no longer directly proportional to the input voltage. Instead, though the fluctuation of grid-connected electricity is up to 3 times, for maintaining the certain value, voltage loop gain remains unchanged, which is efficient for designing deviation amplifier of voltage loop.

Figure 7.2

The CCM step-up PFC converter with feedforward control dual-loop average current control



The control design of single-phased CCM step-up PFC converter

A. Current loop design

For the dual-loop control architecture where outer loop control generates command of inner loop control, the bandwidth of general inner loop is wider than that of outer loop (4 times generally). Therefore, it is supposed to designing inner loop firstly, and regarding the response of inner loop control as ideal when

designing outer loop control. We start from the design of current inner loop; prior to design of current deviation amplifier, it is required to acquire the small signal module from current deviation amplifier outputting to feedback inductor current. Refer to the figure 7.1 for inductor current control loop and we can obtain as follows via state average method:

$$L\frac{dI_{in}}{dt} = V_{in} - (1-d)V_d \tag{7.9}$$

$$\frac{\tilde{I}_{in}}{\tilde{d}} = \frac{V_d}{sL} \tag{7.10}$$

From the (6.22), we may obtain the small signal module of current loop as follows when taking PWM and current sense gain into account.

$$H_i(s) = \frac{\tilde{I}_s}{\tilde{V}_{con}} = \frac{\tilde{I}_{in}K_s}{\tilde{d}V_s} = \frac{K_s V_d}{sLV_s} \tag{7.11}$$

The limit of current loop bandwidth is determined by change rate of PWM control voltage (V_{con}), which should be no greater than change rate of sawtooth wave voltage; that is to say, rising slope of V_{con} must be smaller than that of sawooth wave ($=V_s f_s$). Because V_{con} is acquired from sensed inductor current descending slope reversely amplified by GCA, we can obtain as follows:

$$G_{CA}(\omega_{ci})K_s(V_d - V_{in})/L \leqq V_s f_s \tag{7.12}$$

From the above equation where ωci stands for the zero crossing point (bandwidth) of current loop. Due to input voltage (Vin) fluctuating in accord with sinusoidal wave, when inductor current descending slope appears by the time of zero voltage, the limit of current loop bandwidth, based on the (6.24), will be as follows:

$$G_{CA}(\omega_{ci})K_s V_d/L = V_s f_s \tag{7.13}$$

It, therefore, becomes to:

$$G_{CA,\max} = \frac{\tilde{V}_{con}}{\tilde{I}_s} = \frac{V_s f_s L}{V_d K_s} \tag{7.14}$$

From the (7.11) and (7.14), we acquire as follows via $\omega_{ci}=2\pi f_{ci}$:

$$G_{CA,\max}(\omega_{ci})H_i(\omega_{ci}) = \frac{f_s}{2\pi f_{ci}} = 1 \tag{7.15}$$

From the (7.15), the maximum bandwidth of current loop will be as follows:

$$f_{ci} = \frac{f_s}{2\pi} \tag{7.16}$$

When the second-class deviation amplifier is adopted, as the figure 7.3(a), by G_{CA}, it becomes as follows:

$$G_{CA}(s) = \frac{1 + sR2C1}{sR1(C1 + C2)(1 + sR2C1C2/C1 + C2)} = \frac{K(s+Z)}{s(s+P)} \tag{7.17}$$

$$P = \frac{1}{R_2C_2}\ ,\ Z = \frac{1}{R_2C_1} \tag{7.18}$$

As the figure 7.3(b) shown, first draw the bode plot of Hi followed by setting $f_{ci} < f_s/2$ to obtain $|G_{CA}(f_{ci})| = 1/H_i(f_{ci})$. Specify R_1 to acquire $R_2 = R_1 |G_{CA}(f_{ci})|$. Set P and Z before $P = 3\omega_{ci}$ and $Z = \omega_{ci}/3$, $\omega_{ci} = 2\pi f_{ci}$ followed by referring to (7.18) to acquire $C_1$and C_2.

Figure 7.3

GCA design:
(a) Deviation amplifier circuit

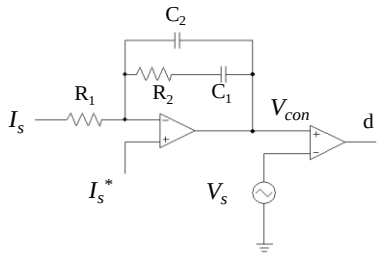
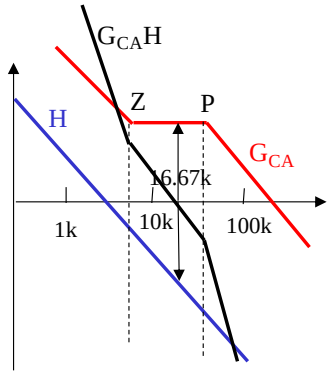


Figure 7.3

GCA design:
(b) Bode plot



B. V

oltage loop design

As the figure 7.4 shown, under the circumstance of unit power factor, the input power factor of single-phased CCM step-up PFC converter can be illustrated as follows:

$$\begin{aligned} P_{ac} &= V_m \sin\omega t \cdot I_m \sin\omega t \\ &= \frac{V_m I_m}{2} - \frac{V_m I_m}{2}\cos 2\omega t \\ &= \overline{P}_{ac} + \widetilde{P}_{ac2} \end{aligned} \tag{7.19}$$

The equation above contains a real power $\overline{P}_{ac}$ and a two-times reactive power $\widetilde{P}_{ac2}$. As mentioned previously, the real power $\overline{P}_{ac}$ is in charge of adjustment of DC output voltage, whilst the two-times reactive power $\widetilde{P}_{ac2}$ has no effect on voltage adjustment but simply causes 2-times ripple of output voltage. Consequently, $\overline{P}_{ac}$ is the only consideration for the adjustment of voltage loop. We may acquire as follows on the basis of power balance.

$$\overline{P}_{ac} = P_{dc} \tag{7.20}$$

That is to say:

$$\frac{V_m I_m}{2} = V_d I_d \tag{7.21}$$

If adopting the control architecture as the figure 7.1, we may obtain the small signal module as follows via (7.21) and (7.5):

$$\widetilde{I}_d = \frac{V_m \widetilde{I}_m}{2V_d} = \frac{V_m \widetilde{V}_{ea}(K_v V_m)}{2V_d K_s} = k_{dc}\widetilde{V}_{ea} \tag{7.22}$$

Where

$$k_{dc} = \frac{K_v V_m^2}{2V_d K_s} \tag{7.23}$$

In terms of 2-class circuit, the small signal module can be illustrated as the figure 7.4(b) shown, and we further acquire as follows via (7.23) and the figure 7.4(b):

$$\frac{\widetilde{V}_d}{\widetilde{V}_{ea}} = \frac{k_{dc}}{sC} \tag{7.24}$$

Figure 7.4

Voltage loop module derivation of single-phased CCM step-up PFC converter:

(a) The equivalent circuit under the unit power factor

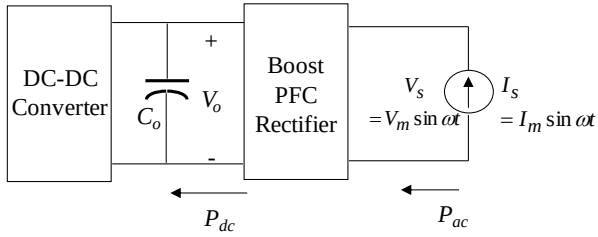
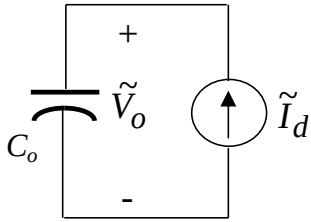


Figure 7.4

Voltage loop module derivation of single-phased CCM step-up PFC converter:

(b) Small signal equivalent circuit



Utilize (7.24) to draw the control block diagram of voltage loop as the figure 7.5(a) shown, where:

$$H_v(s) = \frac{\tilde{v}_d}{\tilde{V}_{ea}} = \frac{k_{dc} k_v}{sC_o} \tag{7.25}$$

Refer to the figure 7.5(b) for the voltage loop bode plot where zero crossing frequency takes the previously mentioned output voltage, due to two-times reactive power causing 2-times ripple, into account. Hence, voltage deviation amplifier G_v adopts the second-class compensator, which is supposed to be, along with zero crossing frequency (f_c) of loop gain $G_v H_v$ built by H_v, lower than the 2-times ripple frequency ($2f_o$ =120Hz) to attenuate the the 2-times ripple of V_{ea} so that output current will be prone to low distortion.

On the other hand, because the zero crossing frequency (f_c) is equivalent to bandwidth of voltage loop, a narrower (f_c) results in deficiency of voltage active response.

Therefore, the best suitable zero crossing frequency generally is set 20Hz, which properly takes both voltage response speed and input current distortion into consideration.

In respect of universal input voltage 90~264Vac, which has approximately 3 times fluctuation, due to the fact that gain (k_{dc}) of voltage loop Hv is affected by fluctuation from square of input voltage indicated as (6.33), H_v gain will result in fluctuation of 9 times (≈20dB). Hence, as the figure 7.5 shown, the zero crossing frequency $f_c(H)$ and $f_c(L)$ generated by loop gain G_vH_v when input voltage is in the moment of highest and lowest, respectively, turns out to be with disparity of 10 times approximately.

For example, when $f_c(H)$=20Hz comes from the design of voltage loop control with higher input voltage parameter, the lower input voltage will cause a narrower bandwidth of voltage loop $f_c(L)$=2Hz, thus making voltage response slower.

On the contrary, when $fc(L)$=20Hz comes from the design of parameter of lower input voltage, it results in wider bandwidth $f_c(H)$=200Hz during high input voltage, being unable to attenuate composition of 2-times ripple of output voltage, which further causes deteriorating current distortion, among other issues.

Figure 7.5

Voltage loop design of control architecture based on figure 6.3:

(a) Control block diagram

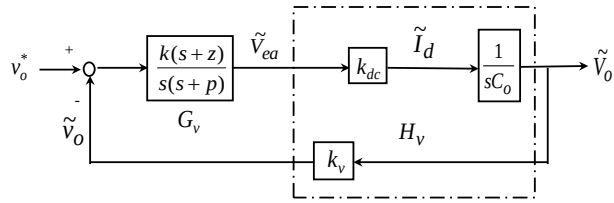
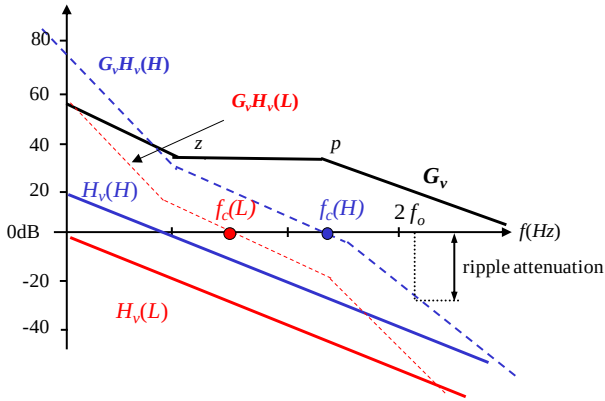


Figure 7.5

Voltage loop design of control architecture based on figure 6.3:

(b) Bode plot



C. T

o add feedforward contro l

In an attempt to overcome the 9 times fluctuation of loop gain derived from 3 times fluctuation of input voltage, it is recommended to utilize the dual-loop average current control architecture with feedforward control indicated as the figure 7.2, further obtaining the small signal module via (7.21) and (7.8).

$$I_d = \frac{V_m I_m}{2V_d} = \frac{V_m V_{ea}(K_v V_m)}{2V_d K_s K (K_v V_m)^2} = k_{dcf} V_{ea} \tag{7.26}$$

In which:

$$k_{dcf} = \frac{1}{2V_d K_s K_v K} \tag{7.27}$$

Redraw, based on (7.27), the control block diagram (7.6(a)) of voltage loop, where:

$$H_v(s) = \frac{\tilde{v}_d}{\tilde{V}_{ea}} = \frac{k_{dcf} k_v}{sC_o} \tag{7.28}$$

Refer to the figure 7.6(b) for the bode plot of voltage loop, because bode plot of H_v is fixed for each input voltage, the design of G_v deviation amplifier aims only at single H_v, and puts the zero crossing frequency fc within 20Hz(=125rad/s) to attenuate voltage ripple of 120Hz($2f_o$).

In general, the zero point and pole of the second-class deviation amplifier G_v are positioned within z=20~30rad/s, p=180~250rad/s.

Figure 7.6

Voltage loop design of control architecture based on figure 7.2:

(a) Control block diagram

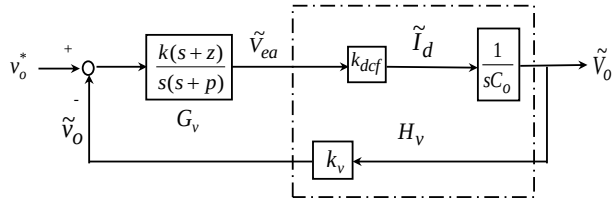
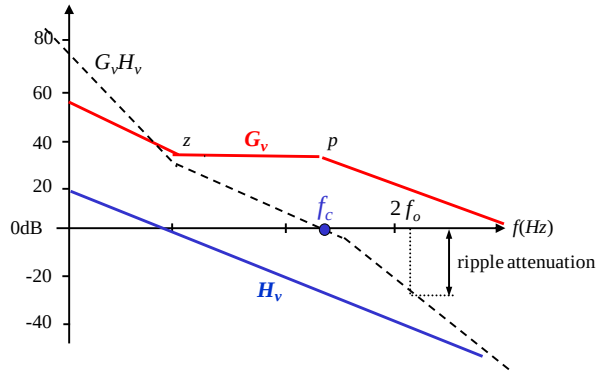


Figure 7.6

Voltage loop design of control architecture based on figure 7.2:

(b) Bode plot



The working principle of single-phased CCM bridgeless step-up converter

To improve efficiency of PFC pre-amplifier, due to conventional step-up PFC converter whose conduction loss of input full bridge rectifier occupies converter by percentage of large scale, a variety of bridgeless PFC circuit architecture are present accordingly. Refer to the figure 7.7 for the foremost released bridgeless step-up PFC converter with mechanism indicated as the figure 7.8. S_1 and D_1 are in operation during positive half cycle and bypass diode of S_2 is treated as rectified diode, remaining conduction during the period of positive half cycle, whilst S_2 and D_2 are in operation during negative half cycle and bypass diode of S_1 is treated as rectified

diode, remaining conduction during the period of negative half cycle. Due to switch in low bandwidth, MOSFET switch bypass diode of S_1 and S_2 is quite enough for use.

Compared with the conventional architecture, whether it's positive or negative half cycle of AC, it has one less diode in components, which practically reduce the conduction loss, when switch in conduction and AC input voltage in conduction.

However, it comes with deficiency that the negative terminal of DC output voltage and the relative voltage of AC voltage are fluctuating high bandwidth; more than that, the size is the exactly voltage level of DC output, and the fluctuating high bandwidth voltage will charge/discharge on output negative terminal and ground terminal of grid-connected electricity, thus resulting in critical common-mode noise, which requires, as a result, higher investment in EMI prevention circuit.

Figure 7.7

Bridgeless step-up PFC converter

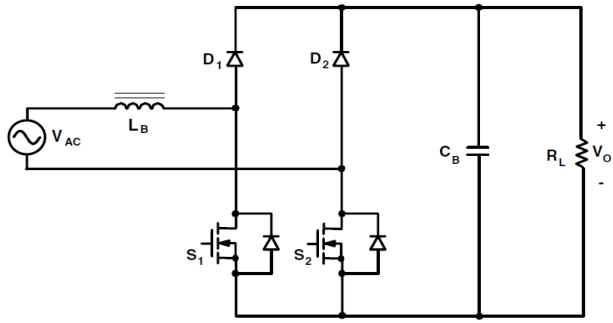


Figure 7.8

The operation of bridgeless step-up PFC converter:

(a) Positive half cycle

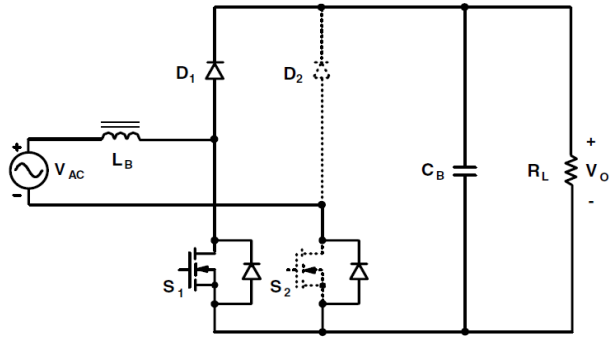
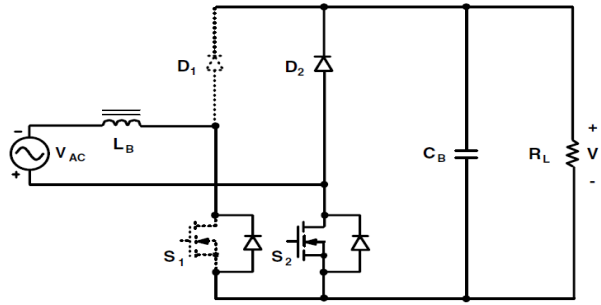


Figure 7.8

The operation of bridgeless step-up PFC converter"

(b) Negative half cycle

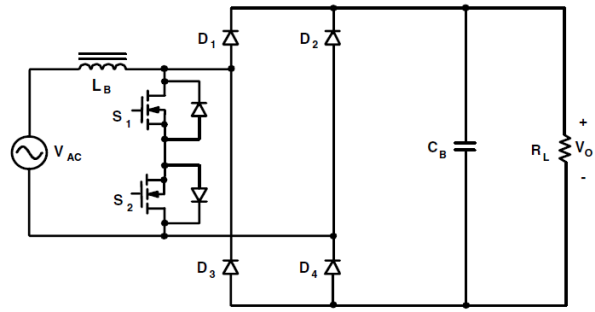


To improve the shortcoming of high-bandwidth common-mode current (figure 7.7), the bidirectional switch bridgeless step-up PFC converter (figure 7.9) is employed, and conducting path has only 2 switches when conduction is active, whether it's positive or negative half cycle. By the time conduction is close, D_1 and D_2 will proceed to high-bandwidth switch to transfer power to DC link, while the diode D_3 and D_4 will proceed to low-bandwidth switch; therefore, negative terminal of DC output voltage and relative voltage of AC voltage are low-bandwidth fluctuation.

Either conduction loss or common-mode current has leaping enhancement, compared with the figure 7.7. In addition, the trigger of 2 switches is common ground and the trigger circuit design is accordingly way compact.

Figure 7.9

Bridgeless step-up PFC converter utilizing bidirectional switch

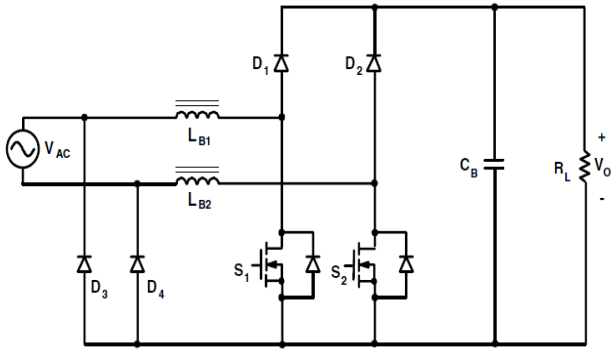


Refer to the figure 7.10 for the bridgeless step-up PFC converter of dual-step-up circuit where L_{B1}-S_1-D_1-D_4 and L_{B2}-S_2-D_2-D_3 form 2 individual step-up converters in the AC positive half cycle and negative half cycle, respectively. D_3 and D_4 are low-bandwidth switch; hence, negative terminal of DC output voltage and relative voltage of AC voltage are low-bandwidth fluctuation accordingly.

The component number of conduction path is equivalent to that of the circuit (figure 7.7) but with 2 inductors, which ease the loss sporadically and has flat and miniature design. The trigger of 2 switches is common ground and is available for similar PWM signal. The trigger circuit design, most importantly, is accordingly way compact.

Figure 7.10

Bridgeless step-up PFC converter utilizing dual step-up circuit

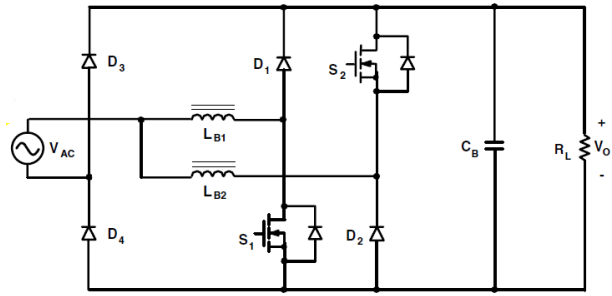


Refer to the figure 7.11 for the bridgeless step-up PFC converter of Pseudo totem-pole where L_{B1}-S_1-D_1-D_4 and L_{B2}-S_2-D_2-D_3 form 2 individual step-up converters in the AC positive half cycle and negative half cycle, respectively. D_3 and D_4 are low-bandwidth switch; hence, negative terminal of DC output voltage and relative voltage of AC voltage are low-bandwidth fluctuation accordingly.

The component number of conduction path is equivalent to that of the dual step-up circuit (figure 7.10). The trigger of 2 switches, however, is non-common ground and requires 2 differed groups of PWM signals individually. The trigger circuit design is complicated.

Figure 7.11

Bridgeless step-up PFC converter of Pseudo totem-pole

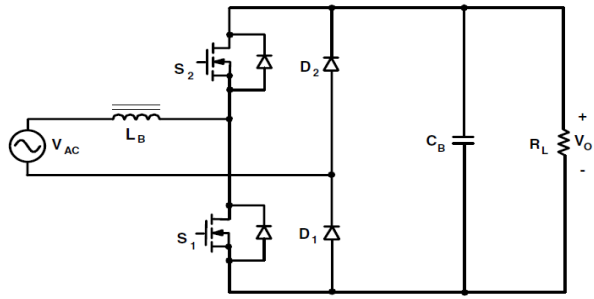


Refer to the figure 7.12 for the bridgeless step-up PFC converter of totem-pole containing a switch arm and a diode arm where the bypass diode of L_B-S_1-D_1-S_2 and the bypass diode of L_B-S_2-D_2-S_1 form 2 individual step-up converter paths in the AC positive half cycle and negative half cycle, respectively. D_1 and D_2 are low-bandwidth switch; hence, negative terminal of DC output voltage and relative voltage of AC voltage are low-bandwidth fluctuation accordingly.

The component number of conduction path is equivalent to that of the dual step-up circuit (figure 7.10). The advantage of it is fewer components employed, and the 2 switches can be triggered via bootstrap drive circuit or by synchronous rectifying method, which greatly enhances the efficiency.

Figure 7.12

Bridgeless step-up PFC converter of totem-pole



Circuit Simulation

Specification of bridgeless step-up PFC converter

- P_o=115W, V_o=40Vac/60Hz,
- V_d = 70V, v_{tri}=18kHz/5V_{pp}, k_s = 1/3.472V/A, k_v = 1/162.2,
- PWM blank time 2μs
- L = 1.323mH, C_d= 330μF

Current loop design

Utilizes the second-class control but puts low-pass portion in sense circuit (f_c =20kHz). The controller adopts proportional integral control ($G_{ca} = \frac{s+1000}{s}$), and a feedforward control signal ($= \frac{V_d - V_{in}}{k_{pwm}}, k_{pwm} = \frac{V_d}{v_t}$) is added in PWM control voltage.

Voltage loop design

- Designed in light of full-load resistor, $R = 49\Omega$. Therefore $H_{dc}(s) = \frac{26.21}{s+61.84}$
- Sets $f_c = 20Hz, \omega_c = 125rad/s$
- Selects p=180rad/s, z=30rad/s of $G_{v,}$ and it turns out $G_v(s) = \frac{30(s+30)}{s(s+180)}$.

PSIM simulation

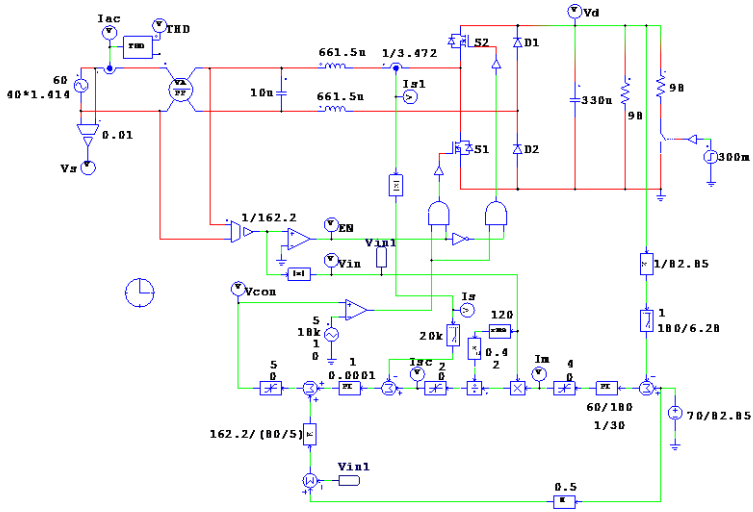


Figure 7.13 The simulating circuit of bridgeless step-up PFC converter of totem-pole

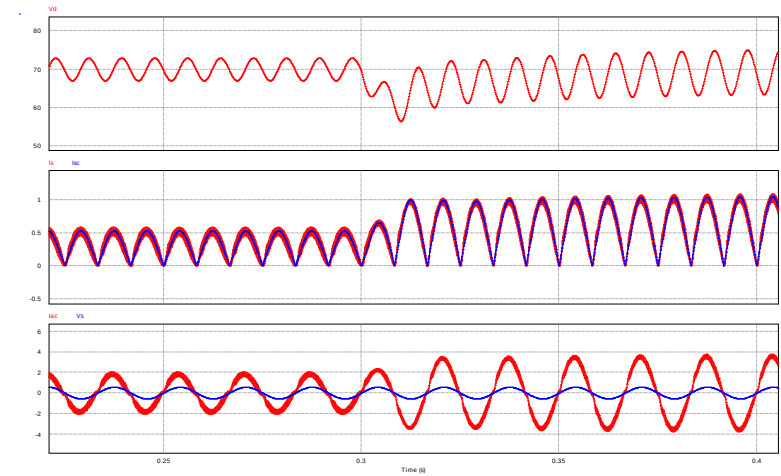


Figure 7.14 The simulating result of bridgeless step-up PFC converter of totem-pole

SimCoder Program Layout and Circuit Simulation

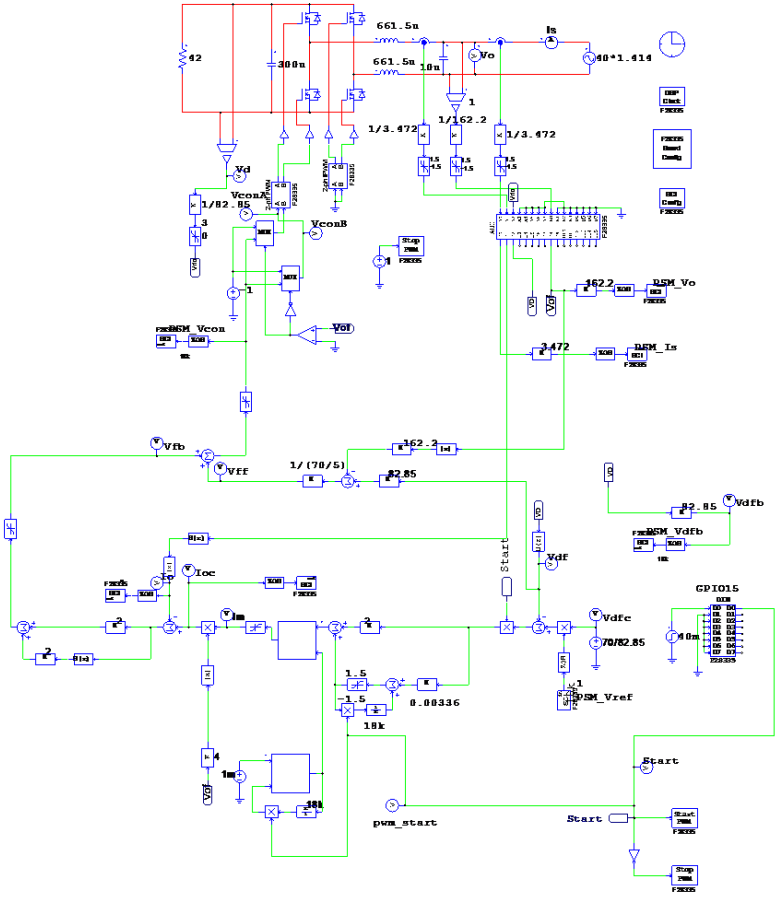


Figure 7.15 The simulating circuit of bridgeless step-up PFC converter of totem-pole built by SimCoder

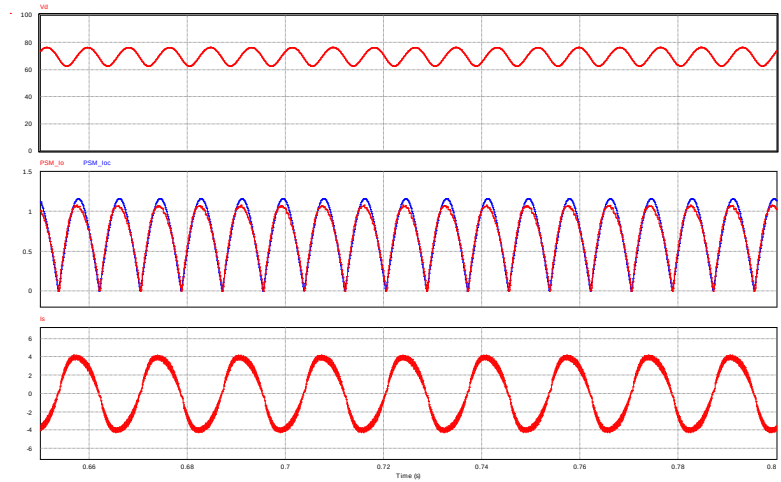


Figure 7.16 The simulating result of bridgeless step-up PFC converter of totem-pole built by SimCoder

Experiment Measurement

The experimental devices and teaching aid layout are illustrated as the figure 7.17. AC power supply APS-7050 is connected to the terminal J7 of PEK-110 and DC load PEL-2040A is connected to the terminal J1 of PEK-110. Refer to the figure 7.18 for the actual measured waveforms. Refer to the figure 7.19 for the waveforms sent from RS232 in DSP oscilloscope.

Figure 7.17

Experiment devices layout

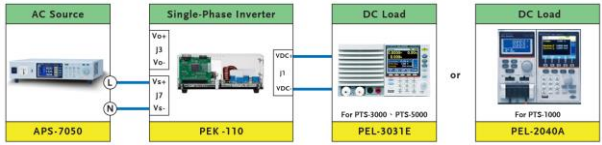


Figure 7.18

The circuit measuring result of bridgeless step-up PFC converter of totem-pole

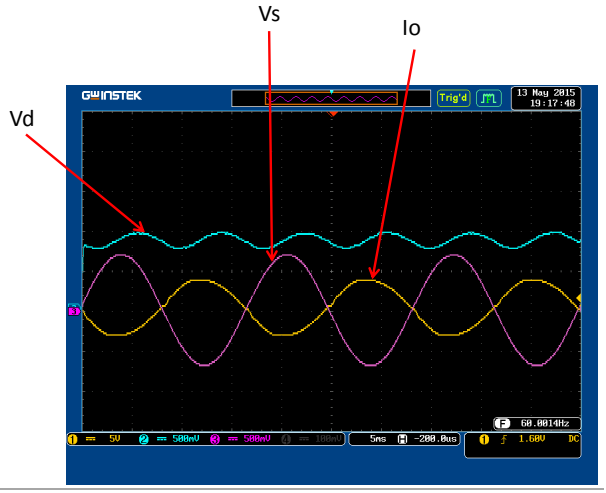


Figure 7.19 (a)

The waveforms sent from RS232 in DSP oscilloscope

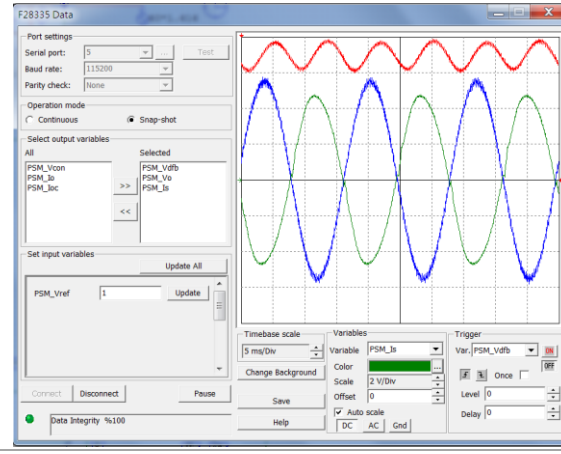
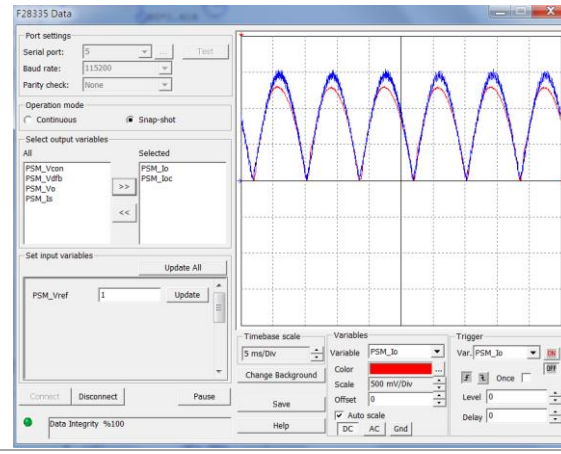


Figure 7.19 (b)

The waveforms sent from RS232 in DSP oscilloscope



Experiment 5 – Full Bridge AC-DC Switchable Rectifier

The purpose of experiment

To learn the principle, current/voltage loop control design and hardware layout as well as SimCoder programming of full bridge AC-DC switchable rectifier.

The principle of experiment

The principle and design of single-phased switchable rectifier

Refer to the figure 8.1 for the single-phased switchable rectifier whose input is AC voltage Vs, and output is DC voltage V_d. It utilizes dual loop design where outer loop is DC voltage control loop used to adjust V_d, whilst inner loop is current loop used to adjust input current (I_s = -I_o) and input voltage into same phase with sinusoidal wave with low distortion rate, thus reaching the very goal of unit power factor.

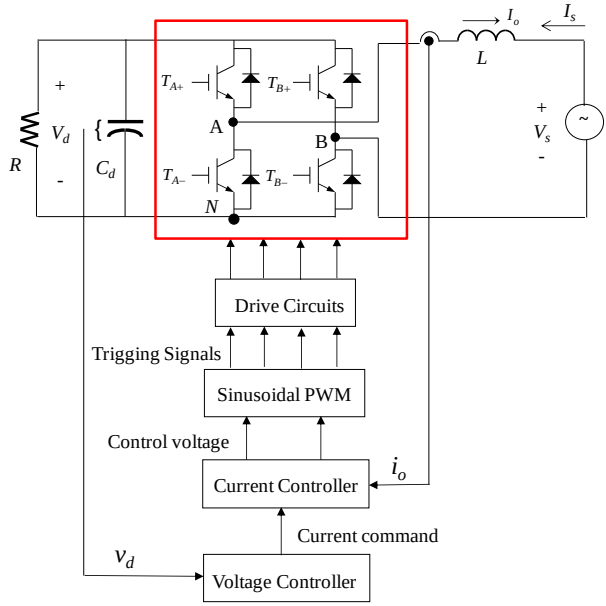
The current loop module of single-phased switchable rectifier is applicable to the previous rectifier module. Refer to the figure 8.2 for the control block diagram in which k_s and k_v are sense gain of current and voltage, respectively. The current control utilizes both feedback and feedforward controls. If input current reaches the same unit power factor as the input voltage, feedforward control signal v_o^*can be used to remove the disturbance to current loop from V_s, and v_o^* is the output voltage command. Therefore, current loop can be feedback loop to acquire as follows:

$$\frac{i_o}{i_o^*} = \frac{\frac{k_s k_1 k_{pwm}}{L}}{s + \frac{k_s k_1 k_{pwm}}{L}} = \frac{u_R}{s + u_R} \quad , \; u_R = \frac{k_s k_1 k_{pwm}}{L} \tag{8.1}$$

u_R is equivalent to bandwidth of input current loop, which can be set by gain k_1. The general bandwidth setting is 1/10~1/5 frequency of the switch frequency.

Figure 8.1

Single-phased switchable rectifier



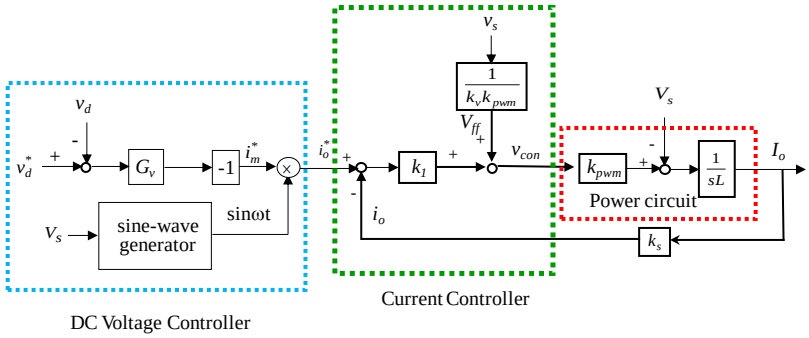


Figure 8.2 Control circuit design

Outer loop DC voltage control G_v generates the current command (io*) of rectifier, which results from the deviation of voltage adjustment multiplied by the unit sinusoidal wave (*sinωt*) of input voltage synchronization. The design of G_v derives from module of DC voltage loop, which is based on the equivalent circuit of unit power factor within the figure 8.3(a); the input power of AC side is as follows:

$$P_{ac} = V_{s(p)} \sin \omega t \cdot I_m \sin \omega t = \frac{V_{s(p)} I_m}{2} - \frac{V_{s(p)} I_m}{2} \cos 2\omega t \quad (8.2)$$
$$= \overline{P}_{ac} + \widetilde{P}_{ac2}$$

In addition to a DC item, a two-times harmonic wave item is also included, which will cause 2-times ripples in DC voltage. The average power of DC side is equal to DC item of AC side power.

$$\overline{P}_{ac} = P_{dc}$$

The equivalent circuit from the following figure 8.3(b) derives from AC current source responding to AC side. Based on the (8.2) we acquire as follows:

$$\frac{V_{s(p)} I_m}{2} = V_d I_d \quad (8.3)$$

$$I_d = \frac{V_{s(p)} I_m}{2V_d} = k_{dc} I_m \quad (8.4)$$

From DC current source Id charging Cd capacitor, we may obtain the module of voltage loop as follows:

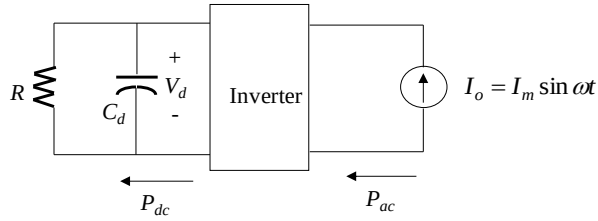
$$\frac{V_d}{I_m} = \frac{k_{dc} R}{1 + sC_d R} = \frac{\frac{k_{dc}}{C_d}}{s + \frac{1}{RC_d}} = \frac{k_{dc} / C_d}{s + a} \text{ , } k_{dc} = \frac{V_{s(p)}}{2V_d} \text{ , } a = \frac{1}{RC_d} \quad (8.5)$$

Make use of the block diagram of voltage control loop from figure 8.4(a) to design voltage control G_v, where due to current loop has much wider in bandwidth over voltage loop, the current loop response from (8.1) should be simplified to be equal to 1. Therefore, the gain of current amplitude I_m from I_m^* to actual Io is the reciprocal of current sense ratio ks, and it is able to, via the bode plot of voltage loop H_{dc}, draw the following figure 8.4(b).

Besides, considering the 2-times ripple of DC voltage, in order to lower down distortion in grid-connected electricity current

command, bandwidth of voltage loop is supposed to be far lower than 120Hz to attenuate the 2-times ripple of voltage. Hence, G_v, adopts the design of type II compensator (i.e., PI + Low-Pass), where the bode plot is illustrated as the figure 8.4(b), and the loop response and the response of PI controller adopted only are illustrated within the figure 8.4(b) for comparison reference.

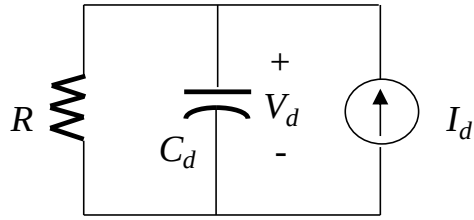
Figure 8.3



The equivalent circuit of single-phased switchable rectifier voltage loop:

(a) The equivalent circuit of unit power factor

Figure 8.3



The equivalent circuit of single-phased switchable rectifier voltage loop:

(b) The equivalent circuit of AC current source responding to DC side

Figure 8.4

DC voltage controller design:

(a) Voltage loop control block diagram

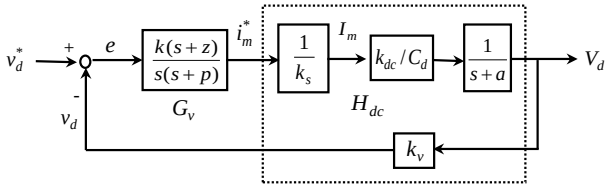
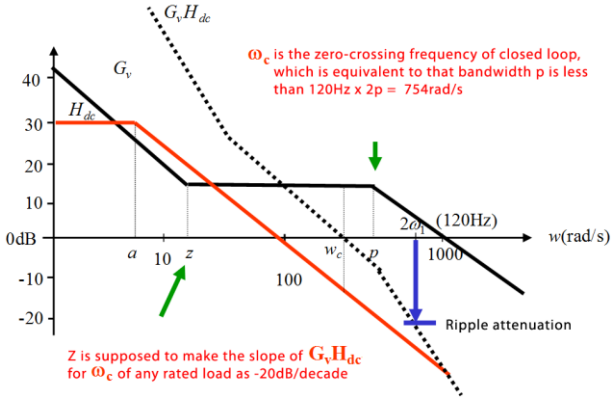


Figure 8.4

DC voltage controller design:

(b) Bode plot of voltage loop



Circuit Simulation

Rectifier specification

- P_o=115W, V_o=40Vac/60Hz,
- V_d = 70V, v_{tri}=18kHz/5V_{pp}, k_s = 1/3.472V/A, k_v = 1/162.2,
- Utilize unipolar voltage switching with blank time 2μs
- L = 1.323mH, C_d= 330μ

Current loop design

- $k_{pwm} = 70/2.5 = 28$
- $f_{ci} = 18k/10 = 1.8kHz$
  $u_R = 1.8k \times 2\pi = 11310 rad/s$
  $k_1 = 1.68$

Voltage loop design

- Design via full-load resistor and $R = 49\Omega$.
  Hence, $H_{dc}(s) = \dfrac{26.21}{s + 61.84}$
- Set $f_c = 20Hz, \omega_c = 125 rad/s$
- When selecting p=180rad/s, z=30rad/s of G_v, it becomes $G_v(s) = \dfrac{1141(s+30)}{s(s+180)}$

PSIM Simulation

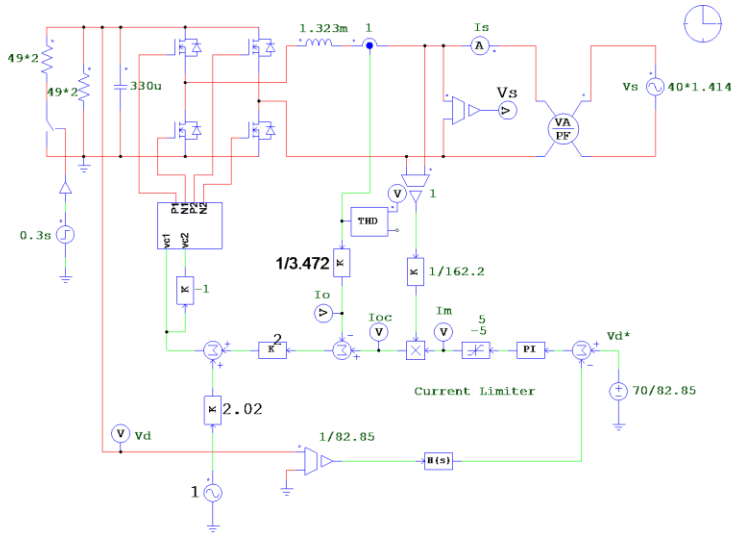


Figure 8.5 The simulating circuit (current loop controlled by P) of load fluctuation from 98Ω το 49Ω

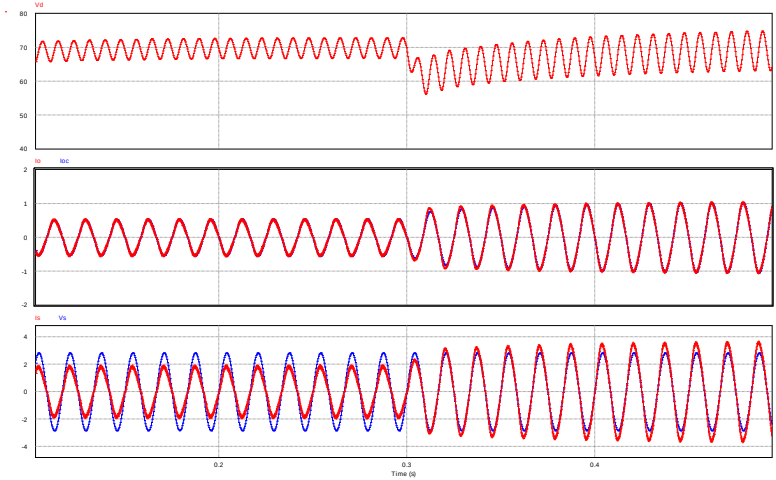


Figure 8.6 The simulating result of load fluctuation from 98Ω το 49Ω

SimCoder Programming Layout and Circuit Simulation

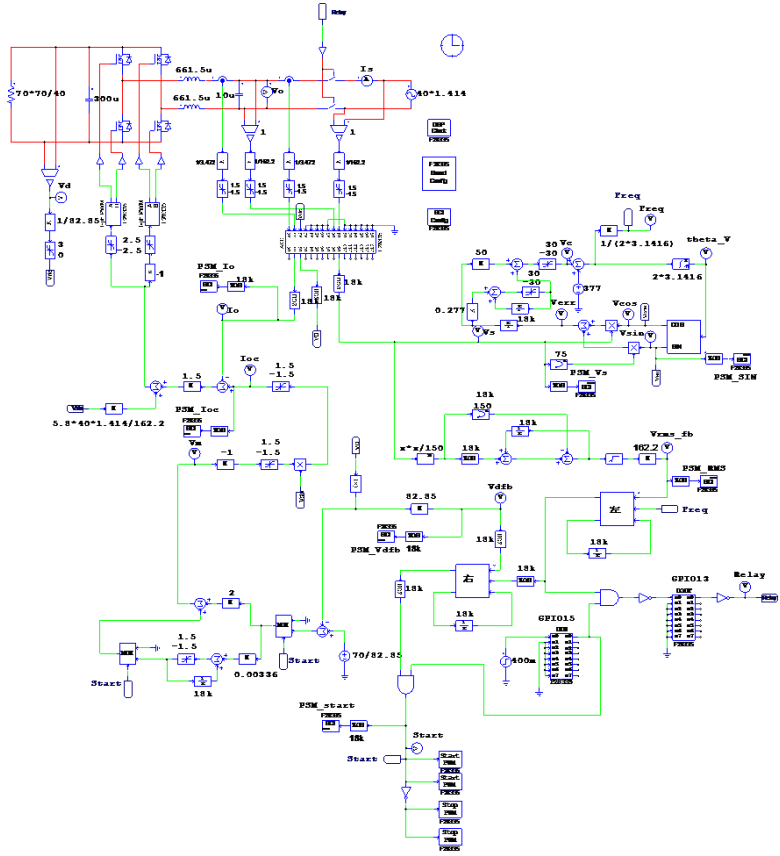


Figure 8.7 The simulating circuit of single-phased switchable rectifier built by SimCoder

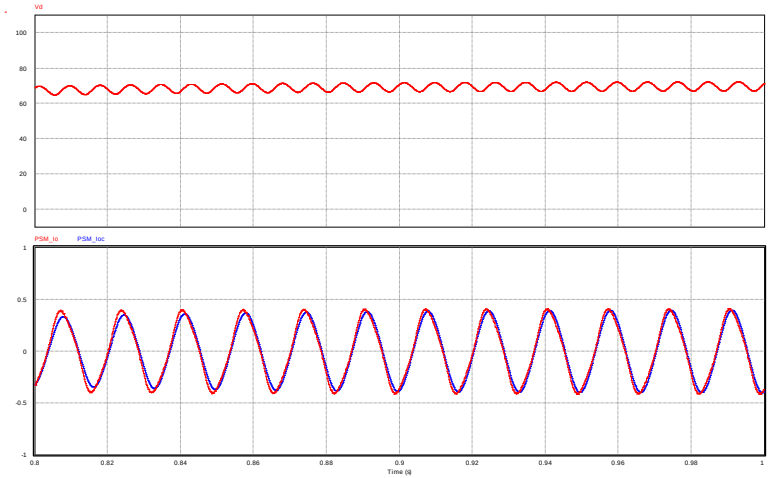


Figure 8.8 The simulating result of single-phased switchable rectifier built by SimCoder

Experiment Measurement

Refer to the figure 8.9 for the layout of experimental devices and teaching aid. AC power supply APS-7050 is connected to the terminal J7 of PEK-110 and DC load PEL-2040A is connected to the terminal J1 of PEK-110. Refer to the figure 8.10 for the actual measured waveforms.

Figure 8.9

Experiment device layout

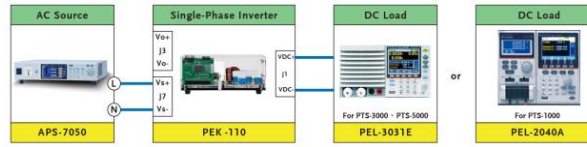


Figure 8.10

The circuit measured result of single-phased switchable rectifier